CONFIDENTIAL
TM 9-1430-250-35
DEPARTMENT OF THE ARMY TECHNICAL MANUAL

FIELD AND DEPOT MAINTENANCE:
THEORY:
ACQUISITION RADAR SYSTEM
(NIKE-HERCULES ANTIAIRCRAFT
GUIDED MISSILE SYSTEM)   (U)

HEADQUARTERS, DEPARTMENT OF THE ARMY
FEBRUARY 1960

CON~~FIDENTIAL~~

WARNING

HIGH VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Be careful not to contact high-voltage connections or 120-volt ac input connections when installing or operating this equipment.

Operators aiding the organizational maintenance technician should observe the following warnings.

Normally, repairmen should not be permitted to work on electronic equipment unless there is another person nearby who is familiar with the hazards of the equipment and is competent in administering first aid.

Whenever possible, power to the equipment should be cut off before beginning work on equipment. Particular care must be taken to ground any capacitor likely to hold a dangerous potential. When working inside the equipment after the power has been turned off, always ground every part before touching it.

Whenever the nature of the operation permits, only one hand should be used for working on electronic equipment. This precaution reduces the probability of current flowing through vital organs of the body, thereby causing fatal injuries.

Fail le 28/9/62? pan Sgt HumPert

TM 9-1430-250-35
C8
SERVICE TECHNIQUE

TECHNICAL MANUAL

FIELD AND DEPOT MAINTENANCE
THEORY: ACQUISITION RADAR SYSTEM (LESS HIPAR)
(NIKE-HERCULES AND IMPROVED NIKE-HERCULES AIR
DEFENSE GUIDED MISSILE SYSTEMS) (U)

TM 9-1430-250-35

CHANGES No. 8

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D. C., *22 June 1962*

TM 9-1430-250-35, 24 February 1960, is changed as follows:

1 (U). The effectivity for material in these changes is as specified in paragraph 3.

2 (U). The effectivity column in paragraph 3 indicates the production cut-in serial number of materiel which has been modified, the DA MWO which contains instructions for modifying existing materiel produced prior to this production cut-in serial number, and changes which apply to·all systems. Process these changes as follows:

   a. Insert changes identified as "All systems" in paragraph 3 on receipt of change.

   b. If the serial number of the materiel in use is of the applicable production cut-in serial number or higher, apply changes as indicated in paragraph 3.

   c. If the serial number of the materiel in use is below the applicable production cut-in serial number and the pertinent DA MWO has been accomplished, apply changes as indicated in paragraph 3.

   d. If the serial number of the materiel in use is below the applicable production cut-in serial number, but the pertinent DA MWO has not been accomplished, do not change the manual until such time as the modification is completed. Retain the changed pages with the transmittal sheets in the front of the manual. After each modification is completed, apply changes as indicated in paragraph 3.

3 (U). In accordance with instructions contained in paragraph 2, the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed (and destroyed in accordance with security regulations). The material on a new or revised page affected by these changes is indicated by a vertical line in the margin of the page. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD or ORD G number.

Vaufie pan
Sgt. M. RIVIÈRE
2 5 Juil 1964

i

Old pages	New pages	Effectivity		Production cut-in serial no.
		DA MWO		
5, 6, 6.1	5, 6, 6.1	—		All systems
9, 10	9, 10, 10.1, 10.2	9-1400-268-50		1363
11, 12	11, 12, 12.1-12.3	9-1400-268-50		1363
None	18.01	9-1400-268-50		1363
33, 34	33, 34, 34.1-34.6	9-1400-268-50		1363
46.5	46.5-46.8	9-1400-268-50		1363
47, 48	47, 48	—		All systems
48.1	48.1	—		All systems
64.3, 64.4	64.3-64.7	9-1400-268-50		1363
66.1	66.1	9-1400-268-50		1363
125, 126, 126.1	125, 126, 126.1	9-1430-251-30/11		1363
131, 132	131, 132, 132.01, 132.02	9-1400-268-50		1363
139, 140	139, 140	9-1400-268-50		1363
141, 142	141, 142	9-1400-268-50		1363
149, 150	149, 150, 150.1, 150.2	9-1400-268-50		1363
161, 162	161, 162, 162.01	9-1400-268-50		1363
None	210.1-210.7	9-1400-268-50		1363
211, 212	211, 212	9-1400-268-50		1363
242.5	242.5	9-1400-268-50		1363
244.1, 244.2	244.1, 244.2	9-1430-251-30/14		System suffix serial no. 075
247, 248	247, 248, 248.1-248.8	9-1400-268-50		1363
251-255	251-256	9-1400-268-50		1363
		9-1430-251-30/11		1363
		9-1430-251-30/14		System suffix serial no. 075

4 (U). Retain the transmittal sheets in the front of the manual for future reference.

MWO non/auti no 1191

ii

TM 9–1430–250–35
C7

TECHNICAL MANUAL
FIELD AND DEPOT MAINTENANCE:
THEORY: ACQUISITION RADAR SYSTEM (LESS HIPAR)
(NIKE-HERCULES AND IMPROVED NIKE-HERCULES AIR
DEFENSE GUIDED MISSILE SYSTEMS) (U)

TM 9–1430–250–35 }

CHANGES NO. 7 }

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D. C., *26 March 1962*

TM 9–1430–250–35, 24 February 1960, is changed as follows:

1 (U). The effectivity for all material in these changes is DA MWO 9–1400–263–30.

2 (U). Apply all changes as indicated herein.

3 (U). In accordance with instructions contained in paragraph 2, the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed and destroyed in accordance with AR 380–5. The material on a new or revised page affected by these changes is indicated by a vertical line in the margin of the page. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD or ORD G number.

Old pages	New pages
5, 6, 6.1, 7, 8	5, 6, 6.1, 7, 8
22.3, 22.4	22.3–22.9
40.3–40.5	40.3–40.9
66.1	66.1
90.1, 80.2	90.1, 90.2
99, 100	99, 100, 100.1
131, 132, 132.1, 132.2	131, 132, 132.1, 132.2
139, 140	139, 140
243, 244, 244.1–244.3	243, 244, 244.1–244.4
247, 248	247, 248
251–254	251–255

4 (U). Retain the transmittal sheets in the front of the manual for future reference.

**DOWNGRADED AT 3 YEAR INTERVALS
DECLASSIFIED AFTER 12 YEARS.
DOD DIR 5200.10**

Sgt. M. RIVIERE
2 5 JUIL 1964

By Order of the Secretary of the Army:

G. H. DECKER,
General, United States Army,
Chief of Staff.

Official:

J. C. LAMBERT,
Major General, United States Army,
The Adjutant General.

Distribution:

To be distributed in accordance with DA Form 12-32, Sec II (Clas) requirements for Nike-Herc, Imp Nike-Herc, TM, Ground Control Equipment.

TECHNICAL MANUAL

Field and Depot Maintenance:

THEORY: ACQUISITION RADAR SYSTEM (LESS HIPAR)

(NIKE-HERCULES AND IMPROVED NIKE-HERCULES AIR

DEFENSE GUIDED MISSILE SYSTEMS) (U)

TM 9-1430-250-35

CHANGES No. 6

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D.C., *16 March 1962*

TM 9-1430-250-35, 24 February 1960, is changed as follows:

1 (U). The effectivity for all material in these changes is production cut-in serial number 1363 and DA MWO 9-1430-254-30/1/1 for system serial number 1307 through 1362.

2 (U). Process these changes as follows:

a. If the serial number of the materiel in use is 1363 or higher, apply all changes as indicated herein.

b. If the serial number of the materiel in use is 1307 through 1362 and DA MWO 9-1430-254-30/1/1 has been accomplished, apply all changes as indicated herein.

c. If the serial number of the materiel in use is 1307 through 1362 but DA MWO 9-1430-254-30/1/1 has not been accomplished, do not change the manual until such time as the modification is completed. Retain the changed pages with the transmittal sheet in the front of the manual. After modification is completed, apply changes as indicated herein.

3 (U). In accordance with instructions contained in paragraph 2, the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed (and destroyed in accordance with security regulations). The material on a new or revised page affected by these changes is indicated by a vertical line in the margin of the page. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD or ORD G number.

Old pages	New pages
5, 6	5, 6
233, 234	233, 234
238.2	238.2
242.1-242.6	242.1-242.5

4 (U). Upon incorporation of these changes, the top and bottom of this transmittal sheet will be marked CONFIDENTIAL Modified Handling Authorized in accordance with AR 380-5.

5 (U). Retain the transmittal sheet in the front of the manual for future reference.

Sgt. M. RIVIÈRE

2 5 JUIL 1964

By Order of the Secretary of the Army:

G. H. DECKER,
General, United States Army,
Chief of Staff.

Official:
J. C. LAMBERT,
Major General, United States Army,
The Adjutant General.

Distribution:
To be distributed in accordance with DA Form 12–32, Sec III (Clas) requirements for Nike-Herc/Imp Nike-Herc, TM, Ground Control Equipment.

TM 9–1430–250–35
C 5

TECHNICAL MANUAL

Field and Depot Maintenance

THEORY: ACQUISITION RADAR SYSTEM (NIKE-HERCULES AND IMPROVED NIKE-HERCULES AIR DEFENSE GUIDED MISSILE SYSTEMS) (U)

TM 9–1430–250–35

Changes No. 5

HEADQUARTERS,
DEPARTMENT OF THE ARMY
Washington 25, D.C., *14 September 1961*

TM 9–1430–250–35, 24 February 1960, is changed as follows:

1. (U) The effectivity for material in these changes is as specified in paragraph 4.

2. (U) The effectivity column in paragraph 4 indicates the production cut-in serial number of materiel which has been modified, the DA MWO which contains instructions for modifying existing materiel produced prior to this production cut-in serial number, and changes which apply to all systems. Process these changes as follows:

   a. Insert changes identified as "All systems" in paragraph 4 on receipt of change.

   b. If the serial number of the materiel in use is of the applicable production cut-in serial number or higher, apply changes as indicated in paragraph 4.

   c. If the serial number of the materiel in use is below the applicable production cut-in serial number and the pertinent DA MWO has been accomplished, apply changes as indicated in paragraph 4.

   d. If the serial number of the materiel in use is below the applicable production cut-in serial number, but the pertinent DA MWO has not been accomplished, do not change the manual until such time as the modification is completed. Retain the changed pages with the transmittal sheet in the front of the manual. After modification is completed, apply changes as indicated in paragraph 4.

   e. For those pages having two or more DA MWO's affecting one sheet (pair of pages), insert these pages when any one of the DA MWO modifications has been incorporated. Do not remove the corresponding old pages until all DA MWO modification affecting the sheet have been incorporated. After the last modification is completed, remove the corresponding old sheet (pair of pages).

3. (U) In accordance with instructions contained in paragraph 3, the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed and destroyed in accordance with security regulations. The material on a new page which is affected by these changes is indicated by a vertical line in the margin of the page. Where revised information requires the use of added pages, vertical lines are also used to indicate added material. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD or ORD G number.

Downgraded at 3-Year Intervals:
Declassified After 12 Years
DOD Dir 5200.10

Sgt. M. RIVIERE

i

Old pages	New pages	Effectivity	
		DA MWO	Production cut-in serial No.
5, 6	5, 6	None	All systems
65, 66, 66.1	65, 66, 66.1, 66.2 (blank)	ORD Y28–W35	All systems
		ORD Y29–W33	All systems
131, 132, 132.1, 132.2	131, 132, 132.1, 132.2	9–1430–291–30	K29
139, 140	139, 140	ORD Y28–W35	All systems
		ORD Y29–W33	All systems
243, 244	243, 244	ORD Y28–W35	All systems
		ORD Y29–W33	All systems
		9–1430–291–30	K29
251, 252	251, 252	9–1430–291–30	K29

4. (U) Retain the transmittal sheets in the front of the manual for future reference.

MWO non faits
sur 1191

ii

TM 9–1430–250–35
C4

Fait le 16-5-66
sk officens

TECHNICAL MANUAL

FIELD AND DEPOT MAINTENANCE:

THEORY: ACQUISITION RADAR SYSTEM (LESS HIPAR)

(NIKE-HERCULES AND IMPROVED NIKE-HERCULES AIR DEFENSE

GUIDED MISSILE SYSTEMS) (U)

TM 9–1430 250 35 }

CHANGES No. 4 }

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D. C., *26 July 1961*

TM 9–1430–250–35, 24 February 1960, is changed as follows:

1. (u) These changes contain Improved NIKE-HERCULES coverage. The effectivity for all material in these changes is all systems.

2. (u) Apply all changes as indicated herein.

3. (u) In accordance with instructions contained in paragraph 2, the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed and destroyed in accordance with security regulations. The material on a new page which is affected by these changes is indicated by a vertical line in the margin of the page. Where revised information requires the use of added pages, vertical lines are also used to indicate added material. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD or ORD G number.

Old pages	New pages
5, 6, 6.1	5, 6, 6.1
47, 48, 48.1	47, 48, 48.1
53, 54	53, 54
97, 98, 98.1, 98.2	97, 98, 98.1, 98.2
98.5–98.10	98.5–98.10
137 140	137–140
243, 244, 244.1, 244.2	243, 244, 244.1, 244.2, 244.2.1
251–254	251–254

4. (u) Retain the transmittal sheet in the front of the manual for future reference.

5. (u) Destroy classified pages removed from the manual as a result of this change in accordance with AR380–5.

Sgt. M. RIVIERE
2 5 JUL 1964

i

By Order of the Secretary of the Army:

G. H. DECKER,
General, United States Army,
Chief of Staff

Official:
R. V. LEE,
Major General, United States Army,
The Adjutant General

Distribution:

Active Army:

DCSLOG (1)
Tech Stf, DA (1) except
  CofOrd (3)
  CofEngrs (3)
  CofT (None)
Ord Bd (2)
USCONARC (3)
ARADCOM (5)
ARADCOM Rgn (5)
OS Maj Comd (5) except
  USARCARIB (3)
  USARAL (2)
  USARPAC (3)
OS Base Comd (2)
LOGCOMD (3)
Armies (3) except
  Third USA (8)
  Seventh USA (5)
  EUSA (5)
MDW (1)
Corps (2)
Instls (3) except
  Ft Benning (6)
  Ft Devens (15)
  Ft Hood (13)
  Ft Lewis (13)
  Ft Riley (6)
  Ft MacArthur (8)
  Ft Sheridan (12)
  Ft Wayne (9)
  Ft Monroe (6)
  Ft Belvoir (6)
  Presidio of San Francisco (6)
Svc Colleges (2)
Br Svc Sch (2) except
  US ARADSCH (100)
  USA Drd Sch (5)
  USAAMS (5)
USAOGMS (150)
USMA (3)
GENDEP (1) except
  Schenectady GENDEP (none)
  New Cumberland GENDEP (none)
Ord Sec, GENDEP (1)
Ord Dep (1) except
  Rossford Ord Dep (10)

Tooele Ord Dep (4)
Wingate Ord Dep (3)
Black Hill Ord Dep (5)
Sierra Ord Dep (2)
Savanna Ord Dep (3)
Ord Ammo Comd (2)
USAOMC (5)
Ord SW Ammo Comd (5)
OWC (1)
USA Msl Comd (5)
7th USA Spt Comd (1)
QMRECOMD (1)
Fld Comd, DASA (20)
Philadelphia QM Cen, USA (3)
USAADCEN (10)
WSMR (10)
ARGMA (61)
USA Trans Tml Comd (2)
Army Tml (2)
POE (OS) (2)
OSA (1)
Ord PG (10) except
  APG (13)
Ord Arsenals (1) except
  Benicia Arsenal (3)
  Frankford Arsenal (3)
  Ravenna Arsenal (2)
  Rock Island Arsenal (2)
  Indiana Arsenal (none)
  Radford Arsenal (none)
  Joliet Arsenal (4)
  Raritan Arsenal (17)
  Redstone Arsenal (9)
Springfield Armory (2)
Ord Dist (1) except
  New York Ord Dist (3)
USACOMZEUR (6)
MAAG, Italy (57)
MAAG, Denmark (18)
MAAG, Norway (18)
MAAG, France (11)
MAAG, Belgium (18)
MAAG, W. Germany (55)
MAAG, Republic of China (18)
MAAG, Netherlands (18)
JUSMAGG (18)

TECHNICAL MANUAL

FIELD AND DEPOT MAINTENANCE:
THEORY: ACQUISITION RADAR SYSTEM (LESS HIPAR)
(NIKE–HERCULES AND IMPROVED NIKE–HERCULES AIR DEFENSE
GUIDED MISSILE SYSTEMS) (U)

TM 9–1430–250–35 ⎰   HEADQUARTERS,
                    DEPARTMENT OF THE ARMY
Changes No. 3   ⎱   WASHINGTON 25, D. C., *15 June 1961*

TM 9–1430–250–35, 24 February 1960 is changed as follows:

1. These changes contain Improved NIKE–HERCULES coverage. The effectivity for all material in these changes is all systems.

2. Upon incorporation of these changes, mark CONFIDENTIAL, Modified Handling Authorized at the top and bottom of this page.

3. Apply all changes as indicated herein.

4. In accordance with instructions contained in paragraph 3, the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed and destroyed in accordance with security regulations. The material on a new page which is affected by these changes is indicated by a vertical line in the margin of the page. Where revised information requires the use of added pages, vertical lines are also used to indicate added material. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD or ORD G number.

Old pages	New pages
5–8, 8.1	5, 6, 6.1, 7, 8, 8.1
64.3, 64.4	64.3, 64.4
None	132.5
209, 210	209, 210

5. Pages 4.1, 4.2, Face p. 4.2, 4.3 through 4.8, Face p. 4.8, 4.9, and 4.10 are rescinded and should be removed from the manual.

6. The following pen and ink changes are to be made in the manual.

Page	Par	Line	Action
48	22.1*b*	3	Add "acquisition" after "same as".
132.1	48.2*b*(6)	1, 2, 5, 8, 11	Change "S5" to read S3 in five places
132.1	48.2*b*(8)	3	Delete "down" and substitute "ON".
132.1	48.2*b*(8)	4	Delete "ON" and substitute "down".
132.1	48 3*b*	19	Change "(2) *Frequency switch S1.*" to read (3) **Frequency switch S1.**
132.2	48 3*b*(10)	4	Change "S2" to read **R2.**
132.4	48.5*b*(2)	6	Change "1-2" to read 1–3.
206	77	Title	Chance "9000009" to read 8158120, **9000009.**
244.1	89 1	Title	Delete "9984907" and substitute "9984404".
244.1	89 1*a*	1	Delete "9984907" and substitute "9984404".
249	2nd column	31	On line above "Instruction Guide:" add "First Aid for Soldiers FM 21 11".
252	1st column	5	After "RF" add "8158120, 9000009".
254	1st column	15	Delete "9984907" and substitute "9984404".

7. Retain the transmittal sheets in the front of the manual for future reference.

Sgt. M. RIVIÈRE
2 5 JUIL 1964

TM 9–1430–250–35

TECHNICAL MANUAL

FIELD AND DEPOT MAINTENANCE
THEORY: ACQUISITION RADAR SYSTEM
(NIKE-HERCULES ANTIAIRCRAFT GUIDED MISSILE SYSTEM) (U)

fait le 05-05-62
Pan Sgt RIGAL

TM 9–1430–250–35 ⎱

CHANGES No. 2 ⎰

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D. C., *30 March 1961*

TM 9–1430–250–35, 24 February 1960, is changed as follows:

1. These changes contain Improved NIKE-HERCULES coverage. The effectivity for all material in these changes is all systems.

2. Upon incorporation of these changes the title of this manual becomes as follows:

FIELD AND DEPOT MAINTENANCE:
THEORY: ACQUISITION RADAR SYSTEM (LESS HIPAR)
(NIKE-HERCULES AND IMPROVED NIKE-HERCULES AIR DEFENSE
GUIDED MISSILE SYSTEMS) (U)

3. Apply all changes as indicated herein.

4. In accordance with instructions contained in paragraph 3, the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed and destroyed in accordance with security regulations. The material on a new page which is affected by these changes is indicated by a vertical line in the margin of the page. Where revised information requires the use of added pages, vertical lines are also used to indicate added material. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD or ORD G number.

Old pages	New pages
4.1–4.4	
5–8, 8.1	5–8, 8.1
21, 22	21, 22, 22.1–22.4
33, 34	33, 34, 34.1
39, 40	39, 40, 40.1–40.5
47, 48	47, 48, 48.1
56.1, 57, 58	56.1, 57, 58
62.1, 62.2	62.1–62.2
None	64.1–64.4
66.1	66.1
97, 98	97, 98, 98.1–98.10
111, 112	111, 112, 112.1–112.7
117, 118	117, 118, 118.1–118.5
125, 126	125, 126, 126.1
131, 132, 132.1	131, 132, 132.1–132.4
139, 140	139, 140
243, 244	243, 244, 244.1–244.3
249–254	249–254

5. The following pen and ink changes are to be made in the manual.

Page	Par.	Line	Action
1	Title	1	After "ACQUISITION RADAR SYSTEM" add "(LESS HIPAR)".
1	Title	2	Delete "ANTIAIRCRAFT" and substitute "AND IMPROVED NIKE-HERCULES AIR DEFENSE".
150	58	1	Title should read "Compressor 7605715 or Pressurization Unit 9138649".
213	79	2	After "9000289" add "or 8158132".
240	91b(4)	1, 2	Delete "TA–346/M–8513396" and substitute" or remote control circuit 9139909"

6. Retain the transmittal sheets in the front of the manual for future reference.

TM 9–1430–250–35
C1

TECHNICAL MANUAL

FIELD AND DEPOT MAINTENANCE:
THEORY: ACQUISITION RADAR SYSTEM
(NIKE-HERCULES ANTIAIRCRAFT GUIDED MISSILE SYSTEM) (U)

TM 9–1430–250–35 }

CHANGE No. 1 }

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D.C., *8 December 1960*

TM 9–1430–250–35, 24 February 1960, is changed as follows:

1. The effectivity for material in these changes is as specified in paragraphs 4 and 5.

2. Upon incorporation of these changes the manual is downgraded to CONFIDENTIAL, MODIFIED HANDLING AUTHORIZED.

3. The effectivity columns in paragraphs 4 and 5 indicate the production cut-in serial number of materiel which has been modified, the MWO which contains instructions for modifying existing materiel produced prior to this production cut-in serial number, and changes which apply to all systems. Process these changes as follows:

a. If the materiel in use is of the applicable production cut-in serial number or higher, apply changes as indicated in paragraphs 4 and 5.

b. If the serial number of the materiel in use is below the applicable production cut-in serial number and the pertinent MWO has been accomplished, apply changes as indicated in paragraphs 4 and 5.

c. If the serial number of the materiel in use is below the applicable production cut-in serial number, but the pertinent MWO has not been accomplished, do not change the manual until such time as the modification is completed. Retain the change pages with the transmittal sheets in the front of the manual. After modification is completed, apply changes as indicated in paragraphs 4 and 5.

4. In accordance with instructions contained in paragraph 3 the attached new pages, as enumerated below, will be inserted in the manual and the old pages will be removed. The portion of the material in a new page affected by these changes is indicated by a vertical line in the margin of the page. Where revised information requires use of added pages, vertical lines are also used to indicate changed material. Added or revised illustrations are indicated by a vertical line adjacent to the RA PD number.

i

Old pages	New pages	Effectivity		Production cut-in serial no.
		MWO		
1–3, face p. 4, 5–8	1–3, 4, 1–4, 4, 5–8, 8.1	None		All systems
13–18	13–18, 18. 1, 18.2	Y28–W11, Y28–W32		1247
37–42	37–42, 42.1, 42.2	Y28–W11, Y28–W29		1247
45, 46	45, 46, 46.1–46.5	None		1071
49, 50	49, 50, 50.1, 50.2	None		1287
55–57	55, 56, 56.1, 57	Y28 W24		1219
61–66	61, 62, 62.1, 62 2, 63–66, 66.1	Y28 W11, Y28–W24		1247
67–74	67–74, 74.1, 74.2	Y28–W29		1307
83–92	83–90, 90.1, 90.2, 91, 92	Y28–W29		1307
131, 132	131, 132, 132.1	Y28–W11		1247
151–153	151, 152, 152.1, 153, 154	None		1327
Face p. 162	162.1	None		1287
233–238, face p. 238, 239–242	233–238, 238.1, 238.2 239–242, 242.1–242.6	Y25–W4		1307
243, 244	243, 244, 244.1	Y28–W24		1219
251–254	251–254	None		All systems

5. The following pen and ink changes are to be made in this manual.

Page	Par.	Line	Fig.	Action	Effectivity	
					MWO	Production cut-in serial no.
34	18	1	—	Delete "8174091" and substitute "9142873"	Y28-W29	1307
48	23	1	—	After "7614632" add ", Acquisition 5-Minute Delay Timer-9142969'.	None	1287
58	29	1	—	Delete "8006012" and substitute '9138109".	Y28-W11	1247
59	29b(3)	20	—	After "voltages," add "interlock switch S2 opens an interlock circuit and".	Y28-W11	1247
67	33a(1)	Last	—	Change "200,000" to 250,000.	Y28-W29	1307
67	33a(3) (a)	1	—	Add "or 9007951".	Y28-W29	1307
67	33a(3) (d)	1	—	Delete "8158267" and substitute "9142869".	Y28-W29	1307
67	33a(3) (e)	1	—	Delete "8157989" and substitute '9007680".	Y28-W29	1307
126	48	1	—	Delete "8158840" and substitute "9137929".	Y28-W11	1247
126	48b	2	—	In note change "(20)" to "(21)".	Y28-W11	1247
135	50	1	—	Delete "8518877, 9007757" and substitute "9142872'	Y28-W29	1291
137	50c	—	—	Delete entire paragraph c.	Y28-W29	1291
161	64b(2) (b)	6	—	Add "or the acquisition 5-minute delay timer" after 'timer".	None	1287
180	70a	2	—	Delete "RF" and substitute "IF".	None	All systems
187	74	1	—	Delete "8173949" and substitute "9143030"	Y25-W3	1209
188	74b(1) (a)	21	—	After "C42" add ", C45,"	Y25-W3	1209
245	—	—	106	Delete entire figure.	Y28-W24	1219
247	92	1	—	Delete "8007298" and substitute "8158225".	Y28-W5	1091
247	92	6	—	After "fan." add "and IFF decoder MX-1995/TPX."	Y28-W5	1091
249	4	32	—	In second column change "TM 9-1430-250-10" to TM 9-1400-250-10.	None	All systems
249	4	36	—	In second column change "TM 9-1430-251-12" to TM 9-1400-251-12	None	All systems

6. Retain the transmittal sheets in the front of the manual for future reference.

By Order of *Wilber M. Brucker*, Secretary of the Army:

G. H. DECKER,
General, United States Army,
Chief of Staff.

Official:

R. V. LEE,
Major General, United States Army,
The Adjutant General.

Distribution:
Active Army:
To be distributed in accordance with DA Form 12–7 requirements for TM 9 Series (Class) Plus the following:

DCSLOG (1)	MAAG (Belgium) (18)
Tech Stf, DA (1)	MAAG (West Germany) (18)
except CofOrd (3)	MAAG (Republic of China) (18)
US ARADCOM (2)	MAAG (Netherlands) (18)
US ARADCOM Rgn (2)	JUSMAGG (18)
MDW (1)	JUSMMAT (18)
Seventh US Army (3)	Units org under fol TOE:
EUSA (5)	9–12 (1)
Corps (2)	9–17 (1)
1st GM Bde (50)	9–47 (1)
WSMR (10)	9–57 (2)
MAAG (Italy) (57)	9–76 (2)
MAAG (Denmark) (18)	9–227 (3)
MAAG (Norway) (18)	9–377 (1)
MAAG (France) (11)	9–500 (DD) (3)
	9–510 (FA) (3)

NG & USAR: None.
For explanation of abbreviations used, see AR 320–50.

EXTREMELY DANGEROUS POTENTIALS

greater than 500 volts exist in the following units:

Warning: **Potentials less than 500 volts may cause death under certain conditions; therefore, reasonable precautions should be taken when working in all units of the acquisition radar system.**

Acquisition antenna-receiver-transmitter group:
- Acquisition modulator
- Acquisition receiver-transmitter
- Acquisition RF power supply control

Battery control console:
- PPI
- PPI HV power supply
- Precision indicator

Director station group:
- −1,000v power supply
- Acquisition HV power supply
- Battery control interconnecting box

JUSMMAT (18)
Units org under fol TOE:
  9-12 (1)
  9-17 (1)
  9-47 (1)   ·
  9-57 (2)

9-76 (2)
9-87 (3)
9-227 (3)
9-377 (1)
9 500 (EA,FA,FR) (3)
9-510 (FA) (1)

NG: Units org under fol TOE: 44-545 (4).

USAR: None.

For explanation of abbreviations used, see AR 320-50.

TECHNICAL MANUAL

No. 9–1430 250 35

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D C . *24 February 1960*

THEORY: ACQUISITION RADAR SYSTEM (LESS HIPAR)
HWD IMPROVED NIKE-HERCULES AIR DEFENSE
(NIKE-HERCULES ANTIAIRCRAFT GUIDED MISSILE SYSTEM)   (U)

FIRST AID FOR ELECTRICAL SHOCK

I. GENERAL

a. Rescue. In case of electric shock, shut off the high voltage at once and ground the circuits. If the high voltage cannot be turned off without delay, free the victim from contact with the live conductor as promptly as possible. Avoid direct contact with either the live conductor or the victim's body. Use a dry board, dry clothing, or other non-conductor to free the victim. An axe with a dry wooden handle may be used to cut the high-voltage wire. Use extreme caution to avoid the resulting electric flash.

b. Symptoms.

(1) Breathing stops abruptly in electric shock if the current passes through the breathing center at the base of the brain. If the shock has not been too severe, the breath center recovers after a while and normal breathing is resumed, provided that a sufficient supply of air has been furnished meanwhile by artificial respiration.

(2) The victim is usually very white or blue. The pulse is very weak or entirely absent and unconsciousness is complete. Burns are usually present. The victim's body may become rigid or stiff in a very few minutes. This condition is due to the action of electricity and is not to be considered rigor mortis. Artificial respiration must still be given, as several such cases are re-ported to have recovered. The ordinary and general tests for death should never be accepted.

II. MOUTH-TO-MOUTH ARTIFICIAL RESPIRATION

Start artificial respiration immediately. Do not wait for a mechanical resuscitator; but when an approved model is available, use it. At the same time send for a medical officer if assistance is available. Do not leave the victim unattended. Perform artificial respiration at the scene of the accident, unless the victim's or operator's life is endangered from such action. In this case only, remove the victim to another location, but no farther than is necessary for safety. If the new location is more than a few feet away, artificial respiration should be given while the victim is being moved. Artificial respiration, once started, must be continued without loss of rhythm. The mouth-to-mouth method of artificial respiration is described here.

III. TECHNIQUE OF MOUTH-TO-MOUTH ARTIFICIAL RESPIRATION

1. Position of Victim (A). Place victim in the face upward position and kneel close to his left ear.

2. Clear the Throat. Turn the head to one side, and quickly wipe out any fluid, mucus, or foreign body from mouth and throat with the fingers.

3. Open and Aline Air Passages. Tilt the head back and extend the neck to open

and aline the air passages, so that they do not become blocked by kinking or pressure.

4. <u>Lift Jaw Forward.</u> Place the thumb into the mouth and grasp the jaw firmly. Lift the jaw forward to pull the tongue forward out of the air passage. Do not attempt to hold or depress tongue.

5. <u>Pinch Nostrils Closed.</u> Use other hand to keep the victim's nostrils pinched closed to prevent air leak.

6. <u>Form Tight Seal with Lips</u> (B). Rescuer's <u>wide-open</u> mouth completely surrounds and seals the open mouth of the victim. This is not a kissing or puckered position - the mouth of the rescuer must be wide open.

7. <u>Blow.</u> Exhale firmly into victim's mouth until the chest is seen to lift. This can be seen by the rescuer without difficulty.

8. <u>Remove Mouth and Breathe In</u> (C). During this time, rescuer can hear and feel the escape of air from the victim's lungs.

9. <u>Repeat 6, 7, and 8.</u> Continue at a rate of 12-20 times per minute.

CAUTION: EXCESSIVELY DEEP AND RAPID BREATHING BY THE RESCUER MAY CAUSE HIM TO BECOME FAINT, TO TINGLE, AND EVEN LOSE CON-SCIOUSNESS. BREATHING SHOULD BE NORMAL IN RATE WITH ONLY MODER-ATE INCREASE IN VOLUME. IN THIS WAY, RESCUE BREATHING CAN BE CONTINUED FOR LONG PERIODS WITHOUT FATIGUE.
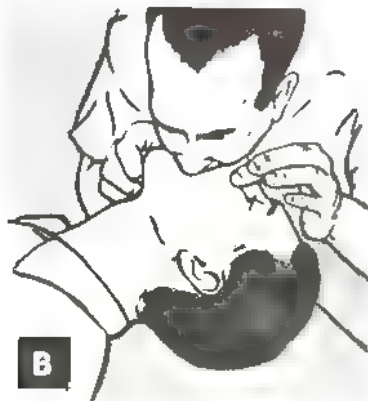
10. <u>Remember.</u>

<u>a</u>. Keep airway clear of fluid and other obstruction.

<u>b</u>. Readjust position if air does not flow freely in and out of victim.

<u>c</u>. Keep neck extended and chin pulled forward.

<u>d</u>. Do not breathe too forcible or too large a volume if victim is infant or small child.

RA PD 461689

CHAPTER 1 (U)

INTRODUCTION

1 (U). Scope

a. These instructions are published for the information and guidance of personnel responsible for field and depot maintenance of the NIKE-HERCULES and Improved NIKE-HERCULES Air Defense Guided Missile Systems. These instructions contain information on maintenance which is beyond the scope of the tools, equipment or supplies normally available to using organizations. This manual does not contain information which is intended primarily for the using organization, since such information is available in the pertinent operator and organizational maintenance manuals.

b This manual contains detailed theory of operation of all chassis which make up the acquisition radar system (less HIPAR). It also contains information on cabinet-mounted components that are not part of chassis. In addition, this manual contains a mechanical description of the acquisition antenna-receiver-transmitter group. Functional theory, which shows the functional relationships between chassis, is held to a minimum. It is covered only where necessary to adequately explain a circuit. For functional theory, refer to TM 9-1430-250-20/1.

c. Multiple-use chassis are discussed where first encountered in this manual and cross-referenced thereafter.

d. The appendix contains a list of current references, including supply manuals, technical manuals, and other available publications applicable to the NIKE-HERCULES and Improved NIKE-HERCULES Systems.

e. Any errors or omissions will be brought to the attention of the Commander, U. S. Army Ordnance Missile Command, Army Rocket and Guided Missile Agency, Redstone Arsenal, Ala., ATTN: ORDXR-FMPT, using DA Form 468 (Unsatisfactory Equipment Report).

2 (U). Related Publications

This manual is one of a series of manuals covering field and depot maintenance of the NIKE-HERCULES and Improved NIKE-HERCULES Systems Items of the NIKE-HERCULES Air Defense Guided Missile System are shown in Appendix I of TM 9–1400–250–10/1. Items of the Improved NIKE-HERCULES Air Defense Guided Missile System are shown in Appendix I of TM 9–1400–250–10/2. A list of the technical manuals covering these items is included in each appendix.

3 (U). Arrangement of Material

This manual is divided into eight chapters, with a chapter devoted to each major assembly or console in the acquisition radar system (less HIPAR). Each chapter contains a paragraph to cover detailed theory of operation of each chassis located within the major assembly or console. Where applicable, a paragraph is included in each chapter to cover nonchassis electrical components that are mounted on the major assembly or console, and to cover a mechanical description of certain mechanisms.

4 (U). Technical Manual Effectivity

a. This manual is technically correct up to and including NIKE-HERCULES System serial number 1370, provided Department of the Army Modification Work Orders (DA MWO's) listed in table I have been incorporated in these systems. Table I also contains a brief description of each DA MWO. This manual is also technically correct up to and including system suffix serial No. 075 of the Improved NIKE-HERCULES System.

b. For a complete listing of all DA MWO's that affect this equipment, refer to DA Pam 310-4.

Table I (U). MWO Changes

MWO No.	Description	MWO No.	Description
Y25-W1	Redesigns front end plate of the magnetic circuit to improve adjustment, using existing instructions. System serial nos. 1001 through 1028 are affected.	Y28-W23	Reduces 6901 tube failures, improves diodes, and increases stability. Systems 1001 through 1266 are affected.
Y25-W3	Adds capacitor C45 to the acquisition AFC to eliminate noise pickup. System serial nos. 1001 through 1246 are affected.	Y28-W24	Provides calibration voltage for PPI adjustment and provides a means of adjustment +250 or +160 volt regulator. Systems 1001 through 1218 are affected.
Y25-W4	Prevents destruction of timing relays in the electro-mechnical control box. System serial nos. 1071 through 1306 are affected.	Y28-W29	Adds a video clamper to PPI. Systems 1001 through 1306 are affected.
Y28-W2	Changes resistor R3 on the delay amplifier to 56 ohms to enable amplifier in the moving target indicator (MTI) circuit to operate with Ord 7 delay lines. System serial nos. 1001 through 1006 are affected.	Y28-W30	Corrects wiring in the FUIF interconnecting box and cover. Systems 1001 through 1183 are affected.
		Y28-W32	Modifies the acquisition-track synchronizer to prevent loss of sync pulses. System 1001 through 1266 are affected.
Y28-W5	Adds selective indentification facilities and incorporates Mark XI Identification Friend or Foe (IFF) equipment; also adds trigger pulse generator. System serial nos. 1001 through 1090 are affected.	Y28-W35 and Y39-W23	Adds facilities to permit use of radar signal simulator (selected systems).
		Y28-W37	Converts electronic gate to plug-in unit to improve assembly and maintenance.
Y28-W7	Adds shielded wires, a corona shield, and a new tube socket to eliminate high voltage arc-over in the PPI and prevents loss of gates due to transients. System serial nos. 1001 through 1070 are affected.	Y28-W44	Eliminates cross-talk and resultant degradation of system MTI. Also eliminates mechanical interference between door and cover plate on the director station group.
Y28-W9	Interchanges two wires so that fuse circuits will function to agree with engraving on the fuse and control panel in the recorder and switchboard cabinet. System serial nos. 1001 through 1031 are affected	9-1400-261-30	Converts a NIKE-HERCULES System to an Improved NIKE-HERCULES System (selected systems).
		9-1430-251-30/8	Adds radar bomb scoring facilities (selected systems).
Y28-W11	Adds suppression circuits to the acquisition radar system to reduce interfering signals and noise. System serial nos. 1001 through 1246 are affected.	9-1400-291-30	Adds HIPAR AJD capabilities to Improved NIKE-HERCULES systems. System suffix serial nos. 001 through 028 are affected.
Y28-W21	Modifies sweep and symbol circuits, range unit, and PPI marker generator for extended range on PPI in director station group. System serial nos. 1001 through 1048 are affected.	9-1430-254-30/1/1	Prevents acquisition primary actuator motor from coasting. Systems 1307 through 1362 are affected.
		9-1430-263-30	Adapts the radar course directing central (RCDC) to accept auxiliary acquisition radar (selected systems).

Table I (U). MWO Changes—Continued

MWO No.	Description
9-1400-268-50	Provides antijam display (AJD) capability to NIKE-HERCULES Acquisition Radar system. May be installed with or without AAR. (Selected systems.)
9 1430 251-30/14	Minimizes 400-cps beat frequency interference between Auxiliary Acquisition Radar or HIPAR and Improved NIKE-HERCULES system. (INH suffix serial numbers 001 through 074.)
9-1430-251-30/11	Modifies feedback circuit in control-indicator so acquisition range rate may be factory adjusted to desired limits. (Systems HERCULES 1001 through 1362; INH, All.)

5 (U). Nomenclature

Table II contains an alphabetical listing of technical manual (TM) nomenclature used in this manual with a cross-reference to official nomenclature. It should be noted that items having identical TM and official nomenclature have not been included in the table.

Table II (U). Nomenclature Cross-Reference

TM nomenclature	Official nomenclature
4-kc oscillator	Audio frequency oscillator
5-minute delay timer ...	Interval timer
15-minute delay timer	Interval timer TD-115/M
20-30-second delay timer	Interval timer TD-114/M
−28v power supply	Power supply
+250 or +150 volt regulator.	Voltage regulator
−250, +250, or +150 volt regulator.	Voltage regulator CN-281 M

Table II (U) Nomenclature Cross-Reference—Continued

TM nomenclature	Official nomenclature
+270v, −28v, and +75v or +175v power supply	Power supply PP-1161A/M
+320v or +220v power supply.	Power supply PP-1160B/M
−1000v power supply	Power supply
Acquisition 5-minute delay timer.	Interval timer
Acquisition AFC	Receiver control
Acquisition antenna ...	Antenna AT-779/T
Acquisition antenna	Antenna AS-980/T
Acquisition antenna drive	Antenna drive
Acquisition antenna pedestal.	Antenna pedestal AB-545/T
Acquisition antenna pedestal.	Antenna pedestal AB-544/T
Acquisition control-indicator.	Control-indicator
Acquisition control-indicator.	Control-indicator (acquisition and IFF).
Acquisition duplexer	Duplexer
Acquisition HV power supply.	Power supply
Acquisition IF amplifier.	Intermediate frequency amplifier AM-1062/MS.
Acquisition IF preamplifier.	Intermediate frequency amplifier AM-1059/MS.
Acquisition modulator.	Radar modulator MD-311/T
Acquisition orientation level.	Surveying level TS-844/MS
Acquisition power control panel	Power distribution panel
Acquisition range generator.	Pulse generator
Acquisition range generator.	Pulse-sweep generator
Acquisition receiver-transmitter.	Radar receiver-transmitter RT-430/T.

Table II (U). Nomenclature Cross-Reference—Continued

TM nomenclature	Official nomenclature	TM nomenclature	Official nomenclature
Acquisition RF power supply control.	Power supply control	HIPAR control-indicator.	Control-indicator
Acquisition slip ring __	Slip ring	HIPAR resolver amplifier.	Electronic control amplifier
Acquisition trigger amplifier.	Trigger amplifier	Hydraulic control relay assembly.	Relay assembly
Acquisition-track synchronizer.	Electrical synchronizer	IFF control-indicator _	Control-indicator
Auxiliary acquisition coaxial relay assembly.	Relay assembly	Interference suppressor pulse amplifier-generator.	Amplifier-generator
Auxiliary acquisition control interconnecting group.	Control interconnecting group.	LOPAR auxiliary control-indicator.	Control-indicator
Auxiliary acquisition control interconnecting box.	Interconnecting box	LOPAR control-indicator.	Control-indicator
Auxiliary acquisition interconnecting box.	Interconnecting box	LOPAR relay assembly	Low power acquisition radar relay assembly.
Auxiliary acquisition interconnecting box cover.	Interconnecting box cover.	Low-power servo amplifier.	Electronic control amplifier AM-1056/M.
Auxiliary acquisition relay assembly.	Relay assembly	Mark generator _____	Pulse generator
Azimuth sweep generator mixer stage.	Sweep control mixer stage CV-318/M.	Modulator control-indicator.	Control-indicator
Battery control console.	Battery control console OA-1481/MSA-19.	Modulator control-indicator.	Control-indicator (modulator).
Battery control console.	Guided missile battery control console.	MTI delay line __ ___	Delay line
Battery control interconnecting box.	Interconnecting box J-850/MSA-19.	MTI delay line _____	Delay line (ultrasonic)
Battery control interconnecting box housing.	Junction box housing	MTI oscilloscope _____	Oscilloscope
		MTI synchronizer ____	Electrical synchronizer
		MTI video amplifier __	Video amplifier
Carrier oscillator ____	Radio frequency oscillator	PPI _____	Azimuth and range indicator.
Compressor _____	Motor driven reciprocating compressor.	PPI dc amplifier ____	Direct current amplifier
Delay amplifier _ ____	Intermediate frequency amplifier.	PPI HV power supply_	Power supply
		PPI marker generator.	Electronic marker generator
Director station group.	Guided missile director station group.	PPI test panel _____	Electrical test panel
Director station group.	Director station group OA-1480/MSA-19.	PPI video amplifier __	Video amplifier
		Precision indicator ___	Azimuth and range indicator
Electro-mechanical control box.	Control box	Precision mark generator.	Pulse generator
Electro-mechanical control panel.	Control panel	Precision video amplifier.	Video amplifier AM-1076/M
Equipment cooling fan	Centrifugal fan HD-167/M	Primary actuator ____	Electro-mechanical actuator
Equipment cooling cabinet.	Electrical equipment cabinet	Primary actuator ____	Electro-mechanical actuator (primary).
FUIF fixed attenuator	Fixed attenuator	Primary hydraulic cylinder.	Antenna reflector hydraulic cylinder.
FUIF interconnecting box.	Interconnecting box J-851/MSA-19.	Range sweep generator	Sweep generator O-294A/M
FUIF interconnecting box cover.	Interconnecting box cover CW-439/MSA-19.	Range sweep generator	Sweep generator
		Remote control circuit	Guided missile remote control circuit MX-2631/MS.
FUIF relay assembly _	Relay assembly	Resolver amplifier ____	Electronic control amplifier AM-1057/MS.
HIPAR auxiliary control-indicator.	Control-indicator	Resolver-video amplifier.	Electronic control amplifier
		Rotary coupler _____	Radio frequency rotary coupler.
		Secondary actuator ___	Electro-mechanical actuator

Table II (U). Nomenclature Cross-Reference—
Continued

TM nomenclature	Official nomenclature
Secondary actuator	Electro-mechanical actuator (secondary).
Secondary hydraulic cylinder.	Antenna reflector hydraulic cylinder.
STC	Receiver control
Target designate control-indicator.	Control-indicator
Trigger pulse amplifier.	Generator amplifier
Video and mark mixer.	Video signal mixer
Video and mark mixer.	Video mixer

6 (U). Forms, Records, and Reports

a. General. Responsibility for the proper execution of forms, records, and reports rests upon the commanding officers of all units maintaining this equipment. However, the value of accurate records must be fully appreciated by all persons responsible for their compilation, maintenance, and use. Records, reports, and authorized forms are normally utilized to indicate the type, quantity, and condition of the materiel to be inspected, to be repaired, or to be used in repair. Properly executed forms convey authorization and serve as records for repair or replacement of materiel in the hands of troops and for delivery of materiel requiring further repair to ordnance shops in arsenals, depots, etc. The forms, records, and reports establish the work required, the progress of work within the shops, and the status of materiel upon completion of its repair.

b. Authorized Forms. The forms generally applicable to units operating this materiel are listed in the appendix. For a listing of blank forms, refer to DA Pam 310-2. For instructions on use of these forms, refer to FM 9-3 and FM 9-4.

c. Field Report of Accidents. The reports necessary to comply with the requirements of the Army safety program are prescribed in detail in AR 385-40. These reports are required whenever accidents involving injury to personnel or damage to materiel occur.

d. Report of Unsatisfactory Equipment or Materials. Any deficiencies detected in the equipment covered herein, which occur under the circumstances indicated in AR 700-38, should be immediately reported in accordance with the applicable instructions in cited regulation.

e. Report of Errors or Omissions. Any errors or omissions will be brought to the attention of the Commander, Army Rocket and Guided Missile Agency, U. S. Army Ordnance Missile Command, Redstone Arsenal, Alabama, ATTENTION: ORDXR-FMPT, using DA Form 2028.

f. Report of Failure or Replacement of Parts. In order to comply with the requirement in AR 700-37, report every part that fails, or is replaced, on DA Form 9-110, Guided Missile Component Evaluation Data Report, and forward the form in accordance with its instructions.

7 (U). Illustrations

Schematic illustrations of the equipment covered by this manual are contained in TM 9-1430-257-20/1. Simplified schematics and block diagrams illustrate complex circuits or show relationships between unit chassis. Photographs and line drawings show special details that cannot be adequately explained by text or by schematic representation.

8 (U). Waveforms

Waveforms are included on the block diagrams and simplified schematic diagrams contained in this manual. These waveforms are ideal and may differ from actual observed waveforms which are taken on the equipment and which appear on the schematic diagrams of TM 9-1430-257-20/1. The theoretical amplitude and duration of these ideal waveforms, expressed in text, may also differ from those shown on the schematic.

9 (U). Differences Among Models

a. General. There are differences among models that exist because of production changes not covered by MWO's. This manual provides coverage of these differences, at chassis level, in the appropriate paragraph of the text.

b. Methods of Coverage.

(1) Differences among models are covered by four methods. If the differences among models of a chassis are extensive, the earlier (or oldest) model is covered first, followed by a paragraph about the later model. For identification purposes, the title of each paragraph contains the ordnance part number of the chassis.

(2) Where the differences among models of a chassis are less extensive, both models are covered in the same paragraph. The earlier model is covered in detail. All chassis

ordnance part numbers are used in the title of the paragraph to identify the chassis under discussion. A subparagraph is then provided to explain how the later model differs from the earlier model. The ordnance part number of the later model is included in the subparagraph title.

(3) In instances when differences among models can be explained in a few sentences, the earlier chassis is discussed and the later chassis differences given at appropriate points in the discussion. All ordnance part numbers are given in the paragraph heading.

(4) Where differences among models exist but there has been no change in ordnance number, the chassis is explained as it was prior to the change. Then a subparagraph entitled Differences among models is included to explain the differences.

CHAPTER 2

DIRECTOR STATION GROUP

10. Acquisition IF Amplifier 7621810

a. General. The acquisition IF amplifier increases the signal level of the echo signals and provides protection against certain types of pulse jamming and all continuous wave jamming.

b. Detailed Theory.

(1) The 60-megacycle IF signals are coupled through connector J1 and capacitor C1 (fig. 37, TM 9-1430-257-20) to impedance-matching transformer T1. This double-tuned transformer is used for interstage coupling. It resonates with the circuit capacitance at 60 megacycles. The desired 4-megacycle bandpass is obtained by over-coupling the primary and secondary windings, and loading the secondary windings with resistor R1. Over-coupling produces a steep sided bandpass curve. Resistor R1 lowers the "Q" of the secondary circuit and thus produces the bandpass for the desired frequencies. The windings of T1 are factory set for the desired output by physically positioning the windings; they cannot be readjusted in the field.

(2) The 60-megacycle IF signals at the control grid of IF amplifier V1 are amplified by V1 and applied across the primary of transformer T2. Resistor R3 across the primary of T2 performs the same function as R1 across the secondary of T1, and T2 the same function as T1. The plate, grids, and filament of V1 are de coupled from the power supplies by resistive-capacitive and inductive-capacitive networks. Capacitors C2, C7, C14, C19, C26, C31, C10A, C22A, C34A, C41A, and C49, and resistors R4, R11, R12, R19, R27, R28, R35, R43, R44, R52, and R60 are decoupling networks for the control grids of V1 through V6. Capacitors C4, C9, C16, C21, C28, C33, C10B, C22B, C34B, C41B, and C50, and resistors R5, R13, R21, R29, R37, R45, R54, and R58 are decoupling networks for the screen grids and plates of V1 through V6. Inductors L4 through L11 and capacitors C53 through C61 are decoupling networks for the filaments of V1 through V8. The decoupling networks prevent V1 through V8 from breaking into continuous wave oscillations which would otherwise occur in interstage coupling.

(3) Since medium-gain, low-noise, voltage amplifiers V1 through V6 are identical, the same detailed theory outlined for V1 applies for the remaining five stages. Protection from jamming is accomplished by providing IF amplifiers V1 through V6 with a back-bias facility, which causes the stage bias to increase during the time that jamming signals are received. Each of the first six stages contains a 12,000-ohm cathode resistor bypassed by a 500-micromicrofarad capacitor. When pulse jamming signals longer than 6 microseconds or continuous wave jamming signals are received, the bypass capacitor accumulates sufficient charge to shift the operating point of the tube toward cutoff. This results in decreased amplification of the jamming signal. Since this attenuation is additive through six stages, the jamming signal is greatly minimized. Target video signals receive near normal amplification, however, since they are effectively superimposed on the jamming signal and fall in the linear portion of the tube characteristic curve.

(4) The output signal from IF amplifier V6 is coupled through transformer T7 to high-gain IF power amplifier V7. This stage contains a power pentode tube using a low value of cathode resistance. It provides sufficient power to drive bypass MTI video detector V8A and bypass video detector V8B. The 60 + 4-megacycle IF signal from V7 is coupled through transformer T8 to the plate of V8A and the cathode of V8B. Detectors V8A and V8B conduct on opposite cycles of the input signal and charge capacitors C45, C47, and C48 in their respective filter networks. Between cycles, these capacitors discharge through inductors L1 and L2 which present a high impedance to 60 megacycles. In this manner the capacitors maintain a polarized charge for approximately 1.3 microseconds and then discharge rapidly between pulses. This action provides a negative bypass video output and a positive MTI video output to the MTI system

10.1 (U). Main Acquisition IF Amplifier 9990755

a. General. The main acquisition IF amplifier increases the signal level of the echo signals and eliminates or reduces the effects of strong transmission jamming signals.

b. Detailed Theory.

(1) The 60-megacycle IF signals are coupled through connector J1, developed across resistor R6, and coupled through resistor R7 and capacitor C1 (fig. 37.1, TM 9-1430-257-20) to impedance-matching transformer T1 which is tuned to resonate at the intermediate frequency. The desired bandpass is obtained by overcoupling the windings, to produce a steep-sided bandpass curve, and by loading the secondary with resistor R1 to lower the "Q" of the circuit. The windings of T1 are factory adjusted for the desired output and cannot be readjusted in the field.

(2) The 60-megacycle IF signals at the T1 secondary are applied to the control grid of amplifier V1 where they are amplified and applied across the primary of transformer T2. The functions of resistor R3 and of T2 are the same as of R1 and T1. Capacitors C2, C7, C14, C19, C26, C42, C43, C44, C51, and C38, and resistors R4, R11, R12, R19, R27, R28, R35, R44, R52, and R60 are decoupling networks for the control grids of V1 through V5. Capacitors C4, C9, C16, C21, C28, C10A, C10B, C22A, C22B, C31, C34A, and C34B, and resistors R5, R13, R14, R20, R21, R29, R30, R36, R37, R38, and R43 are decoupling networks for the screen grids and plates of V1 through V5. Inductors L4 through L10 and capacitors C53 through C60 are decoupling networks for the filaments of V1 through V7. The decoupling networks prevent the tube stages from breaking into continuous wave oscillations.

(3) Since medium-gain, low-noise, voltage amplifiers V1 through V5 are identical, the same detailed theory outlined for V1 applies for stages V2 through V5. Protection from jamming is accomplished by providing IF amplifiers V1 through V5 with a back-bias facility, which causes the stage bias to increase during the time that jamming signals are received. Each of the first five stages contain a 12,000 ohm cathode resistor bypassed by a 500-micromicrofarad capacitor. When pulse jamming signals longer than 6 microseconds or when continuous wave jamming signals are received, the bypass capacitor accumulates sufficient charge to shift the operating point of the tube toward cutoff. This action results in decreased amplification of the jamming signal. Since this attenuation is additive through five stages, the jamming signal is greatly minimized. Target video signals receive near normal amplification, however, since they are effectively superimposed on the jamming signal and fall in the linear portion of the tube characteristic curve.

(4) The output signal from IF amplifier V5 is coupled through transformer T6 to IF amplifier V6. This is a low noise high-gain amplifier stage. It provides isolation between high-gain IF power amplifier V7 and IF amplifier stages V1 through V5. The operation of this stage is similar to the operation of stages V1 through V5. The cathode is bypassed by C32. Capacitor C61 and resistor R39 decouple the −250-volt power supply. Capacitor C33 is the screen grid and plate bypass capacitor. Resistors R45, R54, R58, and R53, and capacitors C41A, C41B, and C49 are decoupling networks for the screen grids and plates of V6 and V7.

(5) The output of IF amplifier V6 is coupled through transformer T7 to high-gain power amplifier V7. This stage contains a power pentode tube using a low-value cathode resistor. The IF signal is coupled through transformer T8 to semiconductor diode detectors CR1 and CR2 which conduct on opposite half-cycles of the input signal charge capacitors C47, C48, C45, and C46 in their respective filter networks. Between charges, these capacitors discharge through inductors L1 and L2. The 60-megacycle IF is blocked by the high impedances of L1 and L2, but is shunted to ground through the low impedances of C47 and C45. The pulse developed across resistor R56 when C45 and C46 discharge is coupled through resistor R55 to the noise measuring circuit.

(6) Video signals detected by CR2 are developed across resistor R57 and coupled to the grid of amplifier V8, from which two outputs are obtained. A positive video is developed across cathode resistor R61 and applied through connector P2-10 to the MTI circuits. A negative bypass video is developed across the plate load resistor which is located in the fast AGC amplifier (fig. 26.2, TM 9-1430-257-20).

11 (U). Carrier Oscillator 8513287

a. *General.* The carrier oscillator generates a 15-megacycle carrier suitable for modulation by combined test, MTI video, and preknock pulses. It establishes the delay video and non-delay video channel for the above pulses.

b. *Detailed Theory.*

(1) To accurately reproduce the MTI video pulses, a crystal transducer located in the MTI delay line must be excited by a 15-megacycle carrier modulated by the MTI video pulses. This carrier frequency is generated by oscillator V3 (fig. 35, TM 9-1430-257-20). The LC network, consisting of inductor L3, oscillator frequency variable capacitor C16, and capacitor C20, is a Hartley-tuned tank and is tuned to 15 megacycles. Adjustment of C16 is made using battery type 4 test equipment. The output from the tank is coupled through capacitor C12, developed across resistor R18, then applied to the control grid of V3. Resistor R17 is the dropping resistor for the plate of V3, and capacitor C11 decouples the plate and screen grid from the power supply. The output from V3 is coupled through capacitor C7 to the junction of resistors R12, R13, and the control grid of modulator V1.

(2) A 6-volt, 7-microsecond test pulse is applied through connector J2 and isolating resistor R6 to the junction of resistors R7 and R8. Capacitor C2 bypasses transient voltages to ground. Also, a video pulse is applied through connector P1-9 to MOD ADJ variable resistor R1. The positioning of R1 determines the percentage of video modulation on the carrier; an amplitude of video equal to the amplitude of the test pulse (100 percent modulation) is desirable. The adjusted video is applied through isolating resistor R5 to the junction of R7 and R8. The combined video and test pulses are developed across R7 and applied through R8 to the suppressor grid of modulator V1. These pulses modulate the 15-megacycle carrier in V1 and are applied from the plate through

coupling capacitor C6 to amplifier V2, until V1 is cut off by a preknock pulse.

(3) The preknock pulse enters the unit at connector J1 and is inverted in transformer T1 to give a negative pulse at the suppressor grid of V1. At J1 the preknock pulse is positive and has a 40-volt amplitude and a 1-microsecond duration. An inverted facsimile of this pulse is applied from terminal 4 of T1 through resistors R2 and R3 of the T filter, composed of R2, R3, and capacitor C1, to the cathode of isolating diode CR1. The forward resistance of CR1 is negligible and passes the negative preknock pulse which is then developed across R7 and applied through R8 to V1. At the suppressor grid, the preknock pulse is large enough to cut V1 off for the duration of the pulse, thereby blocking the 15-megacycle car-

rier and producing a positive output pulse from V1.

(4) The operating point for the suppressor grid of V1 is set by means of LEVEL ADJ. variable resistor R22. This point is determined by the voltage divider consisting of resistors R22, R9, R8, and R7. Since the divider is inserted between −250 volts and ground, it applies between −2.3 and −4.4 volts bias at the suppressor grid of V1. This dc level controls the amplitude of the carrier and is isolated from T1 by the high back resistance of CR1. When no preknock pulse is applied, the T filter network consisting of R2, R3, and C1 completes the circuit for the secondary of T1 and bypasses any spurious line noises that may be present in the input of T1. During application of the preknock pulse, the T filter network prevents overshooting and ringing from entering the input network of V1.

(5) The test pulse and the preknock pulse appear with the MTI video pulse as part of the 15-megacycle RF modulation on the plate of V1. Resistor R10 is a parasitic suppressor, and C3 and C4 are bypass capacitors. The screen voltage is dropped by resistor R4 and maintained at a fixed potential by capacitor C5. The modulated-carrier output is of low amplitude, due to the low value of plate load resistor R11. Carrier shift can occur due to the instability of oscillator V3. However, the effect is negligible since the external MTI delay line has a broad bandpass. The modulated 15-megacycle carrier is applied through capacitor C6 to V2.

(6) The composite signal is developed across inductor L1 which is broadly tuned to avoid loss of video due to the carrier shift. Cathode resistor R15 is bypassed by capacitor C8; the remainder of V2 stage components are similar to counterparts in modulator V1. The output from V2 is coupled through capacitor C9 to delay amplifier V4, the components of which

are similar to those of V2 with the exception of plate load resistor R23 and delay video bandwidth variable inductor L4. Resistor R23 across L4 broadens the bandwidth. Resistors R19 and R20 are parasitic suppressors. Capacitors C14, C15, C17, and C18 are decoupling capacitors which keep the RF from the power supply. The modulated carrier output from V4 is coupled through capacitor C21 to connector P2 and to the input network of nondelay amplifier V5. Delay video bandwidth variable inductor L5, together with resistors R24 and R25, form a broad bandwidth network at the input of V5. The network also maintains broad bandwidth in the circuits connecting the output of V4 with the external MTI delay line.

(7) Only a small value of the composite signal is developed across resistor R25 and applied to the grid of V5. Resistor R24 limits grid current which reduces the loading effect on V4. The composite signal is inverted in V5 and reinverted in transformer T2. Resistor R27 across the primary winding of T2 broadens the bandwidth. The 15-megacycle component is removed from the composite signal in the full-wave rectifier composed of transformer T2, diodes CR2 and CR3, and capacitor C27 and nondelay video bandwidth variable capacitor C35. Capacitor C26 equalizes the potential between the cathodes of CR2 and CR3 with respect to the center tap of T2. The diodes conduct on alternate RF cycles; the current path is through C27 and C35, ground, and the center tap of T2 to the cathode of the respective diode. These alternate paths filter out the 15-megacycle carrier and offer a high impedance to the short duration test, MTI video, and preknock pulses. These pulses encounter a low impedance at the load connected through connector J3.

(8) Nondelay amplifier V5 has a bandwidth

equal to the 2-megacycle bandwidth of the external crystal transducer in the MTI delay line. Capacitor C35 is adjusted to maintain this bandwidth in the circuits connecting the output of V5 to the input impedance of the external MTI synchronizer. Connector J4 is a test point for external monitoring and R29 is a dropping resistor used to protect the external carrier level meter located on the MTI oscilloscope connected at P1-1 and 7. The nondelay output at J3 is a complex waveform containing a positive preknock pulse, negative test pulse, and MTI video pulses referenced at −4 volts dc. Because the negative, 7-microsecond test pulse is longer than the preknock or MTI video pulses, an average dc value (−4 volts) is created by the full-wave rectifier conduction during the time the test pulse is applied. Therefore, the output waveform at J3 is referenced at −4 volts dc.

11.1 (U). Delay Line Driver 9990570

a. *General.* The delay line driver generates a 15-megacycle carrier suitable for modulation by combined test, MTI video, and preknock pulses during MTI or interference suppressor (IS) operation. During video processor operation, the delay line driver has two separate inputs, pre-MTI video and processor feedback, and two corresponding outputs. During MTI or IS operation the delay line driver uses a single input and provides two outputs. In either case, one output is non-delayed video and the other is an amplitude modulated 15-megacycle carrier used to drive the external delay line.

b. *Detailed Theory.*

(1) To accurately reproduce the MTI video pulses or the processor feedback video, a crystal transducer located in the MTI delay line must be excited by a 15-megacycle carrier modulated by the MTI video or the processor feedback video. This carrier frequency is generated by oscillator V3 (fig. 35.1, TM 9-1430-257-20). The LC network, consisting of inductor L3, oscillator frequency variable capacitor C16, and capacitor C17, is a Hartley-tuned tank and is tuned to 15-megacycles. Adjustment of C16 is made using battery type 4 test equipment. The output from the tank is coupled through capacitor C32, developed across resistor R30, then applied to the control grid of V3. Resistor R29 is the plate dropping resistor and capacitor C15 decouples the plate and screen grid from the power supply. The output from V3 is coupled through capacitors C13 and C14 to the control grids of modulators V1 and V7.

(2) The delay line driver is divided into two channels. Channel 1 is composed of V6B, V7, and V8. Channel 2 is composed of V6A, V1, V2, and V4. V5 is common to both channels. A 6-volt, 7-microsecond test pulse is applied through connector J2 and isolating resistor R24 to CR7 and to capacitor C45, which bypasses transient voltages to ground. A video pulse is applied through connector P1-9 to MOD ADJ variable resistor R1, which controls the percentage of carrier modulation, and which is adjusted for a desired video output from cathode follower V6B equal in amplitude to the test pulse (100-percent modulation). The video pulse is applied from the brush arm of R1 to the diode gate switch consisting of CR1 through CR4. A 23-microsecond gate pulse is applied through connectors P1-10 and P1-12 which opens the diode gate switch during the preknock to sync period, effectively removing all signal and noise from the input and permitting the test pulse to be inserted during a noise free period to enable the MTI AGC to function properly. The test pulse is inserted simultaneously in both channels so that the MTI AGC functions properly in the video processor mode as well as the MTI mode. At the expiration of the video gate pulse, video is applied through the now closed diode gate switch and is developed across resistor R4. Diode CR5 shunts the negative portions of the

video to ground so that only positive video is applied to the grid of cathode follower V6A.

(3) The positive output from cathode follower V6A is developed across resistor R45, coupled through resistors R46 and R48 to the suppressor grid of modulator V1. The positive preknock pulse, applied through connector J1 is inverted in transformer T1 and applied from terminal 4 of T1 through resistors R22 and R23 of the T filter, composed of R22, R23, and C12, to the cathode of isolating diode CR7 The forward resistance of CR7 is negligible and passes the negative preknock pulse which is then developed across R47 and applied through R48 to the suppressor grid of V1. At the suppressor grid, the preknock pulse is large enough to cut off V1 for the duration of the pulse, thereby blocking the 15-megacycle carrier and producing a positive output pulse from V1.

(4) The operating point for the V1 suppressor grid is set by means of CHAN 2 CARRIER LEVEL ADJ variable resistor R25, which varies the grid bias between −2.3 and −4.4 volts, thereby controlling the carrier amplitude. R25 is part of a voltage divider, consisting also of R26, R47, and R48 which is connected between −250 volts and ground, and which is isolated from T1 by the high back resistance of CR7. When no preknock pulse is applied, the T filter network consisting of R22, R23, and C12 completes the circuit for the secondary of T1 and bypasses any spurious line noises that may be present in the input of T1. During application of the preknock pulse, the T filter network prevents overshooting and ringing from entering the input network of V1.

(5) The test pulse and the preknock pulse appear with the MTI video pulse as part of the 15-megacycle RF modulation on the plate of V1 Resistor R50 is a parasitic suppressor, and C25 and C24 are bypass capacitors. The screen voltage is dropped by resistor R49 and maintained at a fixed potential by capacitor C24. The modulated carrier output is of low amplitude, due to the low value of plate load resistor R51. The modulated 15-megacycle carrier is applied through capacitor C26 to the control grid of amplifier V2.

(6) The composite signal is developed across inductor L1 which is broadly tuned to avoid loss of video due to the carrier shift. Cathode resistor R55 is bypassed by capacitor C27: the remainder of V2 stage components are similar to counterparts in V1. The output from V2 is coupled through capacitor C29 to amplifier V4, the components of which are similar to those of V2 with the exception of plate load resistor R58 and inductor L4. Resistor R58 across L4 broadens the bandwidth. Resistor R56 is a parasitic suppressor. Capacitor C30 is a decoupling capacitor which keeps RF from the power supply The modulated carrier output from V4 is coupled through capacitor C33 to connector P2 and to the input network of amplifier V5. Variable inductor L5, together with resistors R60 and R61, form a broad bandwidth network at the input of V5.

(7) The input network to the grid of V5 is composed of switching diodes CR8 and CR9 and inductor L9. Switching diodes CR8 and CR9 are switched by contacts 1, 2, and 6 of relay K1. When K1 is deenergized, −118 volts is applied from the voltage divider composed of resistors R31 and R32 between −250 volts and ground through contacts 1 and 6 of K1, inductor L12 and resistor R36 to the cathode of CR9. The −118 volts is also applied through resistor R35 to the anode of CR8. This action causes CR9 to conduct and it appears as a short circuit. At the same time CR8 is back biased and appears as an open circuit to the signals from V8.

(8) Only a small value of the composite signal is developed across resistor R61 and applied through capacitor

C34 to the grid of V5. The composite signal is inverted in V5 and reinverted in transformer T2. Resistor R39 across the primary of T2 broadens the bandwidth. The 15-megacycle component is removed from the composite signal in the bi-phase half-wave rectifier composed of transformer T2, diodes CR16 and CR17, and capacitor C22. Capacitor C21 equalizes the potential between the cathodes of CR16 and CR17 with respect to the center tap of T2. The diodes conduct on alternate RF cycles; the current path is through C22, ground, and the center tap of T2 to the cathode of the respective diode. The alternate paths filter out the 15-megacycle carrier and offer a high impedance to the short duration test, MTI video, and preknock pulses. These pulses encounter a low impedance at the load connected at J3. Resistor R40 is a dropping resistor used to protect the external meter connected through connector P1-7. The output at J3 is a complex waveform containing a positive preknock pulse, negative test pulse, and MTI video pulses referenced at —4 volts dc. Because the negative, 7-microsecond test pulse is longer than the preknock or MTI video pulses, an average dc value (4 volts) is created in the rectifier composed of diodes, CR16 and CR17, during the time the test pulse is applied.

(9) When K1 is energized, the input to V6A is switched from pre-MTI video to processor feedback video through contacts 3 and 5. At the same time the bias voltage on switching diodes CR8 and CR9 is reversed through contacts 2 and 6 of K1. CR9 acts as an open circuit and CR8 acts as a short circuit. The delay line driver will now function as a dual channel amplifier with processor feedback video through channel 2 and pre-MTI video through channel 1.

(10) The operation of channel 1 is essentially the same as that of channel 2 discussed in (1) through (8) above

except that there is one stage of amplification (V4) in channel 2 which has no counterpart in channel 1.

12 (U). MTI Delay Line 8519066

a. *General.* The purpose of the MTI delay line is to provide the delay necessary for MTI operation. It converts a composite electrical signal to ultrasonic vibrations by means of a piezo-electric quartz crystal transducer. The ultrasonic vibrations are delayed one pulse repetition period by a 14-sided fused quartz disk. They are then restored to their original form by another crystal transducer. By delaying the pulses one repetition period, the MTI delay line establishes the repetition rate of the MTI system.

b. *Detailed Theory.*

(1) The MTI delay line (fig. 3) is a 14-sided polygonal disk approximately 12-1/2 inches in diameter and 1-1 4 inches thick. Each of the 14 sides is a smoothly polished quartz facet These facets are arranged to reflect the ultrasonic vibrations in paths parallel to the plane of the disk. Connections to and from the delay line are shown in B27 and B30, figure 25, TM 9-1430-257-20.

(2) A 15-megacycle modulated carrier is applied through INPUT connector J1 (fig. 3) and converted to ultrasonic vibrations by the input crystal transducer. The speed of these vibrations propagated through striction of the 14-sided fused quartz disk is much slower than the speed of electromagnetic waves traveling through a common conductor. The vibrations travel parallel to the plane of the disk to the opposite facet. Then, by successive reflections, the waves touch each facet of the disk and return to the output crystal transducer where the ultrasonic vibrations are reconverted to the original electrical composite signal. The path of travel is of sufficient length to provide a delay equal to a repetition period of the preknock pulse, or approximately 2,000 microseconds. The delay modulated 15-megacycle carrier output is applied

through OUTPUT connector J2 to an external delay amplifier.

13 (U). Delay Amplifier 8512849, 9007731

a. General. The delay amplifier raises the output level of the delay video channel to equal the output level of the nondelay video channel. These outputs are 180° out of phase with each other.

b. Detailed Theory.

(1) A 15-megacycle modulated carrier from the MTI delay line is applied through connector P2 (fig. 41, TM 9-1430-257-20) to the delay amplifier. The signal is developed across imped-ance matching resistor R3 which is the termination for the low impedance coaxial input cable. In delay amplifier 8512849 (systems 1001-1006), resistor R3 has a value of 150 ohms. In delay amplifier 9007731 (systems 1007-1059), the value of R3 has been reduced to 56 ohms in order to decrease the input sensitivity of voltage amplifier V1 with respect to AGC voltage. The input signal is coupled through capacitor C4 to the control grid of V1. Also, a negative AGC voltage from the MTI video amplifier is applied through connector P1 to the input circuit of V1.

Resistor R4 limits current and isolates the 15-megacycle modulated carrier from the AGC source. The negative AGC voltage is essentially a dc value that charges capacitor C5. This voltage is applied to V1 through inductor L2 to maintain the delay amplifier output at the same dc level but opposite in polarity as the nondelay video channel level.

(2) Voltage amplifier V1 is a tuned-grid, tuned-plate stage, and V2 is a tuned-plate amplifier. Inductors L2, L6, and L7 reso nate with the distributed circuit capacity at 15 megacycles to produce optimum output at that frequency. Resistors R1, R2, R6, R9, and R10 are parasitic suppressors and capacitors C12, C15, and C17 are screen bypass capacitors. Capacitors C6, C13, and C16, shunted across cathode resistors R5, R8, and R12, respectively, serve to minimize cathode degeneration.

(3) The inverted output from V1 is coupled through capacitor C11 to voltage amplifier V2. The composite signal is developed across resistor R7 and applied to the control grid of V2. An inverted and am-
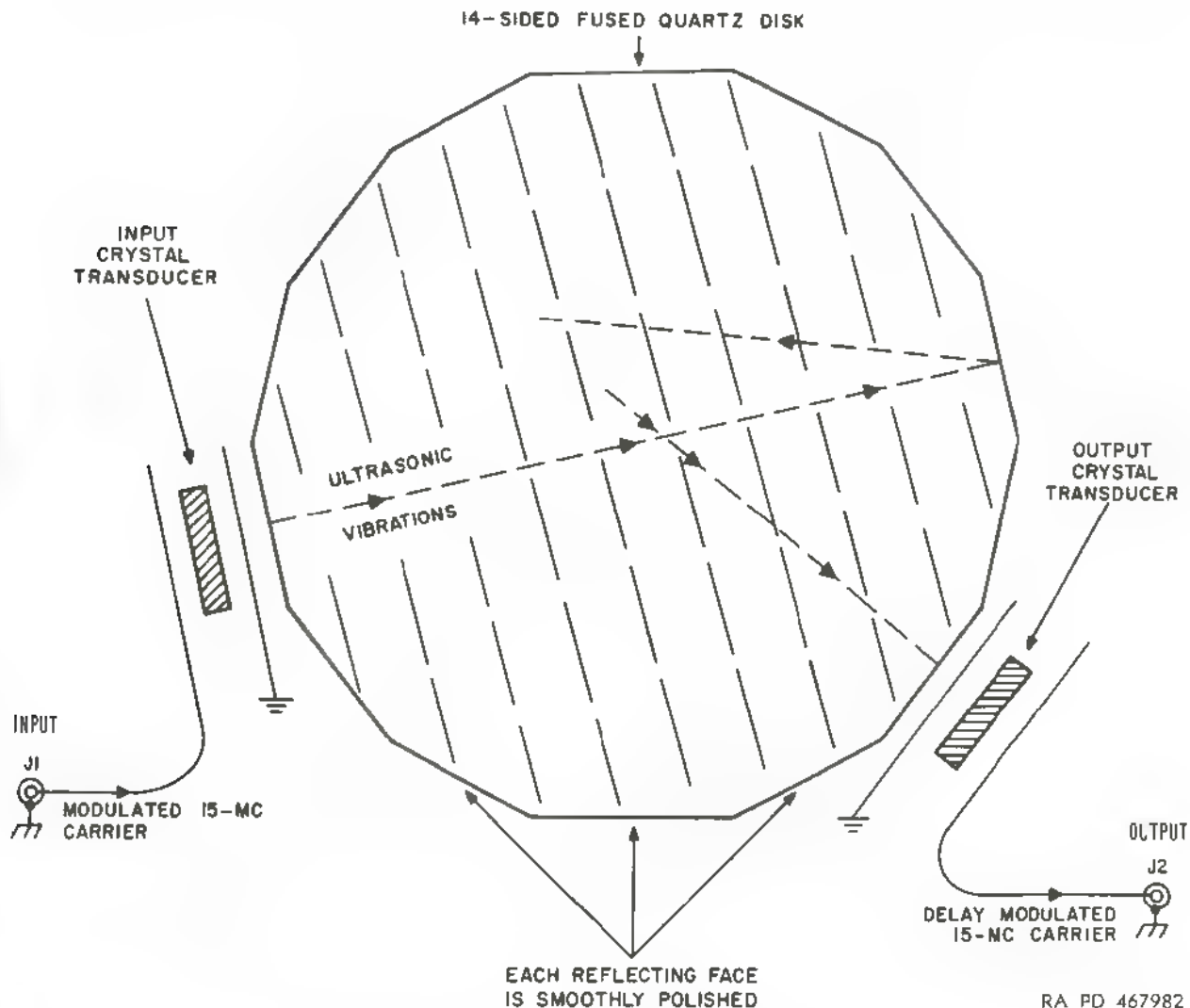
Figure 3. (U) MTI delay line—simplified schematic diagram

14-SIDED FUSED QUARTZ DISK

INPUT CRYSTAL TRANSDUCER

OUTPUT CRYSTAL TRANSDUCER

ULTRASONIC VIBRATIONS

INPUT

J1

MODULATED 15-MC CARRIER

OUTPUT

J2

DELAY MODULATED 15-MC CARRIER

EACH REFLECTING FACE IS SMOOTHLY POLISHED

RA PD 467982

plified facsimile of this input is applied from the junction of load inductor L7 and the plate of V2 through capacitor C14 to power amplifier V3. This signal is developed across resistor R11 and applied to the control grid of V3. In turn, the output of V3 is applied through transformer T1 to drive full-wave rectifier CR1 and CR2. The primary of T1 is shunted by resistor R13 to prevent ringing in T1; RF on the plate of V3 is filtered by inductor L1 and capacitor C3 to prevent RF from entering the power supply.

(4) The successive alternations of the modulated carrier are applied from the secondary of T1 to the plates of diodes CR1 and CR2 which form a full-wave rectifier. Shunting capacitor C18 maintains an equal potential between the plates with respect to the grounded center tap in the secondary of T1. The electron current flow originates in the input circuits of the external MTI synchronizer, and its direction of travel is through the connecting cable and connector J1 to the cathodes of CR1 and CR2. Conduction through the diodes depends upon which plate is positively polarized at the moment. The conducting diode appears as a short circuit and passes electrons to its related winding of T1. Then, the electron current flows to the center tap of T1, to ground, and returns to the input circuits in the MTI synchronizer. On the next signal alternation, the counterpart diode conducts. The combined action of the diodes provides full-wave rectification

of the signal by filtering out the carrier and detecting the modulating components. Filtering of the carrier is accomplished by stray circuit capacitances and the full-wave rectifier. The detected signals consist of a negative preknock pulse, positive test pulse, and positive MTI video pulses referenced at +4 volts dc. Because the positive, 7-microsecond test pulse is longer than the preknock pulse or MTI video pulses, an average dc value (+4 volts) is created by the full-wave rectifier conduction during the time the test pulse is applied. Therefore, the detected signals at J1 are referenced at +4 volts dc.

(5) The amplification provided by these three stages is adequate to compensate for the 52 ± 3 db of attenuation encountered in the MTI delay line. With proper AGC control, these stages provide an output level that is identical in amplitude and opposite in polarity to the non-delay video output at connector J3 of the carrier oscillator. Inductors L3, L4, and L5 with capacitors C7 through C10 prevent RF from entering the filament power supply.

14. (U) Trigger Pulse-Video Amplifier
    - 9137927

a. General. The trigger pulse-video amplifier sums the information content of the delay and non-delay channels to extract the moving-target component. It also synchronizes a preknock pulse with a delayed preknock pulse to obtain an auto sync pulse. Two cathode follower amplifiers provide delay and non-delay video to drive the external interference suppressor circuits.

b. Detailed Theory.
  (1) General. The trigger pulse-video amplifier (fig. 36, TM 9-1430-257-20) is divided into two sections. One section provides the auto sync pulse and the delay video for the external IS circuits. The other section re-establishes a dual channel system for oppositely polarized residue signals and provides non-delay video for the IS circuits. The two sections divide at the junction of R1 and R2.
  (2) Auto sync pulse circuit.
      (a) Trigger selector diode V1A selects the negative delayed preknock pulse by separating it from the positive video and test pulses succeeding it. The delayed video composite signal is developed across resistors R1 and R2 and applied to the cathode of V1A. The stage is biased so that positive video and test pulses keep V1A cut off. The delayed preknock pulse, however, is negative and drives V1A into conduction, creating a drop across load resistor R13. Since the plate follows the cathode the output signal is also a negative pulse. This negative pulse is directly coupled to the grid of trigger selector amplifier V1B, where it is amplified, inverted, and coupled through capacitor C2 to the grid of cathode follower V2A. The signal is developed across resistor R16. Since the cathode of V2A follows the grid, a positive preknock pulse is developed across cathode resistor R17. This pulse is coupled through capacitor C3 and superimposed on a neg-

ative disable gate applied through isolating resistor R18. The pulse which results from mixing the preknock pulse and the disable gate is called the MTI auto sync pulse.

      (b) During the quiescent state, the control grid of phantastron V3 is at a positive potential due to control grid current through resistors R21 and R22. Screen current through cathode resistor R20 causes the cathode to rise above the suppressor grid bias of 13.6 volts which is set by the voltage divider composed of resistors R23 and R24 between ground and +150 volts. The plate of V3 is on the threshold of conduction; therefore, no plate current flows through load resistor R25. Diode CR2 conducts from the +150-volt supply through R25 toward the +250-volt supply. The +150 volts, plus the small drop across CR2, is applied to the grid of cathode follower V4B. Since the cathode follows the grid, the junction of resistor R26 and capacitor C5 is raised to a voltage level higher than the control grid of V3. The side of C5 connected to the cathode of V4B charges to a higher positive level than the side connected to the control grid of V3. This is the quiescent state.
      (c) When a positive preknock pulse is applied through connector J1 and capacitor C6 to the suppressor grid of V3, plate current flows and the plate voltage drops below +150 volts. This change in plate

voltage is applied to the grid of V4B, causing the tube to conduct less current. The potential at the junction of R26 and C5 drops and since the charge on C5 cannot change instantaneously, the voltage drop appears on the control grid of V3. After the initial voltage drop at the junction of R26 and C5, C5 starts to discharge through R21, the +150-volt supply, ground, and R26 to the other side of C5.

(d) The initial drop at the junction of R26 and C5 also appears at the control grid of V3, causing a reduction in plate current and a rise in plate voltage. The rise in plate voltage is coupled to C5 and counteracts part of the capacitor discharge, thereby slowing discharge considerably. The degenerative effect produces an exponential voltage curve at the grid which is counteracted by an opposite voltage curve at the plate due to the inverting properties of the tube. This opposite effect is added algebraically to produce a linear current in R20 and a linear voltage drop across R20 (fig. 4).

(e) The time base of the inverted trapezoid is determined by the discharge time of C5 (fig. 36, TM 9-1430-257-20) and in this case the interval is 1500 microseconds. As C5 discharges, increased current flows through R20 with a resultant increase in bias. When C5 is completely discharged after 1500 microseconds, the cathode bias is sufficiently positive with re-

spect to the suppressor grid to cause cutoff of plate current. The plate voltage then rises to +150 volts and cathode follower V4B conducts at a steady rate. The dc level at the cathode of V4B is coupled through C5 to the control grid of V3 and maintains a steady screen current through resistor R19. Since the cathode potential exceeds that of the suppressor grid, V3 is returned to its quiescent state.

(f) The negative trapezoidal wave at the cathode of V3 is coupled through capacitor C4 to diode CR1 which clamps the dc reference level to 0 volts. The negative trapezoidal waveform is to be used as a disabling gate to prevent premature triggering of the external acquisitions-track synchronizer. The gate is applied through isolating resistor R18 and mixed with the positive preknock pulse from V2A which is coupled through C3. Here the positive preknock pulse is superimposed on the leading edge of the negative disable gate (fig. 4). This action occurs every 2000 microseconds. The combined action provides a sync time base for the MTI system, as well as the acquisition and target track systems. The MT1 auto sync pulse is applied to the external acquisition - track synchronizer through connector J2.

(3) Paraphase amplifiers V5A and V5B.

(a) The demodulated components of the composite signal from the non-delay channel are ap-

plied through connector P3. The signal consists of a positive preknock pulse followed by a negative test pulse and negative MTI video pulses referenced at -4 volts. This signal is applied to the grid of paraphase amplifier V5A through isolating resistor R4. Resistor R4 limits grid current to protect the crystal diodes in the external carrier oscillator.

(b) A signal identical to the one applied to P3, but of opposite polarity and opposite reference level, is applied from the delay channel through connector P2. This signal is applied through resistors R1 and R3 which, with resistor R2, form a "T" bridging network to isolate V5 from V1 but allow mixing of the two inputs. This delay signal is developed across R2, then passes through network Z1 (a fixed 0.6-microsecond delay network) and time balance variable impedance network Z2 (a variable 0 to 0.3-microsecond delay network) to provide fine synchronization of the two signals on the grid of V5A. The grid of V5A is returned to ground through resistor R5 and the 1350-ohm terminating resistor in Z2.

(c) The inversely polarized delay and non-delay signals, occuring at the same interval, having equal bases, and being equal in amplitude, cancel at the grid of V5A. Any residue present after cancellation is determined by non-symmetrical elements of the algebraically combined video signals. The resulting signal is the desired moving-target video which is then amplified in V5A and cathode coupled to paraphase amplifier V5B.

(d) Amplifiers V5A and V5B provide two output signals, one in phase and the other 180 degrees out of phase with the moving-target video input signal. The two output voltages of opposite phases are necessary for driving the push-pull amplifier in the external MTI video amplifier. The dual triode sections of V5 are coupled together through common cathode resistor R10 which, together with resistors R8 and R9, forms the cathode voltage divider between ground and -250 volts. Amplifier V5A inverts the applied signal and increases the amplitude to the desired level. The plate of V5B follows the grid signal of V5A. Amplifier V5B amplifies the signal to the same level as that obtained from V5A. The grids of both triodes are at dc ground potential. Due to the symmetry of stages, the quiescent currents of the two triodes are nearly equal. These currents add in R10 to prevent fluctuations when the -250-volt power supply fluctuates. This biasing arrangement provides for highly effective self-compensation. An increase in value of negative supply voltage causes an increase in the quiescent tube currents and thus an increase in the drop across R10, making up for the drop in the supply voltage.

(e) In dynamic operation, the large cathode resistor, R10, has the effect of preventing an appreciable change in the sum of the two quiescent currents. When the quiescent current through V5A decreases, due to a negative signal being applied to the grid, the potential on the cathodes tends to drop. This decreases the cathode-to-grid voltage on V5B, causing an increase in the quiescent current through V5B. The sum current flowing through R10 thus remains essentially constant, since an extremely small variation in the sum current is enough to allow the cathode to swing by an amount sufficient for adjusting the current through V5B, as required. Accordingly, every excursion of the quiescent current through V5A from the quiescent value results in a very nearly equal and oppositely directed excursion of quiescent current through V5B. The cathode potential is such as to allow the currents to compensate each other in the described manner, i.e., the cathodes swing in phase with the moving-target signal applied to the grid of V5A and with an amplitude equal to half the signal amplitude. As a result, only half the signal is effective between the cathode and grid of V5B. The alternating voltages on the plates of V5A and V5B are, accordingly, equal in amplitude and opposite in phase.

(f) The signal from the junction of the plate of V5A and re-sistor R6 is the phase 1 output and is connected to the external load through connector P5. The signal from the junction of the plate of V5B and resistor R7 is the phase 2 output and is connected to the external load through connector P4.

(4) Delay video amplifier V4A. The composite signal from the delay channel, which consists of a negative preknock pulse followed by a positive test pulse plus positive video pulse, is taken from the TIME BAL output of variable delay network Z2. The signal is developed across resistors R29 and R31 and applied to the grid of cathode follower V4A through parasitic suppressor resistor R28. Degenerative feedback from the junction of cathode resistors R30 and R31 is used to improve amplifier stability. The low-impedance output is connected to the external load through connector J4.

(5) Non-delay video amplifier V2B. The composite signal from the non-delay channel, which consists of a positive preknock pulse followed by a negative test pulse and negative video pulses, is taken from connector P3, coupled through capacitor C8, developed across resistor R34 and R35, and coupled through parasitic suppressor resistor R32 to the grid of cathode follower V2B. Degenerative feedback from the junction of cathode resistors R33 and R35 is used to improve amplifier stability. The low-impedance output is connected to the external load through connector J3.

14.1 (U). Trigger Pulse-Video Amplifier 9989353

Trigger pulse-video amplifier 9989353 is identical to trigger pulse-video amplifier 9137927 discussed in paragraph 14 except for the added relay K1 (fig. 36.1, TM 9-1430-257-20). When relay K1 is deenergized, the output of TIME BAL network Z2 is applied through contacts 8-6 and 42 to coupling capacitor C7. When K1 is energized, delay video is coupled through contacts 5-6 and 12 to coupling capacitor C7 thus passing the delay video around the TIME BAL network. This action is necessary in order to obtain coincidence when operating in the processor mode in the antijam display receiver.

PREKNOCK PULSE

2000 USEC

0

PLATE EFFECT

RESULTANT

GRID EFFECT

DISABLE GATE
1500 USEC

RA PD 467983
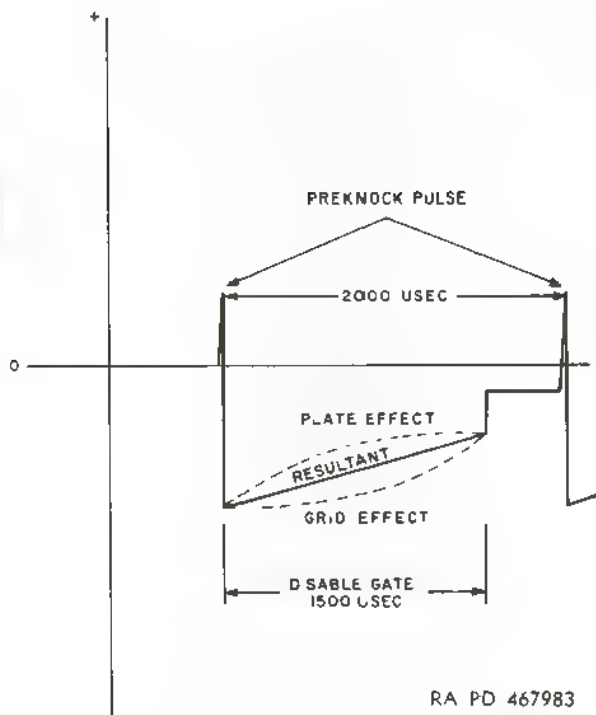
Figure 4. (U) MTI auto sync pulse

15. (U) Acquisition-Track Synchronizer 9142937

   a. General. The acquisition-track synchronizer generates the timing pulses that control the operations of the acquisition radar system. These pulses are: preknock, MTI test, transmitter sync, and sync. For accurate MTI operation, the acquisition-track synchronizer is synchronized with the MTI system by the MTI auto sync pulse.

   b. Detailed Theory.

   (1) Preknock pulse circuit.

   (a) Sync amplifier V1. An MTI auto sync pulse, which consists of a positive pulse superimposed on the leading edge of a negative disable gate, is applied from connector J1 to INT-AUTO switch S1 (fig. 43, TM 9-1430-257-20). When S1 is in the INT position, there is no input to sync amplifier V1 and repeti-

tion rate blocking oscillator V2A operates as a free-running blocking oscillator, as described in (b) below. Switch S1 is placed in the INT position during chassis testing or when it is desired to operate the acquisition-track synchronizer disconnected from the MTI system. When S1 is placed in the AUTO position, the MTI auto sync pulse is developed across resistor R2 and applied to the control grid of V1. The positive portion of the MTI auto sync pulse is amplified in V1 and a resulting negative sync pulse is developed across the primary of blocking oscillator transformer T1. Amplifier V1 is cut off for the following 1,500 microseconds by the negative disable gate portion of the MTI auto sync pulse. This action prevents false triggering of V2A by circuit stray pulses. Capacitor C1 and resistor R1 provide a screen-grid decoupling for V1. Resistor R3 establishes bias for V1 and capacitor C2 bypasses ac signals around R3.

   (b) Repetition rate blocking oscillator V2A.

   1. Free-running operation. When plate voltage is applied, V2A conducts. The surge of current through plate winding 1-2 of T1 causes a voltage to be induced in winding 3-4 of T1. This drives the grid positive, and current increases through V2A and plate winding 1-2 of T1. The increase in current causes a larger positive voltage to be cou-

pled to the grid of V2A, and the regenerative coupling action between the plate and grid windings of T1 quickly drives V2A into saturation. However, grid current flows before saturation is reached. This current charges the grid side of capacitor C4 negative. At saturation, the current through winding 1-2 becomes constant. Since no positive voltage is coupled to the grid of V2A, tube current decreases. Capacitor C4 is allowed to discharge through resistor R11, FREQ variable resistor R6, R5, the +250-volt power supply, ground, and through cathode resistors R48 and R47 back to C4. The negative voltage on C4 causes a decrease in conduction through V2A and the electromagnetic fields of winding 1-2 in T1 to start collapsing. The collapsing fields of winding 1-2 of T1 cause a negative voltage to be coupled through C4 to the grid of V2A, driving V2A well beyond cutoff. As C4 discharges, the grid of V2A rises toward ground. Near ground potential, V2A conducts and the free-running cycle is repeated. Resistor R6 is adjusted so that the free-running frequency is slightly lower than 500 pps. This allows the MTI auto sync pulse to trigger the circuit into oscillation before it normally be-

comes free-running, provided the INT-AUTO switch is set to AUTO.

2. *Synchronized operation.* Since the pulse repetition frequency of the MTI auto sync pulse is 500 pps, it is applied to the grid of V2A at a time when the grid is still rising exponentially toward cutoff. Therefore, the MTI auto sync pulse raises the grid potential above cutoff prior to the time V2A would normally conduct in its free-running state. This action synchronizes its frequency with the MTI auto sync pulse frequency. A positive 20-40-volt, 1-microsecond pulse is developed across R48 and coupled to connector J2, trigger amplifier V3A, and 5-microsecond delay network Z2. Capacitors C3A and C3B and resistor R5 form a decoupling network for the +250-volt power supply.

(2) *MTI test pulse circuit.*

(a) The positive preknock pulse is delayed 5 microseconds in delay network Z2 and then coupled through capacitor C12 to the grid of voltage amplifier V6A. Amplifier V6A is normally cut off by −25 volts applied to the grid by the voltage divider composed of resistors R35 and R34 from ground to −250 volts. When the preknock pulse triggers V6A into conduction, an amplified negative pulse is developed across winding 3-4 of pulse transformer T3. The negative pulse is inverted by T3 and applied as a positive pulse to the grid of MTI test pulse blocking oscillator V6B.

(b) Blocking oscillator V6B is normally cut off by −25 volts applied to the grid by the voltage divider composed of resistors R38 and R37 from ground to the −250-volt supply. When triggered by the preknock pulse, V6B conducts for 7 microseconds. The operation of V6B is similar to V2A, as described in (1)(b) above. A positive 6-volt, 7-microsecond test pulse is developed across cathode resistor R40. This pulse is applied to connector J3. Resistor R42 and capacitor C14 are a decoupling network for the +250-volt power supply.

(3) *Sync pulse circuit.*

(a) The positive preknock pulse is coupled through capacitor C5 and resistor R14 to the grid of trigger amplifier V3A. Amplifier V3A is normally cut off by −30 volts applied to the grid by the voltage divider consisting of resistors R13 and R12 from ground to the −250-volt supply. When the preknock pulse triggers V3A into conduction, an amplified negative pulse is developed across resistor R15. This resistor is the common plate load of V3A and delay multivibrator V4A, which is one section of a monostable plate-coupled multivibrator. The negative pulse is then coupled through capacitor C7 to the grid of delay multivibrator V4B. Beginning with system 1059, type 5814 tubes V4 and V5 have been changed to ruggedized type 5814A tubes.

(b) Multivibrator V4A is normally cut off by −30 volts applied to the grid by the voltage divider consisting of resistors R16 and R17 from ground to the −250 volt supply. Multivibrator V4B is normally conducting since the grid is returned through current limiting resistor R22 to the +250-volt supply.

(c) When the negative pulse is applied to the grid of V4B from V3A, V4B cuts off. The resulting positive rise in plate voltage at V4B is coupled through capacitor C6 to the grid of V4A and raises the grid above cutoff. The resulting negative drop in plate voltage at V4A is coupled through C7 to the grid of V4B, and keeps V4B cut off until C7 discharges sufficiently through R22 to place the grid of V4B near ground potential. At this point, 60 microseconds later, V4B conducts.

CONFIDENTIAL

The resulting negative drop in plate voltage at V4B is coupled through C6 to the grid of V4A. This negative voltage cuts off V4A, returning V4A and V4B to the quiescent state with V4A cut off and V4B conducting. A negative 60-microsecond gate is produced in the plate circuit of V4A. This gate is coupled directly to a pulse delay circuit composed of temperature-controlled delay line Z1 and switch diode V3B.

(d) Switch diode V3B is connected as a diode since the grid is connected to the plate. In the quiescent state, V3B conducts heavily since its plate and grid are returned to the +250-volt supply. The return path is through Z1 and SYNC DELAY variable resistor R21. The voltage drop across cathode resistor R41 places the plate and cathode of V3B at +2.5 volts above ground. The capacitor located in Z1 charges between this voltage and the +250 volts at the plate of V4A, which is cut off at this time.

(e) In the dynamic state, V4A produces a negative 60-microsecond gate which is coupled through the delay line capacitor in Z1 to V3B. This negative gate cuts off V3B, causing the voltage across R41 to drop to 0 volts. Simultaneously, the delay line capacitor begins discharging to the low-plate voltage of V4A through Z1, R21, the +250-volt supply, ground, and V4A. Adjustment of R21 varies the discharge time by ±1 microsecond. Approximately 23.5 microseconds later, the plate of V3B rises slightly above ground potential. Since the plate of V3B is now positive with respect to the cathode, V3B conducts. The voltage across R41 again rises to +2.5 volts, producing the trailing edge of the 23.5-microsecond negative gate. Since V3B cuts on and off sharply, the output gate is square-sided, thus lending itself easily to dif-

ferentiation. The conduction of V3B clamps its plate to +2.5 volts, preventing any further discharge of the delay line capacitor. Therefore, this capacitor charges from +2.5 volts to the low-plate voltage of V4A. When the trailing edge of the 60-microsecond gate passes, the plate of V4A rises again to +250 volts. The delay line capacitor continues charging to this voltage, re-establishing the quiescent condition of the circuit. A temperature-regulating resistive element is mounted in Z1 and returned through terminals 4 and 5 to 6.3 volts ac. Its heat dissipation varies with temperature, thus effectively counteracting any temperature changes within Z1. Consequently, the resistance of the resistors within Z1 does not fluctuate with temperature changes, and the period of delay does not vary from 23.5 microseconds.

(f) The negative 23.5-microsecond gate from V3B is coupled directly to the grid of pulse delay amplifier V5A. An amplified positive gate is differentiated by capacitor C8 and resistor R26, producing negative and positive pips at the grid of pulse delay amplifier V5B. The pips correspond in time to the leading and trailing edges of the 23.5-microsecond gate.

(g) With no signal applied, V5B is cut off by −25 volts applied to the grid by the voltage divider consisting of resistors R27 and R28 from ground to the 250-volt supply. Capacitor C9 stabilizes this potential. The positive pip from V5A raises the grid of V5B above cutoff, and V5B conducts. An amplified negative pip is developed across primary winding 6–5 of blocking oscillator transformer T2.

(h) Since a blocking oscillator transformer is designed to pass narrow pulses, its high-frequency response is good. Conversely, its low-frequency response is

20

CONFIDENTIAL

poor. Therefore, T2 passes the high-frequency components in the pips and attenuates the low-frequency components. This action effectively improves the shape of the pips. The pips are coupled through secondary winding 1-2 and tertiary winding 3-4 of T2 to the grid of sync pulse blocking oscillator V2B.

(i) Blocking oscillator V2B is normally cut off by approximately —25 volts bias between the grid and cathode established by the voltage divider consisting of resistors R32, R33, and R30 connected between ground and the —250-volt supply. Since V2B is cut off, the leading negative pip has no effect. However, the trailing positive pip triggers V2B into conduction 23.5 microseconds after preknock time. The operation of V2B is similar to that of V2A, as described in (1)(b) above. Blocking oscillator V2B produces a positive 40-volt, 0.15-microsecond sync pulse, which is developed across cathode resistor R30 and coupled directly to connector J4 through C15 to sync pulse amplifier V7A. Capacitor C10 and resistor R29 provide plate decoupling for V5B, V2B, V7A, and V7B. Resistor R8 limits any grid current in V7A.

(4) *Transmitter sync pulse circuit.*

(a) Sync pulse amplifier V7A is normally cut off by —30 volts applied to the grid by the voltage divider composed of resistors R7 and R9 from ground to the —250-volt supply. Capacitor C16 stabilizes this potential. When the sync pulse triggers V7A into conduction, an amplified negative pulse is developed across winding 1-2 of blocking oscillator transformer T4. This pulse is induced and inverted in winding 3-4 of T4 and applied as a positive pulse to the grid of transmitter sync pulse blocking oscillator V7B.

(b) Blocking oscillator V7B is normally cut off by —25 volts applied to the

grid by the voltage divider consisting of resistors R45 and R46 from ground to the —250-volt supply. The positive pulse raises the grid above cutoff, and V7B conducts for 0.15 microsecond. The operation of V7B is similar to V2A, as described in (1)(b) above. A positive 40-volt, 0.15-microsecond transmitter sync pulse is produced across cathode resistor R49 and coupled to connector J5.

15.1 (U). Acquisition-Track Synchronizer 9144786

a. *General.* The acquisition-track synchronizer generates the timing pulses that control the operations of the acquisition radar system. These pulses are: preknock, MTI test, transmitter sync, and sync. For accurate MTI operation, the acquisition-track synchronizer is synchronized with the MTI system by the MTI auto sync pulse.

b. *Detailed Theory.*

(1) *Preknock pulse circuit.*

(a) *Sync amplifier V1.* An MTI auto pulse, which consists of a positive pulse superimposed on the leading edge of a negative disable gate, is applied from connector J1 to contact 4 of relay K3 (fig. 93, TM 9-1430-257-20/1). When relay K3 is energized, there is no input to sync amplifier V1 and repetition rate blocking oscillator V2A operates as a free-running blocking oscillator, as described in (b) below. When relay K3 is deenergized, the MTI auto sync pulse is developed across resistor R2 and applied to the control grid of V1. The positive portion of the MTI auto sync pulse is amplified in V1, and a resulting negative sync pulse is developed across the primary of blocking oscillator transformer T1. Amplifier V1 is cut off for the following 1500 microseconds by the negative disable gate portion of the MTI auto sync pulse. This action prevents false trig-

gering of V2A by circuit stray pulses. Capacitor C1A and resistor R1 provide a screen-grid decoupling for V1. Resistor R3 establishes bias for V1 and capacitor C2 bypasses ac signals around R3.

(b) *Repetition rate blocking oscillator V2A.*

1. *Free-running operation.* When plate voltage is applied, V2A conducts. The surge of current through plate winding 1-2 of T1 causes a voltage to be induced in winding 3-4 of T1. This drives the grid positive, and current increases through V2A and plate winding 1-2 of T1. The increase in current causes a larger positive voltage to be coupled to the grid of V2A, and the regenerative coupling action between the plate and grid windings of T1 quickly drives V2A into saturation. However, grid current flows before saturation is reached. This current charges the grid side of capacitor C4 negative. At saturation, the current through winding 1-2 becomes constant. Since no positive voltage is coupled to the grid of V2A, tube current decreases. With relay K1 deenergized, capacitor C4 discharges through resistor R11, FREQ LOPAR variable resistor R6, R5, the +250-volt power supply, ground, and through cathode resistors R48 and R47 back to C4. The negative voltage on C4 causes a decrease in conduction through V2A and the electromagnetic fields of winding 1-2 in T1 to start collapsing. The collapsing fields of winding 1-2 of T1 cause a negative voltage to be coupled through C4 to the grid of V2A, driving V2A well beyond cutoff. As C4 discharges, the grid of V2A rises toward ground. Near ground potential, V2A conducts and the free-running cycle is repeated. FREQ LOPAR variable resistor

R6 is adjusted so that the free-running frequency is slightly lower than the LOPAR repetition rate of 500 pps. This allows the MTI auto sync pulse to trigger the circuit into oscillation before it normally becomes free-running, provided relay K3 is deenergized. With relay K1 energized, capacitor C4 discharges through resistor R1 and FREQ HIPAR variable resistor R50 instead of R11 and R6. FREQ HIPAR variable resistor R50 is adjusted so that the free-running frequency is slightly lower than the HIPAR repetition rate of 400 pps. This allows the MTI auto sync pulse to trigger the circuit into oscillation before it normally becomes free-running.

2. *Synchronized operation.* Since the pulse repetition rate of the MTI auto sync pulse is either 400 pps or 500 pps, it is applied to the grid of V2A at a time when the grid is still rising exponentially toward cutoff. Therefore, the MTI auto sync pulse raises the grid potential above cutoff prior to the time V2A would normally conduct in its free-running state. This action synchronizes its frequency with the MTI auto sync pulse frequency. A positive 20-40-volt, 1-microsecond pulse is developed across R48 and coupled to connector J2, trigger amplifier V3A, and 5-microsecond delay network Z2. Capacitors C3A and C3B and resistor R5 form a decoupling network for the +250-volt power supply.

(2) *MTI test pulse circuit.*

(a) The positive preknock pulse is delayed 5 microseconds in delay network Z2 and then coupled through capacitor C12 to the grid of voltage amplifier V6A. Amplifier V6A is normally cut off by −25 volts applied to the grid by the voltage

divider composed of resistors R35 and R34 from ground to −250 volts. When the preknock pulse triggers V6A into conduction, an amplified negative pulse is developed across winding 3-4 of pulse transformer T3. The negative pulse is inverted by T3 and applied as a positive pulse to the grid of MTI test pulse blocking oscillator V6B.

(b) Blocking oscillator V6B is normally cut off by −25 volts applied to the grid by the voltage divider composed of resistors R38 and R37 from ground to the −250-volt supply. When triggered by the preknock pulse, V6B conducts for 7 microseconds. The operation of V6B is similar to V2A, as described in (1)(b) above. A positive 6-volt, 7-microsecond test pulse is developed across cathode resistor R40. This pulse is applied to connector J3. Resistor R42 and capacitor C14 are a decoupling network for the +250-volt power supply.

(3) *Sync pulse circuit.*

(a) The positive preknock pulse is coupled through capacitor C5 and resistor R14 to the grid of trigger amplifier V3A. Amplifier V3A is normally cut off by −30 volts applied to the grid by the voltage divider consisting of resistors R13 and R12 from ground to the −250-volt supply. When the preknock pulse triggers V3A into conduction, an amplified negative pulse is developed across resistor R15. This resistor is the common plate load of V3A and delay multivibrator V4A, which is one section of a monostable plate-coupled multivibrator. The negative pulse is then coupled through capacitor C7 to the grid of delay multivibrator V4B.

(b) Multivibrator V4A is normally cut off by −30 volts applied to the grid by the voltage divider consisting of resistors R16 and R17 from ground to the −250-volt supply. Multivibrator V4B is normally conducting

since the grid is returned through current limiting resistor R22 to the +250-volt supply.

(c) When the negative pulse is applied from V3A to the grid of V4B, V4B cuts off. The resulting positive rise in plate voltage at V4B is coupled through capacitor C6 to the grid of V4A and raises the grid above cutoff. The resulting negative drop in plate voltage at V4A is coupled through C7 to the grid of V4B, and keeps V4B cut off until C7 discharges sufficiently through R22 to place the grid of V4B near ground potential. At this point, 60 microseconds later, V4B conducts. The resulting negative drop in plate voltage at V4B is coupled through C6 to the grid of V4A. This negative voltage cuts off V4A, returning V4A and V4B to the quiescent state with V4A cut off and V4B conducting. A negative 60-microsecond gate is produced in the plate circuit of V4A. This gate is coupled directly to a pulse delay circuit composed of temperature-controlled delay line Z1 and switch diode V3B.

(d) Switch diode V3B is connected as a diode since the grid is connected to the plate. In the quiescent state, V3B conducts heavily since its plate and grid are returned to the +250-volt supply. When relay K2 is deenergized, the return path is through Z1 and SYNC DELAY LONG PULSE variable resistor R21. When K2 is energized, the return path is through Z1 and SYNC DELAY SHORT PULSE variable resistor R52. The voltage drop across cathode resistor R41 places the plate and cathode of V3B at +2.5 volts above ground. The capacitor located in Z1 charges between this voltage and the +250 volts at the plate of V4A, which is cut off at this time.

(e) In the dynamic state, V4A produces a negative 60-microsecond gate which is coupled through the

delay line capacitor in Z1 to V3B. This negative gate cuts off V3B, causing the voltage across R41 to drop to 0 volts. Simultaneously, the delay line capacitor begins discharging to the low-plate voltage of V4A through Z1, R21 or R52, the +250-volt supply, ground, and V4A. Adjustment of R21 or R52 varies the discharge time by ±1 microsecond. Approximately 23.5 microseconds later, the plate of V3B rises slightly above ground potential. Since the plate of V3B is now positive with respect to the cathode, V3B conducts. The voltage across R41 again rises to +2.5 volts, producing the trailing edge of the 23.5-microsecond negative gate. Since V3B cuts on and off sharply, the output gate is square-sided, thus lending itself easily to differentiation. The conduction of V3B clamps its plate to +2.5 volts, preventing any further discharge of the delay line capacitor. Therefore, this capacitor charges from +2.5 volts to the low-plate voltage of V4A. When the trailing edge of the 60-microsecond gate passes, the plate of V4A rises again to +250 volts. The delay line capacitor continues charging to this voltage, reestablishing the quiescent condition of the circuit. A temperature-regulating resistive element is mounted in Z1 and returned through terminals 4 and 5 to 6.3 volts ac. Its heat dissipation varies with the temperature, thus effectively counteracting any temperature changes within Z1. Consequently, the resistance of the resistors within Z1 does not fluctuate with temperature changes, and the period of delay does not vary from 23.5 microseconds.

(f) The negative 23.5-microsecond gate from V3B is coupled directly to the grid of pulse delay amplifier V5A. An amplified positive gate is differentiated by capacitor C8 and resistor R26, producing negative and positive pips at the grid of pulse delay amplifier V5B. The pips correspond in time to the leading and trailing edges of the 23.5-microsecond gate.

(g) With no signal applied, V5B is cut off by -25 volts applied to the grid by the voltage divider consisting of resistors R27 and R28 from ground to the -250-volt supply. Capacitor C1B stabilizes this potential. The positive pip from V5A raises the grid of V5B above cutoff, and V5B conducts. An amplified negative pip is developed across primary winding 6-5 of blocking oscillator transformer T2.

(h) Since a blocking oscillator transformer is designed to pass narrow pulses, its high-frequency response is good. Conversely, its low-frequency response is poor. Therefore, T2 passes the high-frequency components in the pips and attenuates the low-frequency components. This action effectively improves the shape of the pips. The pips are coupled through secondary winding 1-2 and tertiary winding 3-4 of T2 to the grid of sync pulse blocking oscillator V2B.

(i) Blocking oscillator V2B is normally cut off by approximately —25 volts bias between the grid and cathode established by the voltage divider consisting of resistors R32, R33, and R30 connected between ground and the —250-volt supply. Since V2B is cut off, the leading negative pip has no effect. However, the trailing positive pip triggers V2B into conduction 23.5 microseconds after preknock time. The operation of V2B is similar to that of V2A, as described in (1)(b) above. Blocking oscillator V2B produces a positive 40-volt, 0.15-microsecond pulse, which is developed across cathode resistor R30 and coupled directly to connector J4 and through C15 to synchronizing pulse amplifier V7A. Capacitor C10 and

resistor R29 provide plate decoupling for V5B, V2B, V7A, and V7B. Resistor R8 limits any grid current in V7A.

(4) *Transmitter sync pulse circuit.*

(a) Sync ranging pulse amplifier V7A is normally cut off by −30 volts applied to the grid by the voltage divider composed of resistors R7 and R9 from ground to the −250-volt supply. Capacitor C16 stabilizes this potential. When the sync pulse triggers V7A into conduction, an amplified negative pulse is developed across winding 1-2 of blocking oscillator transformer T4. This pulse is induced and inverted in winding 3-4 of T4 and applied as a positive pulse to the grid of synchronizing pulse blocking oscillator V7B.

(b) Blocking oscillator V7B is normally cut off by −25 volts applied to the grid by the voltage divider consisting of resistors R45 and R46 from ground to the −250-volt supply. The positive pulse raises the grid above cutoff, and V7B conducts for 0.15 microsecond. The operation of V7B is similar to V2A, as described in (1) (b) above. A positive 40-volt, 0.15-microsecond transmitter sync pulse is produced across cathode resistor R49 and coupled to connector J5.

(5) *Relay circuits.* Relay K1 is operated when the HIPAR is being used. Contacts of K1 are used to change the free-running frequency of repetition rate oscillator V2A. Contacts of relay K2 select the appropriate variable resistor, R21 or R52, for pulse delay diode V3B. Contacts of relay K3 disconnect the input to synchronizer amplifier V1 under certain test conditions determined by TEST switch S1.

15.2 (U). Acquisition-Track Synchronizer 9988748

a. *General.* The acquisition-track synchronizer generates the timing pulses that control the operations of the acquisition radar system. These pulses are: preknock, MTI test, transmitter sync, and sync. For accurate MTI operation, the acquisition-track synchronizer is synchronized with the MTI system by the MTI auto sync pulse. The synchronizer controls the sync rate of acquisition radar system and the target tracking radar system.

b. *Detailed Theory.*

(1) *Preknock pulse circuit.*

(a) *Sync amplifier V1.* An MTI auto sync pulse, which consists of a positive pulse superimposed on the leading edge of a negative disable gate, is applied from connector J1 to INT-AUTO switch S1 (fig. 43.1, TM 9-1430-257-20). When S1 is in the INT position, there is no input to sync amplifier V1 and repetition rate blocking oscillator V2A operates as a free-running blocking oscillator, as described in (b) below. Switch S1 is placed in the INT position during chassis testing or when it is desired to operate the acquisition-track synchronizer disconnected from the MTI system. When S1 is placed in the AUTO position, the MTI auto sync pulse is developed across resistor R2 and applied to the control grid of V1. The positive portion of the MTI auto sync pulse is amplified in V1 and a resulting negative sync pulse is developed across the primary of blocking oscillator transformer T1. Amplifier V1 is cut off for the following 1500 microseconds by the negative disable gate portion of the MTI auto sync pulse. This action prevents false triggering of V2A by circuit stray pulses. Capacitor C1 and resistor R1 provide a screen-grid decoupling for V1. Resistor R3 establishes bias for V1 and capacitor C2 bypasses ac signals around R3.

(b) *Repetition rate blocking oscillator V2A.*

1. *Free-running operation.* When plate voltage is applied, V2A

conducts. The surge of current through plate winding 1-2 of T1 causes a voltage to be induced in winding 3-4 of T1. This drives the grid positive, and current increases through V2A and plate winding 1-2 of T1. The increase in current causes a larger positive voltage to be coupled to the grid of V2A, and the regenerative coupling action between the plate and grid windings of T1 quickly drives V2A into saturation. However, grid current flows before saturation is reached. This current charges the grid side of capacitor C4 negative. At saturation, the current through winding 1-2 becomes constant. Since no positive voltage is coupled to the grid of V2A, tube current decreases. When NAR is selected, relay K1 is deenergized and capacitor C4 is allowed to discharge through resistor R11, FREQ variable resistor R6, R5, the +250-volt power supply, ground, and through cathode resistors R48 and R47 back to C4. When AAR is selected, relay K1 is energized and capacitor C4 must discharge through the additional resistance of R50. Relay K1 is operational only in the target radar control console. It does not operate in the acquisition radar system. The negative voltage on C4 causes a decrease in conduction through V2A and allows the electromagnetic fields of winding 1-2 in T1 to start collapsing. The collapsing fields of winding 1-2 of T1 causes a negative voltage to be coupled through C4 to the grid of V2A, driving V2A well beyond cutoff. As C4 discharges, the grid of V2A rises toward ground. Near ground potential, V2A conducts and the free-running cycle is repeated. Resistor R6 is adjusted so that the free-running frequency is slightly lower than 500 pps when NAR is selected. When AAR is selected, the additional delay in discharge time for C4 through added resistor R50 changes the free-running frequency of the target track synchronizer to 400 pps. This allows the MTI auto pulse to trigger the circuit into oscillation before it normally becomes free-running, provided the INT-AUTO switch is set to AUTO.

2. *Synchronized operation.* Since the pulse repetition frequency of the MTI auto sync pulse is 500 pps, it is applied to the grid of V2A at a time when the grid is still rising exponentially toward cutoff. Therefore, the MTI auto sync pulse raises the grid potential above cutoff prior to the time V2A would normally conduct in its free-running state. This action synchronizes its frequency with the MTI auto sync pulse frequency. A positive 20-40-volt, 1-microsecond pulse is developed across R48 and coupled to connector J2, trigger amplifier V3A, and 10-microsecond delay network Z2. Capacitors C3A and C3B and resistor R5 form a decoupling network for the +250-volt power supply.

(2) *IFF trigger pulse circuit.* The positive preknock pulse is coupled from the cathode of V2A through capacitor C12 to grid 2 of cathode-follower section 1-2-3 of V6. Section 1-2-3 of V6 is normally cut off by 25 volts applied to the grid by the voltage divider composed of resistors R35 and R34 from ground to −250 volts. When triggered by the preknock pulse, section 1-2-3 of V6 conducts and a positive pulse is developed across cathode resistor R53. This positive pulse is coupled to IFF

TRIGGER OUT connector J6. This trigger pulse is used in the external IFF equipment. Resistor R42 and capacitor C14 decouple the ac signals on the plates of V6 from the power supply.

(3) *MTI test pulse circuit.* The positive preknock pulse is delayed 10 microseconds in delay network Z2 and then coupled through crystal diode CR1 to winding 1-2 of pulse transformer T3. The pulse output voltage from the delay network is developed across resistor R44. Crystal diodes CR1 and CR2 are connected to shunt negative pulses developed in winding 1-2 of T3 to ground to prevent interaction in the preknock pulse circuit. The blocking oscillator section of V6 is normally cut off by –25 volts applied to grid 7 by the voltage divider composed of resistors R38 and R37 from ground to the –250-volt supply. When triggered by the preknock pulse, V6 conducts for 7 microseconds. The operation of the blocking oscillator section of V6 is similar to V2A, as described in (1) (b) above. A positive 6-volt, 7-microsecond test pulse is developed across cathode resistor R40. This pulse is applied to connector J3. Resistor R42 and capacitor C14 are a decoupling network for the +250-volt power supply.

(4) *Sync pulse circuit.*

(a) The positive preknock pulse is coupled through capacitor C5 and resistor R14 to the grid of trigger amplifier V3A. Amplifier V3A is normally cut off by –30 volts applied to the grid by the voltage divider consisting of resistors R13 and R12 from ground to the –250-volt supply. When the preknock pulse triggers V3A into conduction, an amplified negative pulse is developed across resistor R15. This resistor is the common plate load of V3A and delay multivibrator section 1-2-3 of V4, which is one section of a monostable plate-coupled multivibrator. The negative pulse is then coupled through capacitor C7 to grid 7 of delay multivibrator V4.

(b) Multivibrator V4 section 1-2-3 is normally cut off by –30 volts applied to grid 2 by the voltage divider consisting of resistors R16 and R17 from ground to the –250-volt supply. Multivibrator V4 section 6-7-8 is normally conducting since grid 7 is returned through current limiting resistor R22 to the +250-volt supply.

(c) When the negative pulse is applied to grid 7 of V4 from V3A, V4 section 6-7-8 cuts off. The resulting positive rise in plate voltage at plate 6 of V4 is coupled through capacitor C6 to grid 2 of V4 and raises the grid above cutoff. The resulting negative drop in plate voltage at pin 1 of V4 is coupled through C7 to grid 7 of V4, and keeps V4 section 6-7-8 cut off until C7 discharges sufficiently through R22 to place grid 7 of V4 near ground potential. At this point, 60 microseconds later, V4 section 6-7-8 conducts. The resulting negative drop in plate voltage at pin 6 of V4 is coupled through C6 to grid 2 of V4. This negative voltage cuts off section 1-2-3 of V4, returning V4 to the quiescent state with section 1-2-3 of V4 cut off and section 6-7-8 of V4 conducting. A negative 60-microsecond gate is produced in the plate circuit of V4 section 1-2-3. This gate is coupled directly to a pulse delay circuit composed of temperature-controlled delay line Z1 and switch diode V3B.

(d) Switch diode V3B is connected as a diode since the grid is connected to the plate. In the quiescent state, V3B conducts heavily since its plate and grid are returned to the +250-volt supply. The return path is through Z1 and SYNC

DELAY variable resistor R21, and resistor R52 when K1 is deenergized. The voltage drop across cathode resistor R41 places the plate and cathode of V3B at +2.5 volts above ground. The capacitor located in Z1 charges between this voltage and the +250 volts at the plate of V4, which is cut off at this time.

(e) In the dynamic state, V4 section 1-2-3 produces a negative 60-microsecond gate which is coupled through the delay line capacitor in Z1 to V3B. This negative gate cuts off V3B, causing the voltage across R41 to drop to 0 volts. Simultaneously, the delay line capacitor begins discharging to the low-plate voltage of V4 section 1-2-3 through Z1, R21, the +250-volt supply, ground, and V4 section 1-2-3. Adjustment of R21 varies the discharge time by ± 1 microsecond. Approximately 23.5 microseconds later, the plate of V3B rises slightly above ground potential. Since the plate of V3B is now positive with respect to the cathode, V3B conducts. The voltage across R41 again rises to +2.5 volts, producing the trailing edge of the 23.5-microsecond negative gate. Since V3B cuts on and off sharply, the output gate is square-sided, thus lending itself easily to differentiation. The conduction of V3B clamps its plate to +2.5 volts, preventing any further discharge of the delay line capacitor. Therefore, this capacitor charges from +2.5 volts to the low-plate voltage of section 1-2-3 of V4. When the trailing edge of the 60-microsecond gate passes, the plate of section 1-2-3 of V4 rises again to +250 volts. The delay line capacitor continues charging to this voltage, re-establishing the quiescent condition of the circuit. A temperature-regulating resistive element is mounted in Z1 and re-

turned through terminals 4 and 5 to 6.3 volts ac. Its heat dissipation varies with temperature, thus effectively counteracting any temperature changes within Z1. Consequently, the resistance of the resistors within Z1 does not fluctuate with temperature changes, and the period of delay does not vary from 23.5 microseconds. Relay K1, which operates only when the synchronizer is used with the target tracking radar system, is energized when the AAR is selected. When relay K1 is energized, AAR SYNC DELAY variable resistor R51 is switched in series with R21, and R52 is switched out of the plate circuit. This action changes the delay period from 23.5 microseconds to approximately 23.5 microseconds. This delay can be varied around 23.5 microseconds by adjusting R51. This adjustment is set to provide correct gate adjustment for use with the AAR to compensate for the pulse repetition rate change.

(f) The negative 23.5-microsecond gate from V3B is coupled directly to the grid of pulse delay amplifier V5A. V5A is section 1-2-3 of V5 and V5B is section 6-7-8 of V5. An amplified positive gate is differentiated by capacitor C8 and resistor R26, producing negative and positive pips at the grid of pulse delay amplifier V5B. The pips correspond in time to the leading and trailing edges of the 23.5-microsecond gate.

(g) With no signal applied, V5B is cut off by −25 volts applied to the grid by the voltage divider consisting of resistors R27 and R28 from ground to the −250-volt supply. Capacitor C9 stabilizes this potential. The positive pip from V5A raises the grid of V5B above cutoff, and V5B conducts. An amplified negative pip is developed

across primary winding 6-5 of blocking oscillator transformer T2.

(h) Since a blocking oscillator transformer is designed to pass narrow pulses, its high-frequency response is good. Conversely, its low-frequency response is poor. Therefore, T2 passes the high-frequency components in the pips and attenuates the low-frequency components. This action effectively improves the shape of the pips. The pips are coupled through secondary winding 1-2 and tertiary winding 3-4 of T2 to the grid of sync pulse blocking oscillator V2B.

(i) Blocking oscillator V2B is normally cut off by approximately –25 volts bias between the grid and cathode established by the voltage divider consisting of resistors R32, R33, and R30 connected between ground and the –250-volt supply. Since V2B is cut off, the leading negative pip has no effect. However, the trailing positive pip triggers V2B into conduction 23.5 microseconds after preknock time. The operation of V2B is similar to that of V2A, as described in (1) (b) above. Blocking oscillator V2B produces a positive 40-volt, 0.15-microsecond sync pulse, which is developed across cathode resistor R30 and coupled directly to connector J4 and through C15 to sync pulse amplifier V7A. Capacitor C10 and resistor R29 provide plate decoupling for V5B, V2B, V7A, and V7B. Resistor R8 limits any grid current in V7A.

(5) *Transmitter sync pulse circuit.*

(a) Sync pulse amplifier V7A is normally cut off by –30 volts applied to the grid by the voltage divider composed of resistors R7 and R9 from ground to the –250-volt supply. V7A is section 1-2-3 of V7, and V7B is section 6-7-9 of V7. Capacitor C16 stabilizes this potential. When the sync pulse trig-

gers V7A into conduction, an amplified negative pulse is developed across winding 1-2 of blocking oscillator transformer T4. This pulse is induced and inverted in winding 3-4 of T4 and applied as a positive pulse to the grid of transmitter sync pulse blocking oscillator V7B.

(b) Blocking oscillator V7B is normally cut off by –25 volts applied to the grid by the voltage divider consisting of resistor R45 and R46 from ground to the –250-volt supply. The positive pulse raises the grid above cutoff, and V7B conducts for 0.15 microsecond. The operation of V7B is similar to V2A, as described in (1) (b) above. A positive 40-volt, 0.15-microsecond transmitter sync pulse is produced across cathode resistor R49 and coupled to connector J5.

(6) *Relay K1.* Relay K1 is operated in the synchronizer in the target radar control console when AAR is selected. Contacts of K1 are used to change the free running frequency of V2A. Contacts of K1 also select the appropriate variable resistor, R21 or R51, for V3B.

16 (U). MTI Video Amplifier 8513331

a. General.

(1) The largest portion of the circuitry on the MTI video amplifier chassis is devoted to development of the AGC voltage which governs the gain of the delay video channel so that it will equal the gain of the nondelay video channel. Without this balance of gain, MTI operation would not be possible since a larger level of gain, in either channel, would then prevail as output. This AGC voltage is derived from the residue of the test pulse. The original test pulse is a 6-volt, 7-microsecond, positive pulse which is generated in the acquisition-track synchronizer and initially is applied to the carrier oscillator. In the

carrier oscillator, the test pulse is injected between the preknock pulse and MTI video pulse. All three pulses then modulate the 15-megacycle RF carrier. The test pulse is carried through both the delay and nondelay channels. If the inverted facsimiles of the pulses are equal, they cancel by summation in the MTI synchronizer. However, if the amplitudes of the test pulse differ in the two channels, the algebraic difference appears as residue which is then detected and amplified in the MTI video amplifier and returned to the delay amplifier as AGC to achieve balanced gain between the delay video and nondelay video channels.

(2) The remainder of the circuitry in the video amplifier chassis rectifies the combined phase 1 and phase 2 moving-target video to produce a composite output of negatively polarized MTI video pulses. This signal is necessary for final mixing with azimuth and range marks in the external video and mark mixer.

b. *Detailed Theory.*

(1) *MTI video circuit.*

(a) The MTI video circuit provides advantages of push-pull amplification for residue voltages emanating from the external MTI synchronizer. The push-pull output is connected to a full-wave crystal rectifier to produce a single-ended negative output. The phase 1 and phase 2 residue video output from the MTI synchronizer is applied to the MTI video amplifier through connectors J2 and J3, respectively (fig. 40, TM 9-1430-257-20). Phase 1 is coupled through capacitor C2 to phase 2 amplifier V1B. Resistors R1 and R2 are the respective grid return resistors. Resistor R3 is the common cathode resistor for V1A and V1B. When a positive signal appears at the grid of V1A, driving V1A farther into conduction, more current flows through R3 creating a more positive voltage at the cathodes of V1A and V1B. This in turn decreases current through V1B which aids the push-pull operation of V1A and V1B.

(b) Assume that a positive signal exists on the grid of V1A. An increase in current through resistor R4 produces a negative-going voltage coupled from the plate of V1A through capacitor C3 to the MTI video full-wave rectifier composed of crystal diodes CR1 through CR4. Diode CR2 blocks because the cathode is at a higher level than the plate. However, the negative-going voltage from V1A causes CR1 to conduct through MTI VIDEO variable resistor R10 toward +250 volts. The amount of signal required is picked off by the brush arm of R10 and applied through blocking capacitor C7 and connector J6 to the external switching and mixer unit. While the output from V1A goes negative, the output from V1B goes positive. Diode CR4 blocks but diode CR3 conducts, and the positive signal from V1B is dissipated in resistor R11. When the phase of the input signal reverses, the counterpart components perform reciprocal functions, i.e., while the output from V1B goes negative, the output from V1A goes positive. Diodes CR1 and CR3 block, but diodes CR2 and CR4 conduct; the positive signal from V1A is dissipated in R11, and the negative signal from V1B is developed across R10. In either case, the outputs developed across R10 are negative MTI video pulses.

(2) *Test video circuit.*

(a) The test video circuit is part of a built-in test facility used for performing MTI system adjustment procedures. The signal developed

in this circuit is used for monitoring purposes while making the required adjustments.

(b) All residue components developed across resistor R5 are applied through coupling capacitor C4 to the grid of test video cathode follower V2A. This signal is developed across resistor R6, and since the cathode follows the grid, the output is coupled from the junction of resistors R7 and R8 of the voltage divider composed of resistors R9, R8, and R7 through connector J4 to the external MTI oscilloscope.

(3) *AGC circuit.*

(a) The AGC circuit is devoted to development of the MTI system AGC voltage. It consists of cascaded low-gain amplifier stages V3A, V3B, V4A, and V4B, followed by gate amplifiers V5 and V6 and used to detect test pulse residue at test

pulse time and to eliminate the video residue. Accurate discrimination of test residue is accomplished by means of bistable multivibrator V7A and V7B which "flips" with change in phase and constantly drifts along with changes in residue amplitude. The output is applied through AGC cathode follower V2B which isolates the multivibrator from the external load.

(b) Any residue present, due to the difference in test pulses, is developed across V1B plate load resistor R5 and coupled through capacitor C6 and isolating resistor R12 to cathode follower V3A. The grid of V3A is at approximately 21 volts positive potential due to bias developed between +150 volts and ground by the voltage divider consisting of resistors R15 and R16. This bias is applied to V3A through resistors R18 and R12. Resistors R12 and R18 form a divider which prevents the signal on the grid of V3A from appearing on the grid of V3B since it is necessary that the grid of amplifier V3B be maintained at a constant dc voltage.

(c) The phase 2 signal which feeds V3A is the residue of the test and video pulses from the cancellation point in the MTI synchronizer and can be either positive or negative depending upon the relative amount of signal difference in the delay and nondelay channels. Assume that the signal on the grid of V3A is positive. The cathode follows the grid, and the signal developed across resistor R13 is cathode-coupled to amplifier V3B. Since the grid of V3B is positively biased, the grid draws current and charges capacitor C9. Should noise transients in cathode signal exceed the positive grid bias, V3B swings toward cutoff, and clipping of the noise level occurs.

(d) The signal developed across plate load resistor R14 follows the cathode and is coupled through capacitor C8 and isolating resistor R19 to the grid of push-pull cathode coupled amplifier V4A.

(e) The grid of V4A is also kept at approximately 21 volts positive bias through resistor R17. Amplifier V4A is the inverter half of V4 and both V4A and push pull cathode coupled amplifier V4B are mutually coupled through the cathodes connected to bias resistor R20. The grid of V4B is also held at approximately 21 volts positive potential by the voltage developed across R16. The positive signal applied to V4A is inverted and developed across resistor R21 and coupled through capacitor C10 and limiting resistor R23 to the control grid of gate amplifier V5. In a similar manner, the positive signal applied to V4B is developed across R22 and coupled through capacitor C11 and limiting resistor R26 to the control grid of gate amplifier V6. The grids of V5 and V6 are returned through resistors R24 and R25 to −5 volts bias developed across the voltage divider consisting of resistors R27 and R28 between 250 volts and ground. The inputs to the control grids of V5 and V6 normally are low amplitude video signals. Since these tubes are biased near cutoff, all low level positive and negative signals are amplified. The suppressor grids are cut off by the −12 volts bias developed across the voltage divider consisting of resistors R30 and R31 between −250 volts and ground.

(f) Amplifiers V5 and V6 are pentodes used for gating purposes in this circuit, and the positive video and test pulse, assumed as the input to V3A in (c) above, produces a negative residue signal on the control grid of V5.

(g) The positive test pulse coming directly from the acquisition-track synchronizer is applied through connector J1, resistor R29, and capacitor C12 to the suppressor grids of V5 and V6 (fig. 5).

CONFIDENTIAL

Capacitor C13 bypasses transient voltages to ground. This test pulse and the test pulse residue arrive at V5 and V6 at the same time. The video residue is also applied to the control grids of V5 and V6 since it is present at the reference point from which the test pulse residue is taken, i.e., the junction of R5 and the plate of V1B. Elimination of the video residue is necessary to prevent interference with generation of the AGC voltage.

(h) The video residue occurs along the base line at an indefinite time interval (n-microseconds) later than the test pulse residue, depending upon the range of the target. Therefore, the
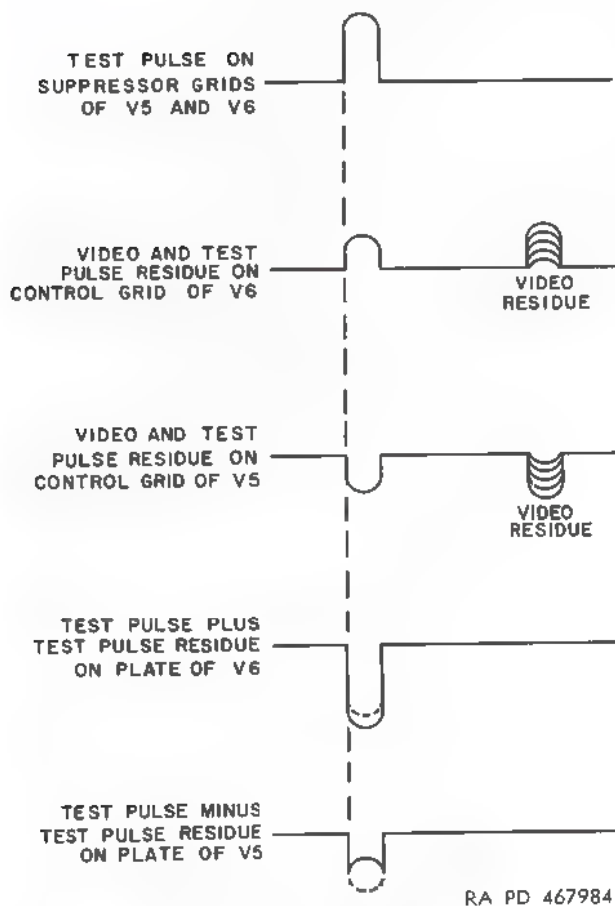
test pulses are passed, but the video residue does not pass the gating stage since no positive gating voltage is present on the suppressor grids which are cut off by the −12-volt bias during the time video residue appears on the control grid. The only output from the gating stage may be the test pulse plus or minus the test pulse residue. With an assumed positive test pulse residue signal on the control grid of V6 and a full test pulse applied to the suppressor grid of V6, the output from V6 is the full test pulse plus the test pulse residue. Then the output from V5 can only be the full test pulse minus the test pulse residue.

(i) The outputs of V5 and V6 (fig. 40, TM 9–1430–257 20) control bistable multivibrator V7A and V7B. The plate of V5 is connected to the plate of V7A, and resistor R36 is the common plate load. The same relationship exists between V6 and V7B where R37 is the common plate load resistor. Because the plate of V7A is coupled through resistor R34 and capacitor C14 to the grid of V7B, and the plate of V7B is coupled through resistor R35 and capacitor C15 to the grid of V7A, the output of V5 actually controls V7B, and the output of V6 controls V7A.

(j) With a small input signal, the limited amplification capabilities of V3A, V3B, V4A, and V4B produce a small difference of output between V5 and V6. By regulating the multivibrator from these two points, control that is sensitive to the small changes is obtained. When the output from V5 has less amplitude than the output from V6, amplifier V6 lowers the voltage on the plate of V7B and tends to drive V7A toward cutoff. The negative-going voltage from V6 is coupled from the plate of V7B through C15 and R35 to the grid of V7A and causes V7A to go toward cutoff. At the same instant, the

Figure 5. (U) Test pulse residue gating waveforms.

RA PD 467984

CONFIDENTIAL

less negative output from V5 and the positive-going voltage from the plate of V7A are coupled through C14 and R34 to the grid of V7B. Multivibrator V7B is driven into heavier conduction and the resultant drop from its plate is applied to the grid of V7A, thus driving V7A farther toward cutoff. This initial condition starts the multivibrator action and, because of the regenerative nature of the circuit, this action will continue. This action is gradual and follows the amplitude of the input. If the output polarities of V5 and V6 do not interchange during successive cycles of the system operation, there will be no change in the polarity of the output of V7A and V7B.

(k) With V7A cutting off, its plate voltage rises and produces the leading edge of the waveform slope. The output from V7A is applied through resistors R38 and R40 to the control grid of AGC cathode follower V2B. Resistors R36, R38, and R39 form a voltage divider between +150 volts and −250 volts. Resistor R40 and capacitor C16 integrate the multivibrator output before it is applied to the control grid of V2B. Resistor R40 also limits the grid current of V2B since during quiescent state the junction of R39 and R40 is at +7 volts. The output from V2B rises with the output from V7A. This signal is developed across cathode resistor R42 and maintained below zero reference level by clamping diode CR5. If the output attempts to go positive, the diode conducts and clamps the signal at ground. Resistor R43 protects CR5 in case the −250-volt power supply fails.

(l) The AGC voltage derived from the test pulse residue is negative or more negative only. The output voltage is continually seeking equilibrium since the multivibrator has no neutral state. The rise in the slope of the output

waveform is produced by V7A voltage rise, and the fall of the slope is produced by a rise in V7B voltage output. However, any change in the output of the AGC circuit is relatively smooth, tending to oscillate slowly about the equilibrium point. This output is applied through connector J5 to the external delay amplifier chassis.

17. Switching and Mixer Unit 8513387

a. General. The switching and mixer unit generates voltages that establish and control the boundaries of an MTI sector on the PPI presentation of the acquisition radar system.

b. Detailed Theory. The switching and mixer unit (fig. 38, TM 9-1430-257-20) combines the preknock pulse, sector angle resolver voltage, bypass video, MTI video, and IFF video to produce a composite output to be utilized by the external video and mark mixer. The above signals are mixed to obtain azimuth and range components for sector presentation of MTI on the acquisition presentation system, to obtain a normal radial sweep with a combination of MTI and bypass video, or to obtain a normal radial sweep with bypass video only. The presentation obtained is selected by MTI—MODE switch S18 located on the acquisition control-indicator (fig. 21, TM 9-1430-257-20). The operation of the switching and mixer unit is explained in (1) through (3) below in terms of settings of MTI—MODE switch S18 in the SECTOR position, then the 360° position, and finally in the OFF position.

(1) *Circuit operation—MTI—MODE switch S18 in SECTOR position.*

(*a*) The functions of clipper amplifier V1A and 4-kc detector V1B (fig. 38, TM 9-1430-257-20) can be utilized only in the SECTOR position of MTI—MODE switch S18 (fig. 8). Amplifier V1A and detector V1B aid in the development of the MTI sector on the PPI presentation. Since the output of V1B is grounded through connector P1-1 in the OFF and 360° positions of S18, an MTI sector cannot be generated in these switch positions. The output

CONFIDENTIAL

from an external sector angle resolver is applied through connector P2-9 to terminal 1 of 4 KC ADJ variable resistor R1. The output from the sector angle resolver is a 4-kc signal (A, fig. 6) modulated by a rotation component which represents the azimuth rate of the acquisition antenna. In order to get one null per revolution, the sector resolver output is mixed with a 4-kc reference carrier (B, fig. 6) that is applied through P2-7 to terminal 3 of R1. The addition of in-phase components and the subtraction of out-of-phase components produce a waveform as indicated by C, figure 6.

(b) Variable resistor R1 (fig. 38, TM 9-1430-257-20) is set to obtain minimum ac voltage at test point J6 during checks and adjustments. The selected reference point from the angle resolver yields a single null point for one antenna revolution, which later serves as a gate center for establishing a sector on the PPI presentation. The composite signal (C, fig. 6) is picked off by the brush arm of R1 (fig. 38, TM 9-1430-257 20) and applied through the isolation circuit consisting of capacitor C1 and resistor R9 to the control grid of clipper amplifier V1A. The isolation circuit prevents the 4.6-volt dc bias, developed across R2 and R3 between ground and −250 volts, from entering the 4-kc oscillator and the sector angle resolver. Since the −4.6-volt bias maintains conduction of V1A slightly above cutoff, grid clipping of the negative portion of the input voltage occurs. Only the positive halves of the composite signal from R1 pass through V1A. These are inverted and amplified in V1A to produce a waveform as shown in D, figure 6.

(c) The output of V1A (fig. 38, TM 9-1430-257 20) is coupled through capacitor C2 to the cathode of V1B. Since any positive voltage on the cathode cuts off V1B, the cutoff level set by means of SECTOR WIDTH variable resistor R6 governs the duration of V1B conduction. Electron current flow from −250 volts through resistors R5, R6, and R7 to +150 volts produces a dc level that is variable from −14 volts to +68 volts. A preset value of voltage in this range provides a dc level for the voltage on C2. Signals at the cathode of V1B are developed across R8, part of R6, and R5. These signals are also coupled through capacitor C3 to J6.

(d) Assume that this level (zero dc line) is set 2 volts below the clipped level from V1A as shown in E, figure 6. All positive portions of the rotation voltage will be clipped by V1B cutoff, and all negative portions will pass from cathode to plate to ground through the network consisting of resistor R10 and capacitor C4. Electron current flow through R10 produces a negative voltage at the junction of R10 and the plate of V1B. When this voltage is applied to the suppressor grid of pre-knock selector V2, it prevents any con duction through V2. Since R6 sets the level for V1B conduction, it establishes the sector width. This sector width is indicated by the dotted lines projected upward from the zero dc line as shown in E, F, and G, figure 6. The sector width is represented by a gate (H, fig. 6) whose time interval exists between V1B cutoff and return to conduction. The gate is used later to produce the MTI sector.

(e) When R6 sets the zero dc line 4 volts below the clipped level from V1A as shown in F, figure 6, V1B is cut off for a longer interval, thus producing a longer gate. This is extended further when the zero dc line is set 6 volts below the clipped level from V1A as shown in G, figure 6. Then the arc segment of the sector increases in

CONFIDENTIAL

ONE ROTATION
OF ANTENNA

A 4KC FROM
SECTOR ANGLE
RESOLVER

IN θ   180°   OUT OF θ   IN θ   180°   OUT OF θ   IN θ

B 4KC REFERENCE

X

C OUTPUT OF RI   Y   Y

ZERO DC
LINE

D OUTPUT OF VIA   Y   Y

PPI SECTOR   X   PPI SECTOR

+2V

E INPUT TO VIB   0

PPI SECTOR

+4V

F INPUT TO VIB   0

PPI SECTOR

+6V

G INPUT TO VIB   0

ZERO DC
LINE

H OUTPUT OF VIB   Y   Y

X

J PREKNOCK IN

K OUTPUT OF V2

CENTER
OF SECTOR

NO MTI
DURING
THIS SECTOR

WIDTH OF
SECTOR

RA PD 467985
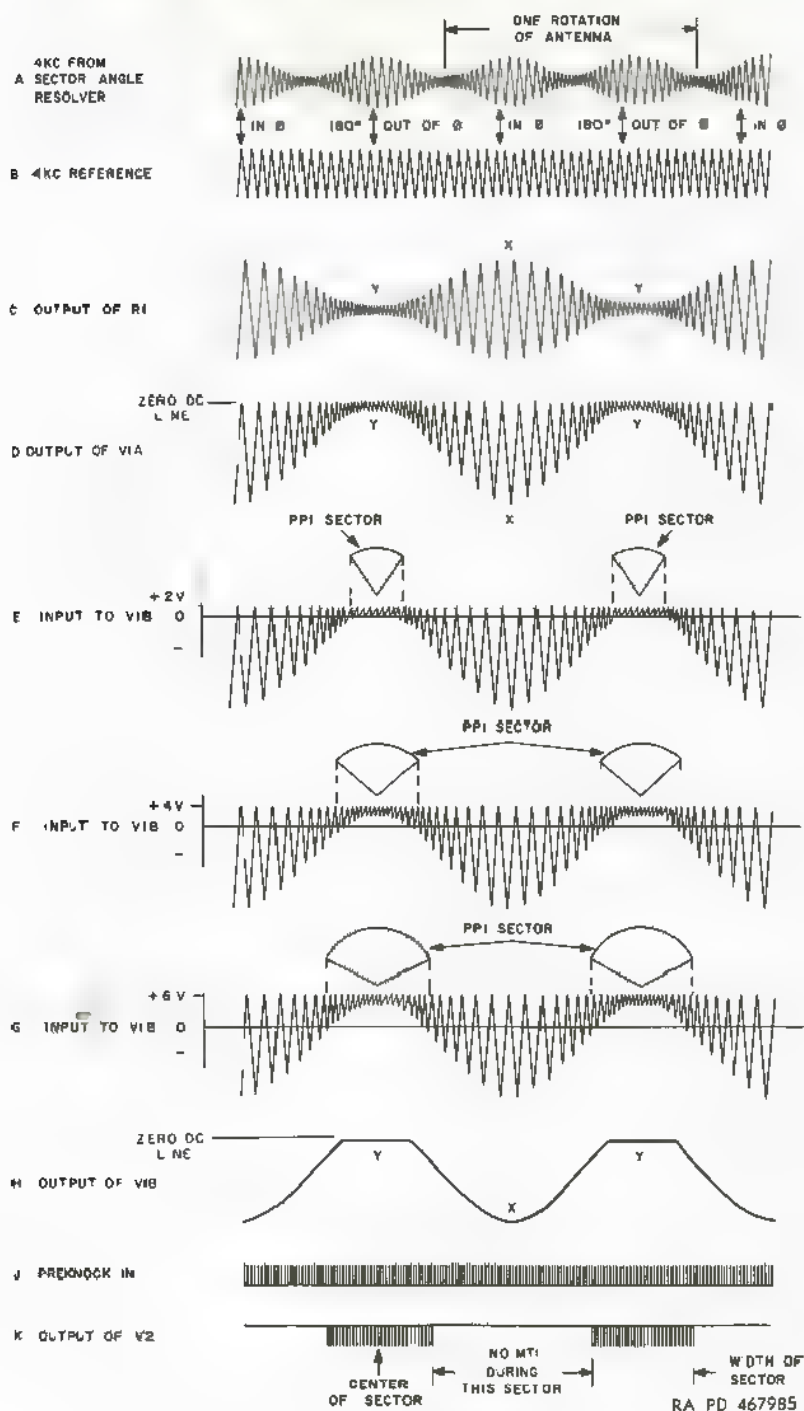
Figure 6 (U) MTI sector selection waveforms.

length and a wider sector is presented on the PPI presentation. During V1B conduction, the 4-kc component is filtered out in the R10, C4 network, and the output appears as represented by the waveforms shown in H, figure 6.

(f) During SECTOR operation of the switching and mixer unit (fig. 38, TM 9-1430-257-20), preknock selector V2 acts as a coincidence tube. The suppressor grid is returned to ground through the R10, C4 circuit instead of being grounded directly to the cathode of V2. With the suppressor connected in this manner, the suppressor grid current in V2 can increase to a level sufficient to cut off V2. In addition, the control grid of V2 is biased at -14.75 volts by a voltage divider consisting of R14 and R15 between ground and -250 volts, thus providing two grid elements in V2, either of which can maintain V2 at cutoff. When the output from V1B is applied to the suppressor grid of V2, the maximum amplitude Y of the gate shown in H, figure 6 effectively grounds the suppressor grid. Then, for the duration of the gate, V2 is held below cutoff only by the bias on the control grid.

(g) Preknock pulses (J, fig. 6) are applied through connector J1 and coupled through capacitor C5 to the control grid of V2. The presence of a gate from V1B on the suppressor grid of V2, in coincidence with preknock pulses on the control grid, drives V2 above cutoff. Then a series of preknock pulses is passed through V2 for a time interval equal to the width of the sector adjustment. The negative-going pulses are developed across resistor R16. The output, shown in K, figure 6, is coupled through capacitor C6 to the cathode of range phantastron diode 1 V3A.

(h) The generation of range in the MTI sector is performed by V3A, range phantastron diode 2 V3B, range phan-

tastron B4, plus associated circuit components. The output from V2 to V3A is shown in expanded form in A, figure 7 to facilitate explanation of occurrences per each preknock pulse. Between preknock pulses, the cathode of V3A (fig. 8) is at $+35$ volts set by the drop across the resistance of the voltage divider consisting of resistors R17, R18, and R19. The plate voltage of V3A is set by the voltage divider consisting of resistor R21, the cathode-to-grid resistance of V4, and resistor R20. The drop through this circuit maintains the plate potential of V3A below that of the cathode, and consequently V3A is cut off. Capacitor C7 bypasses R18 and maintains the voltage drop across R18 constant. This voltage is the suppressor grid voltage for V4.

(i) Between pulses, the positive control grid of V4 causes screen current flow toward the junction of resistor R25 with resistors R23 and R24, which causes a voltage drop across R23 and R24. Current flows from ground through resistor R13, part of SECTOR RANGE variable resistor R11, connector P1-3, switch S18A-3 and 4, P1-7 and 9, TEST switch S1, P1-11, range phantastron diode 2 V3B, and resistor R22 toward $+250$ volts. This lowers the voltage at the junction of the plates of V3B and V4. Due to screen current through R21, the cathode of V4 is near the plate potential, and therefore plate current is cut off. Capacitor C9 charges and stabilizes the potential between the plate and control grid of V4. Consider this condition the pretrigger or quiescent state.

(j) A negative preknock pulse is coupled from V2 through C6 to the cathode of V3A. Diode V3A conducts and lowers the potential on the control grid of V4 which then cuts off screen current and raises the screen voltage. This instantaneous rise is the beginning of the

range gate for MTI presentation and is shown as the leading edge of the square wave in B, figure 7.

(k) On termination of the preknock pulse, the suppressor grid of V4 (fig. 8) receives a positive pulse from the junction of R18 and R19, and the plate of V4 starts to conduct. Now the potential between the plate and control grid becomes unstabilized, and C9 begins to discharge through R20 toward +250 volts. Electron current flow from C9 through R20 causes the control grid to go negative and maintains

the screen grid cut off. Plate current increases and drops the plate voltage to a point where V3B cuts off. Then capacitor C19 charges to the voltage set by R11.

(l) After the preknock pulse has expired, the cathode of V3A returns to +35 volts and the control grid of V4 returns to its quiescent state. Increase in screen current reduces plate current and the plate potential of V4 starts to rise. This rise in plate potential continues until it is higher than the charge on C19 allowing V3B to begin conduct-
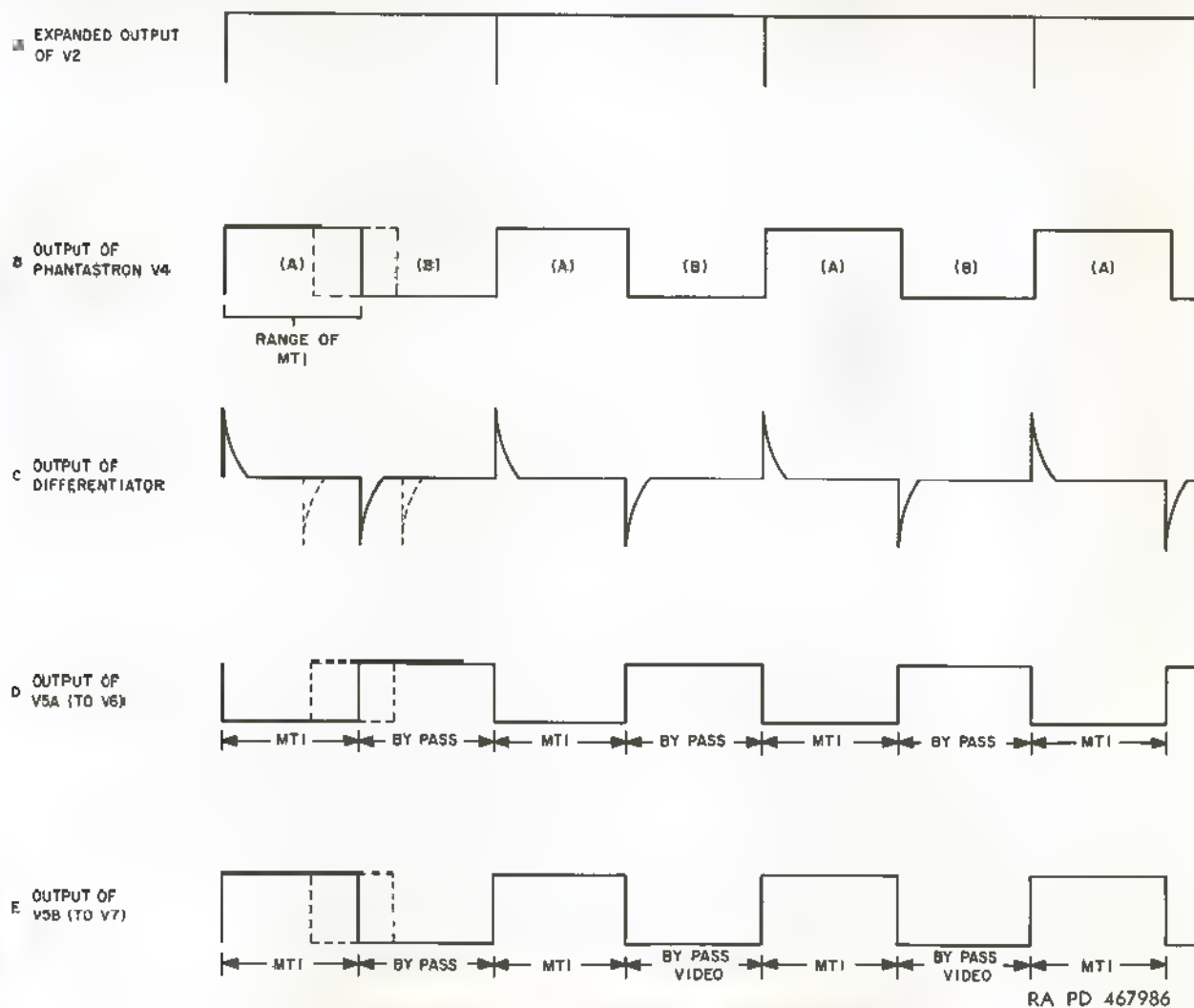
Figure 7. (U) *MTI sector selection expanded waveforms.*

RA PD 467986

ing. Capacitor C19 discharges rapidly through V3B and the drop across R22 cuts off the plate of V4. Simultaneously, the screen arrives at full conduction indicated by the trailing edge of area (A) shown in B, figure 7. Area (A) is the complete interval between screen rise and fall and establishes the time base for the range of the MTI This interval is controlled by the setting of R11. The rise and fall of screen voltage across capacitor C8 and resistor R29 (fig. 38, TM 9-1430-257-20) differentiates the screen square wave as shown in C, figure 7. This differentiated voltage is applied to the control grid of gating multivibrator V5A.

(m) Consider the case when the positive pulse of the differentiated input to V5A (fig. 38, TM 9-1430-257-20) causes V5A to conduct. Electron current flowing from −250 volts, through cathode resistor R28, V5A, and plate load resistors R33 and R35, causes a voltage drop (D, fig. 7) which is directly applied to the suppressor grid of bypass video gate V6. This voltage is also applied through resistor R31 and capacitor C12 to the control grid of gating multivibrator V5B. Reduction of current through V5B produces a positive-going voltage across plate load resistors R34 and R36. This signal (E, fig. 7) is applied to the suppressor grid of MTI video gate V7.

Figure 8. (U) *MTI—MODE switch S18—sector position—partial schematic diagram.*
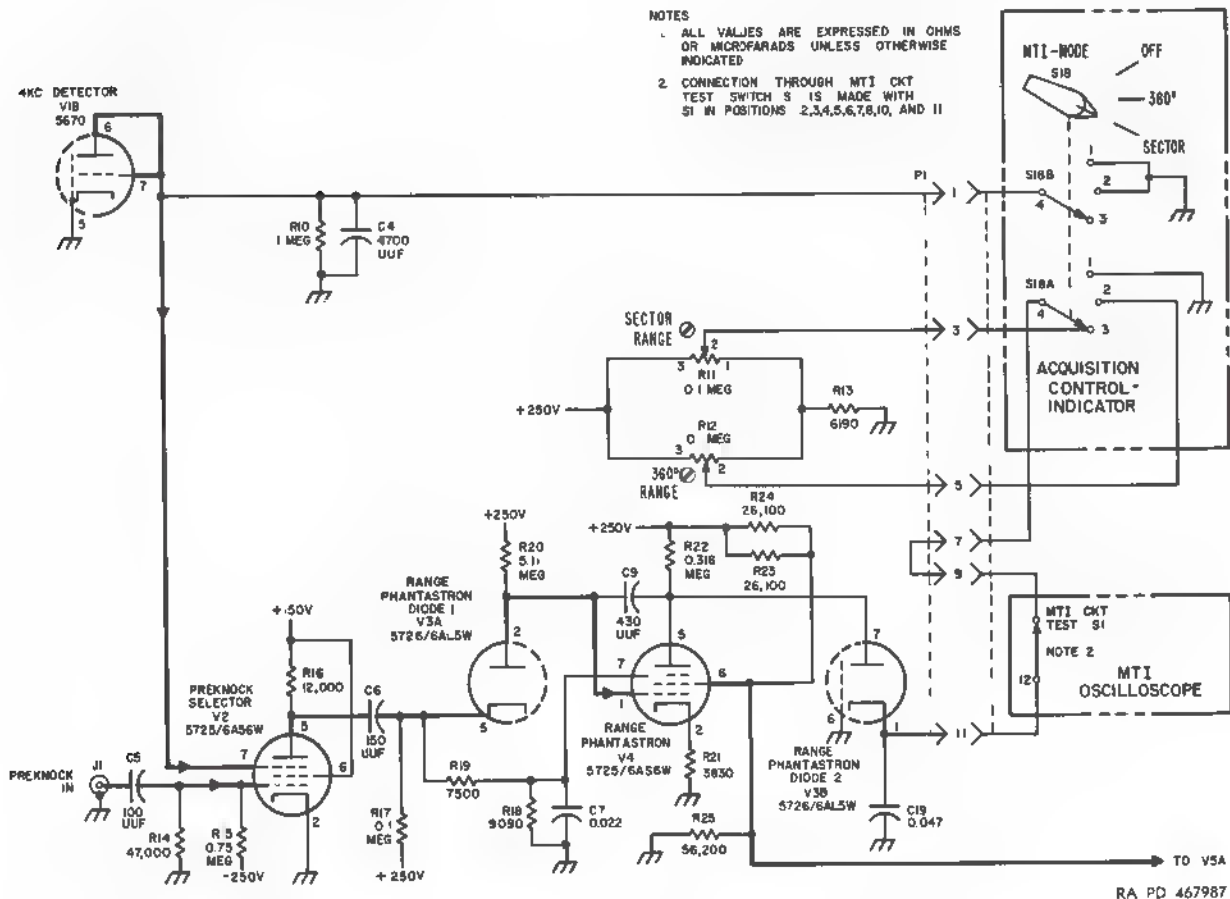
(n) When the MTI video signal, applied through connector J3 to the control grid of V7, is in coincidence with the positive-going gate from V5B, gate V7 conducts and passes the MTI video signal. This is indicated by the positive area (MTI) in E, figure 7. At the same instant, bypass video, applied through connector J2, BY PASS GAIN variable resistor R27, and coupling capacitor C10 to the control grid of V6, is blocked due to the negative-going output from V5A. This is indicated by the negative area of the signal (bypass video) in E, figure 7. Variable resistor R27 adjusts the input from J2 to equal the amplitude of MTI video at J3. Resistor R26 is used to protect the external noise-measuring equipment.

(o) On termination of the range gate from V4 (B, fig. 7), a differentiated pulse of negative polarity (C, fig. 7) is applied to the control grid of V5A. Then the operation of the gating multivibrator is opposite to that just discussed. Now bypass video is obtained from V6 (fig. 38, TM 9–1430–257–20) while MTI video is cut off by V7. Crystal clipper CR1, bypassed by resistor R39, is symmetrical to clipper CR2, bypassed by resistor R42. Each removes the positive portion from the bypass video and the MTI video inputs, respectively. This clipping is necessary to prevent pretriggering of the respective gate tubes by positive pulses in the bypass video and the MTI video.

(p) The plates of V6 and V7 are connected and have a common load resistor, R43. A single output of either MTI video or bypass video is developed across R43. The bias on the cathodes of V6 and V7 is dropped through resistors R38 and R40, respectively, and can be balanced between V6 and V7 by adjusting SW BAL variable resistor R37. This adjustment insures that there is no change in dc level in the output from V6 and V7 resulting from switching from one tube to the other. During switching, if one tube does not resume conduction at the same rate that the other tube ceases to conduct, a transient spike will develop. Gate level variable capacitor C15, connected to the control grid of V5B, and capacitor C14 shunt the switching transient to ground and thus eliminate the spike. Variable capacitor C15 is adjustable to insure optimum shunting of the spike.

(q) Note that with MTI MODE switch S18 (fig. 21, TM 9–1430–257–20) in the SECTOR or OFF position, C14 (fig. 38, TM 9–1430–257–20) is not grounded but is effectively out of the circuit. In these two positions, the transient spike will appear on the PPI where it is used to mark the limit of the MTI range.

(r) Either a bypass video or MTI video signal is coupled from the plates of V6 and V7 through capacitor C17 to the grid of video and IFF mixer V8A. When necessary during tactical operations, an IFF signal is applied through connector J5, through the junction of terminating resistor R50, and through coupling capacitor C18 to the grid of video and IFF mixer V8B. The input to V8A is developed across resistor R45; the input to V8B is developed across R49. If either of these inputs exceeds −4 volts, they are clamped to this level by clamping diodes CR3 and CR4, respectively. This clamping voltage is established by the voltage divider consisting of resistors R46 and R47 connected to the −250 volt supply. The prevailing video signal and the IFF signal are mixed in the paralleled plates of V8A and V8B and applied through connector J4 to the external video and mark mixer.

(2) *Circuit operation—MTI—MODE switch S18 in 360° position.*

(a) In the 360° mode of operation, MTI

CONFIDENTIAL

sector operation is eliminated and only normal PPI coverage of bypass video and moving-target video is presented. The suppressor grid of preknock selector V2 is grounded through connector P1–1 and MTI—MODE switch S18 (fig. 8). The output from the sector angle resolver has no effect on V2 because the output of V1B is grounded by the same path as the suppressor grid of V2. Since V2 is now connected as a pentode, all preknock pulses pass through to V3A.

(b) The remainder of the circuitry operates in an identical manner to SECTOR operation, as described in (1) above, with the following exceptions: The range of the radial sweep is adjusted by means of 360° RANGE variable resistor R12. The electron current flows from ground through resistors R13 and R12, through MTI—MODE switch S18 and MTI CKT TEST switch S1 in the external MTI oscilloscope to the cathode of V3B. Assume that variable resistor R12 is adjusted to increase the recovery time of the plate of V4. As the brush arm of R12 is advanced toward +250 volts, the charge level of capacitor C19 is extended, the plate of V4 reaches the charge level after a longer period, and the screen conducts for a longer period. Therefore, the MTI time is reduced and the duration of the bypass time is extended as indicated by the dotted lines (B, C, D, and E, fig. 7) on the left closest to the initial preknock pulse.

(c) The opposite condition exists when the brush arm of R12 (fig. 8) is advanced toward ground. The charge level of C19 is reduced, the plate of V4 reaches the charge level after a shorter period, and the screen conducts for a shorter period. Therefore, the MTI time is increased and the duration of the bypass time is reduced as indicated by the dotted lines (B, C, D, and E, fig. 7)

on the right farthest from the preknock pulse. The setting of R12 (fig. 8) determines the duration of the gate from V4 and consequently the division of PPI presentation between moving-target video and bypass video.

(3) *Circuit operation—MTI—MODE switch S18 in OFF position.*

(a) During the OFF position of MTI—MODE switch S18, moving-target video is eliminated and a normal 6,400-mil sweep of bypass video is presented. As during 360° operation, described in (2) above, the sector angle resolver has no effect since the suppressor grid of V2 is grounded through connector P1–1 and switch S18. In the OFF position of S18, the cathode of V3B is also grounded through MTI CKT TEST switch S1 in the MTI oscilloscope, thus disabling the charging capabilities of capacitor C19. Since range control is disconnected, V3B conducts at all times and the constant voltage drop across resistor R22 causes the plate voltage of V4 to be very low and renders the plate ineffective. Phantastron V4 is thus converted to an amplifier (using the screen grid as a plate) instead of a phantastron.

(b) The preknock input to V2 (A, fig. 9) is similar to that used in the SECTOR and 360° modes of operation. However, after the negative preknock input to V4 has expired (B, fig. 9), the control grid returns to a positive potential determined by the voltage dropped across resistor R20, and screen grid current through V4 is resumed between preknock pulses. An inverted facsimile (C, fig. 9) of the V4 input is applied from the screen grid to differentiating network R29 and C8 (fig. 38, TM 9–1430-257–20). The leading and trailing edges of the positive pulses are differentiated by R29 and C8 producing positive and negative differentiated pulses (D, fig. 9) at the grid of V5A.

32

CONFIDENTIAL

A   PREKNOCK INPUT TO V2

B   INPUT TO V4

C   OUTPUT FROM V4

D   INPUT TO V5B

BYPASS VIDEO   BYPASS VIDEO
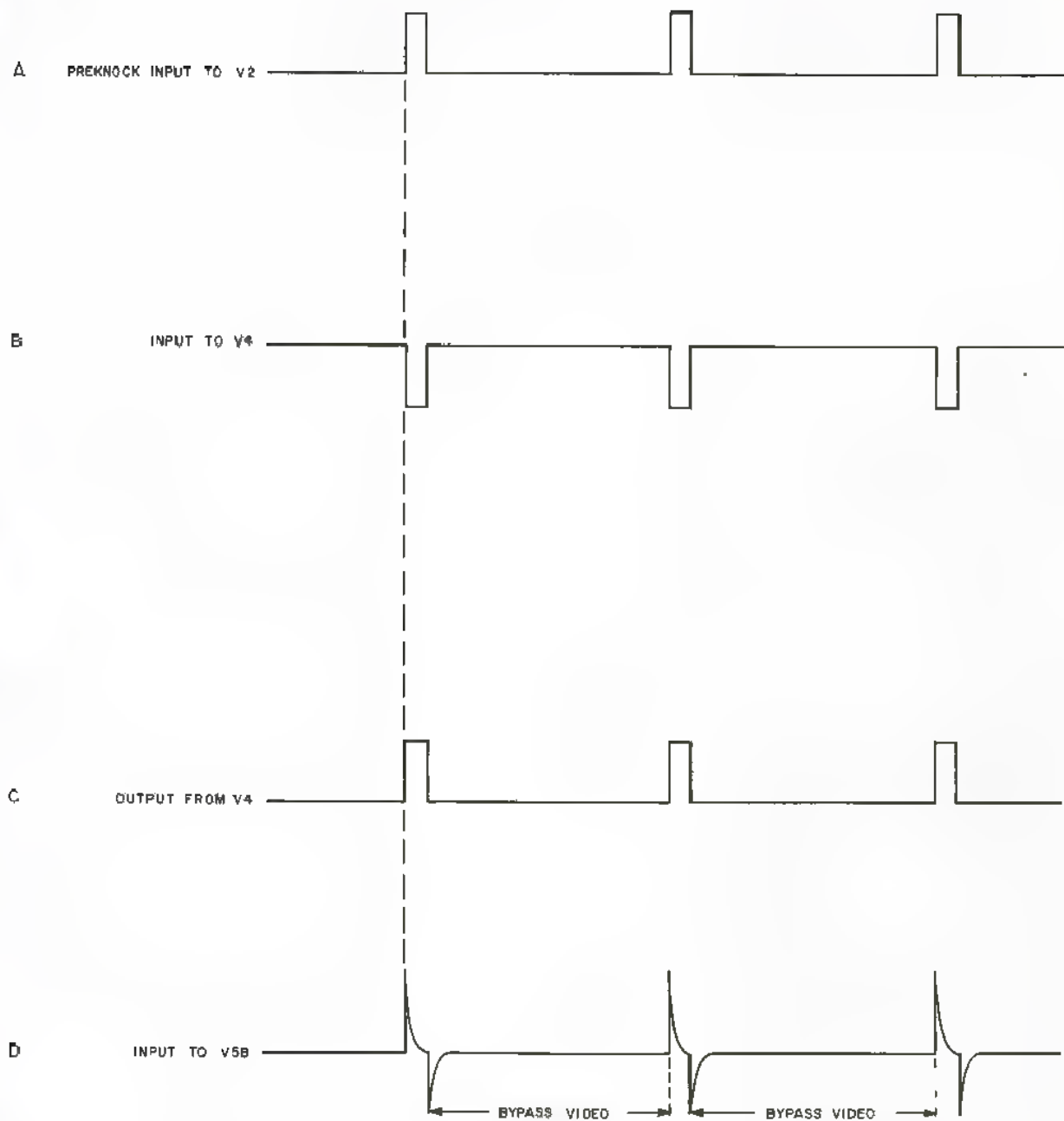
RA PD 467988

Figure 9 (U). Range pulse waveforms – MTI-MODE switch S18 in OFF position

The positive pulse drives V5A into conduction and the negative going plate of V5A causes V5B to cut off. The negative gate at the plate of V5A drives V6 into cutoff and the positive gate at the plate of V5B, when coincident with the MTI video pulse, drives V7 into conduction. However, this interval is short-lived because the negative pulse almost immediately cuts V5A off and V5B on. This action in turn cuts V6 on and V7 off. This conduction remains until the next preknock pulse is applied, at which time the cycle is repeated. Thus, bypass video is passed for practically the entire period between preknock pulses.

17.1 (U). Electronic Gate 9150871

a. General. The electronic gate generates voltages that establish and control the boundaries of an MTI sector on the PPI presentation of the acquisition radar system.

b. Detailed Theory. The detailed theory of electronic gate 9150871 (fig. 91, TM 9-1430-257-20/1) is the same as that for the switching and mixer unit, paragraph 17, except that the IFF video in connector J5 and video and IFF mixer V8B are not used in electronic gate 9150871. Therefore, for electronic gate 9150871 paragraph 17b(1)(r) should read as follows: Either a bypass video or MTI video signal is coupled from the plates of V6 and V7 through capacitor C17, developed across grid resistor R45 and applied to the grid (pin 3) of video and IFF mixer V8. Bias for the grid is established by the voltage divider consisting of resistors R46 and R47 between cathode and ground. The low impedance output of V8 is applied through capacitor C18 and connector J4 to the video and mark mixer.

17.2 (U). Electronic Gate 9990560

a. General. The electronic gate generates voltages that establish and control the boundaries of an MTI sector on the PPI presentation of the acquisition radar system.

b. Detailed Theory. The electronic gate (fig. 38.1, TM 9-1430-257-20) combines the preknock pulse, sector angle resolver voltage, bypass

video, MTI video, and/or jam strobe video to produce a composite output to be used by the external video and mark mixer. The above signals are mixed to obtain azimuth and range components for presentation on the acquisition presentation system, to obtain a normal radial sweep with a combination of MTI video, bypass video, and jam strobe video, or to obtain a normal radial sweep with jam strobe video only. Also, a normal radial sweep with bypass video only may be obtained. The presentation obtained is selected by MTI-MODE switch S18 located on the acquisition and IFF control-indicator (fig. 21 2, TM 9-1430-257-20), AJD switch S20, and JS ONLY switch S11. The operation of the electronic gate is explained in terms of settings of the three switches located on the acquisition and IFF control-indicator.

(1) *Circuit operation — MTI-MODE switch S18 in SECTOR position, JS ONLY switch S11 in OFF position, and AJD switch S20 in OFF position.*

(a) The functions of clipper amplifier V1A and 4-kc detector V1B (fig. 38.1, TM 9-1430-257-20) can be utilized only in the SECTOR position of MTI-MODE switch S18. Amplifier V1A and detector V1B aid in the development of the MTI sector on the PPI presentation. Since the output of V1B is grounded through connector P1-1 in the OFF and 360° positions of S18, an MTI sector cannot be generated in these switch positions. The output from an external sector angle resolver is applied through connector P2-9 to terminal 1 of 4 KC ADJ variable resistor R1. The output from the sector angle resolver is a 4-kc signal (A, fig. 6) modulated by a rotation component which represents the azimuth rate of the acquisition antenna. In order to get one null per revolution, the sector resolver output is mixed with a 4-kc reference carrier (B, fig. 6) that is applied through P2-7 to terminal 3 of R1. The addition of in-phase components and the subtraction of out-of-phase components produce a waveform as indicated by C, figure 6.

(b) Variable resistor R1 (fig. 38.1, TM 9-1430-257-20) is set to obtain minimum ac voltage at test point TP1 during checks and adjustments. The selected reference point from the angle resolver yields a single null point for one antenna revolution, which later serves as a gate center for establishing a sector on the PPI presentation. The composite signal (C, fig. 6) is picked off by the brush arm of R1 (fig. 38.1, TM 9-1430-257-20) and applied through the isolation circuit consisting of capacitor C1 and resistor R2 to the control grid of clipper amplifier V1A. The isolation circuit prevents the —4.6-volt dc bias, developed across R4 and R3 between ground and —250 volts, from entering the 4-kc oscillator and the sector angle resolver. Since the —4.6-volt bias maintains conduction of V1A slightly above cutoff, grid clipping of the negative portion of the input voltage occurs. Only the positive halves of the composite signal from R1 pass through V1A. These are inverted and amplified in V1A to produce a waveform as shown in D, figure 6.

(c) The output of V1A (fig. 38.1, TM 9-1430-257-20) is coupled through capacitor C2 to the cathode of V1B Since positive voltage on the cathode cuts off V1B, the duration of its conduction is governed by the cutoff level set by SECTOR WIDTH variable resistor R8. A voltage divider composed of resistors R7, R8, and R9 provides a dc voltage that is variable from —14 volts to +68 volts. A preset value of voltage in this range provides a dc level for the voltage on C2. Signals at the cathode of V1B are developed across R6, part of R8, and R7. These signals are also coupled through capacitor C3 to TP1.

(d) Assume that this level (zero dc line) is set 2 volts below the clipped level from V1A as shown in E, figure 6. All positive portions of the rotation

voltage will be clipped by V1B cutoff, and all negative portions will pass from cathode to plate to ground through the network consisting of resistor R17 and capacitor C8. Current through R17 produces a negative voltage at the junction of R17 the plate of V1B, and also at the suppressor grid of preknock selector V2 where it prevents tube conduction. Since R8 sets the level for V1B conduction, it also establishes the sector width. This sector width is indicated by the dotted lines projected upward from the zero dc line as shown in E, F, and G, figure 6. The sector width is represented by a gate (H, fig. 6) whose time interval exists between V1B cutoff and return to conduction. The gate is used later to produce the MTI sector.

(e) When R8 sets the zero dc line 4 volts below the clipped level from V1A as shown in F, figure 6, V1B is cut off for a longer interval, thus producing a longer gate. This is extended further when the zero dc line is set 6 volts below the clipped level from V1A as shown in G, figure 6. Then the arc segment of the sector increases in length and a wider sector is presented on the PPI presentation. During V1B conduction, the 4-kc component is filtered out in the R17, C8 network, and the output appears as represented by the waveforms shown in H, figure 6

(f) During SECTOR operation of the switching and mixer unit (fig. 38.1, TM 9-1430-257-20), preknock selector V2 acts as a coincidence tube. The suppressor grid is returned to ground through the R17, C8 circuit instead of being grounded directly to the cathode of V2. With the suppressor connected in this manner, the suppressor grid current in V2 can increase to a level sufficient to cut off V2. In addition, the control grid of V2 is biased at —14.75 volts by a voltage divider consisting of

R18 and R19 between ground and —250 volts, thus providing two grid elements in V2 which can maintain V2 at cutoff. When the output from V1B is applied to the suppressor grid of V2, the maximum amplitude Y of the gate shown in H, figure 6 effectively grounds the suppressor grid. Then, for the duration of the gate, V2 is held below cutoff only by the bias on the control grid.

(g) Preknock pulses (J, fig. 6) are applied through connector J1 and coupled through capacitor C9 to the control grid of V2. The presence of a gate from V1B on the suppressor grid of V2, in coincidence with preknock pulses on the control grid, drives V2 above cutoff. Then a series of preknock pulses is passed through V2 for a time interval equal to the width of the sector adjustment. The negative-going pulses are developed across resistor R10. The output shown in K, figure 6, is coupled through capacitor C4 to the cathode of range phantastron diode 1 V3A.

(h) The generation of range in the MTI sector is performed by V3A, range phantastron diode 2 V3B, range phantastron V4, plus associated circuit components. The output from V2 to V3A is shown in expanded form in A, figure 7 to facilitate explanation of occurrences per each preknock pulse. Between preknock pulses, the cathode of V3A (fig. 38.1, TM 9-1430-257-20) is at +35 volts set by the drop across the resistance of the voltage divider consisting of resistors R11, R13, and R14. The plate voltage of V3A is set by the voltage divider consisting of resistor R12, the cathode-to-grid resistance of V4, and resistor R23. The drop through this circuit maintains the plate potential of V3A below that of the cathode, and consequently V3A is cut off Capacitor C5 bypasses R14 and maintains the voltage drop across R14 constant

This voltage is the suppressor grid voltage for V4.

(i) Between pulses, the positive control grid of V4 causes plate and screen current generating a voltage drop across R23. Electrons flow from ground to the +250 volts supply through resistor R27, part of SECTOR RANGE variable resistor R25, connector P1-3, switch S18A-3 and 4, P1-7 and 9, TEST switch S1, P1-11, range phantastron diode 2 V3B, and resistor R16. This lowers the voltage at the junction of the plates of V3B and V4 Because of screen current in R23, the cathode of V4 approaches plate potential, cutting off plate current. Capacitor C6 charges and stabilizes the potential between the plate and control grid of V4. Consider this condition the pretrigger or quiescent state.

(j) A negative preknock pulse is coupled from V2 through C4 to the cathode of V3A. Diode V3A conducts and lowers the potential on the control grid of V4, cutting off screen current and raising the screen voltage. This instantaneous rise is the beginning of the range gate for MTI presentation and is shown as the leading edge of the square wave in B, figure 7.

(k) On termination of the preknock pulse, the suppressor grid of V4 (fig. 38.1, TM 9-1430-257-20) receives a positive pulse from the junction of R13 and R14, and the plate of V4 starts to conduct. The potential between the plate and control grid becomes unstable, and C6 begins to discharge through R12 toward +250 volts. Current from C6 through R12 causes the control grid to go negative and maintains the screen grid cut off. Plate current increases and drops the plate voltage to a point where V3B cuts off. Then capacitor C7 charges to the voltage set by R25.

(l) After the preknock pulse has expired, the cathode of V3A returns to

+35 volts and the control grid of V4 returns to its quiescent state. Increase in screen current reduces plate current and the plate potential of V4 starts to rise. This rise in plate potential continues until it is higher than the charge on C7, allowing V3B to begin conducting. Capacitor C7 discharges rapidly through V3B and the drop across R16 cuts off the plate of V4. The square wave generated across the cathode resistor R23 of V4 is coupled through capacitor C15, developed across resistor R20 and applied to the grid of V5A. Resistors R22 and R21 between —250 volts and ground form a voltage divider network which holds a bias on the grid of V5A of approximately —195 volts. Crystal diode CR1 is a positive clamper which holds the bias on V5A nearly constant.

(m) Consider the case when the positive pulse of the input to V5A (fig 38.1, TM 9-1430-257-20) causes V5A to conduct. Electron current from —250 volts, through cathode resistor R34, V5A, and plate load resistors R37 and R39 causes a voltage drop (D, fig. 7) which is applied directly to the grid of generator gate V6A. This voltage is also applied through resistor R35 and capacitor C11 to the control grid of gating multivibrator V5B. Reduction of current through V5B produces a positive-going voltage across plate load resistors R38 and R40. This signal (E, fig. 7) is applied to grid of gate generator V6B through resistor R42.

(n) Gate generator V6A is cut off by the negative signal from V5A and the drop across common cathode resistor R44 caused by V6A current is removed. This action allows one section of gating amplifier V7 to conduct and allows bypass video to be amplified. Simultaneously the positive signal from V5B causes V6B to conduct heavily and causes

a large voltage drop across common cathode resistor made up of SW BAL variable resistor R45 and resistor R46 in series. This raises the cathode of the other section of gating amplifier V7 to cutoff and MTI video is blocked. When the negative pulse input cuts off V5A, V5B conducts and gate generators V6A and V6B reverse, and MTI video is passed while bypass video is blocked. Resistors R39 and R40 are grid return resistors for V6A and V6B and resistors R41 and R42 are current limiting resistors. Crystal diodes CR4 and CR5 clip the positive pulses from the output of V5A and V5B to prevent the grids of V6A and V6B from becoming positive and drawing excessive grid current.

(o) When the MTI video signal, applied through connector J3 to control grid 7 of V7, is in coincidence with the negative going gate from V5B and V6B, section 6, 7, 8, of V7 conducts and passes the MTI video signal. At the same instant, bypass video applied through connector J2 to control grid 3 of V7, is blocked due to the positive going output from V5A and V6A. Resistors R32 and R33 are grid return resistors for the two sections of V7. Crystal diodes CR2 and CR3 clip the positive portions of the bypass and MTI video, respectively.

(p) The two plates of V7 are connected and have a common load resistor, R47. A single output of either MTI video or bypass is developed across R47. The bias on the cathodes of V7 is dropped through resistor R44 for section 2, 3, 4, and SW BAL variable resistor R45 in series with R46 for section 6, 7, 8. The cathode bias can be balanced between the two sections of V7 by adjusting SW BAL variable resistor R45. This adjustment insures that there is no change in dc level in the output from the two sections of V7 when

switching from one section to the other. Inductor L1 prevents any video from entering the +150-volt supply.

(q) The positive bypass or MTI video signal is coupled from the plates of V7 through capacitor C16, contacts 1 and 6 of relay K2, to the grid of jam strobe mixer V8A. The input to V8A is developed across resistor R48. The grids of V8A and V8B are clamped at —4.7 volts by the voltage divider consisting of resistor R50 in series with regulator diode CR8 The negative spikes to the input of V8A are clipped by diode CR6. The output of V8A and V8B is applied to Q VIDEO OUT connector J4.

(r) Jam strobe video is applied through connector J5 to JS GAIN variable resistor R53. Variable resistor R53 is in parallel with resistor R49 and the pair are in series with R54. This resistance network terminates the input impedance of the coaxial cable connected to J5. Jam strobe video is applied from the brush arm of R53 to contact 3 of AJD ON relay K1. The input to V8A is either bypass and MTI video output from V7 or jam strobe video, depending on the condition of JS ONLY relay K2. When AJD ON relay K1 is energized, jam strobe video is applied from contact 5 of K1 through coupling capacitor C18 and to the grid of jam strobe mixer V8B. The video output from V8A and V8B are applied through connector J4 Clamping diodes CR6 and CR7 clip the negative spikes from the video when the input voltage exceeds –4.7 volts.

(2) *Circuit operation—MTI-MODE switch S18 in 360° position.*

(a) In the 360° mode of operation, MTI sector operation is eliminated and only normal PPI coverage of bypass video and moving-target video is presented. The suppressor grid of preknock selector V2 is grounded through connector P1-1 and MTI-MODE switch S18. The output from the sector angle resolver has no effect on V2 because the output of V1B is grounded by the same path as the suppressor grid of V2. Since V2 is now connected as a pentode, all preknock pulses pass through V3A.

(b) The remainder of the circuitry operates in an identical manner as described in (1) above, with the following exceptions: The range of the radial sweep is adjusted by means 360° RG variable resistor R26. The electron current flows from ground through resistors R27 and R26, through MTI - MODE switch S18 and MTI CKT TEST switch S1 in the external MTI oscilloscope to the cathode of V3B. Assume that variable resistor R26 is adjusted to increase the recovery time of the plate of V4. As the brush arm of R26 is advanced toward +250 volts, the charge level of capacitor C7 is extended, the plate of V4 reaches the charge level after a longer period. Therefore, the MTI time is reduced and the duration of the bypass time is extended.

(c) The opposite condition exists when the brush arm of R26 is advanced toward ground. The charge level of C7 is reduced, the plate of V4 reaches the charge level after a shorter period. Therefore the MTI time is increased and the duration of the bypass time is reduced. The setting of R26 determines the duration of the gate from V4 and consequently the division of PPI presentation between moving-target video and bypass video.

(3) *Circuit operation—MTI - MODE switch S18 in OFF position.*

(a) During the OFF position of MTI-MODE switch S18, moving-target video is eliminated and a normal 6,400-mil sweep of bypass video is presented. As during 360° operation, described in (2) above, the

sector angle resolver has no effect since the suppressor grid of V2 is grounded through connector P1-1 and switch S18. In the OFF position of S18, the cathode of V3B is also grounded through MTI CKT TEST switch S1 in the MTI oscilloscope, thus disabling the charging capabilities of capacitor C7. Since range control is disconnected, V3B conducts at all times and the constant voltage drop across resistor R16 causes the plate voltage of V4 to be very low and renders the plate ineffective. Phantastron V4 is thus converted to an amplifier (using the screen grid as a plate) instead of a phantastron.

(b) The preknock input of V2 is similar to that used in the SECTOR and 360° modes of operation. However, after the negative preknock input to V4 has expired, the control grid returns to a positive potential determined by the voltage dropped across resistor R17, and screen grid current through V4 is resumed between preknock pulses. The leading and trailing edges of the positive pulses are applied at the grid of V5A. The positive pulse drives V5A into conduction and the negative going plate of V5A causes V5B to cut off. The negative gate at the plate of V5A drives V6A into cutoff and the positive gate at the plate of V5B, when coincident with the MTI video pulse, drives V6B into conduction. However, this interval is short-lived because the negative pulse almost immediately cuts V5A off and V5B on. This action in turn cuts V6A on and V6B off. This conduction remains until the next preknock pulse is applied, at which time the cycle is repeated. Thus, bypass video is passed for practically the entire period between preknock pulses.

18 (U). Video and Mark Mixer 9142873

a. General. The video and mark mixer performs gating and mixing operations on six pres-

entation mark signals. The unit combines the sum of the six marks with acquisition video signals to obtain a composite acquisition video output suitable for application to the acquisition radar indicators

b. Detailed Theory.

(1) The video and mark mixer (fig. 42, TM 9-1430-257-20) supplies the acquisition video signals; the marks which indicate the azimuth of the target tracking antenna (radial segment of the electronic cross); the range setting of the target tracking radar system (arc segment of the electronic cross); a designated azimuth (acquisition azimuth line); and a designated range (range circle) to the acquisition PPI and precision indicators.

(2) Coincidence V1 combines mark and gate signals to produce the arc segment of the electronic cross (fig. 10). These signals originate in the external mark generator (track) and the range mark generator amplifier and are indicated by the horizontal line on the track precision indicator and by the arc of the electronic cross on the PPI indicators. The suppressor grid of V1 (fig. 42, TM 9-1430-257-20) is biased at −5 volts developed across resistor R8 of the voltage divider consisting of resistors R4, R5, and R8 between ground and −250 volts. The control grid of V1 is biased at −11 volts developed across R8 and R5 of the same divider. The acquisition-track range mark, which occurs several times during the period of the track azimuth gate, is applied through ACQ TRK RG MK connector J1 to terminal 3 of ACQ TR. RG. MK. variable resistor R1. The low value of the resistance of R1 combined with that of resistor R15 terminates the input impedance of the cable connected at J1. Resistor R1 sets the amplitude of the acquisition-track range mark. The selected voltage from R1 is coupled through capacitor C2 and developed across resistor R3, then applied to the control grid of V1.

34.5

(3) A track azimuth gate (fig 11) that has a pulse of 711 mils duration riding on a pedestal referenced to a —70-volt level is applied through connector P1-1 to terminal 1 of WIDTH variable resistor R2. The brush arm of R2 is set to a level that allows V1 to conduct for approximately 178 mils (10°) of rotation of the acquisition antenna. The acquisition-track range marks occur at the rate of one for each PPI sweep generated which is 500 cps. These marks are applied to the control grid of V1 and would trace a complete circle on the PPI were this tube always in a conducting stage. However, the bias on the suppressor grid keeps V1 cut off until the track azimuth gate is applied. Then the acquisition-track range marks appear at the plate of V1 as inverted 0.5-microsecond pulses which later form the arc of the electronic cross. Resistor R7 is the plate load, resistor R6 is a parasitic suppressor, and capacitor C3A is a screen grid bypass. The negative-going acquisition-track range marks are coupled through capacitor C4 to stage isolation crystal diode CR1. The nega-

PPI

PRECISION INDICATORS

RADIAL
SEGMENT

ARC
SEGMENT

ELECTRONIC
CROSS

TARGET TRACK CONSOLE

ACQUISITION AZIMUTH
LINE

ACQUISITION RANGE
CIRCLE

BATTERY CONTROL CONSOLE
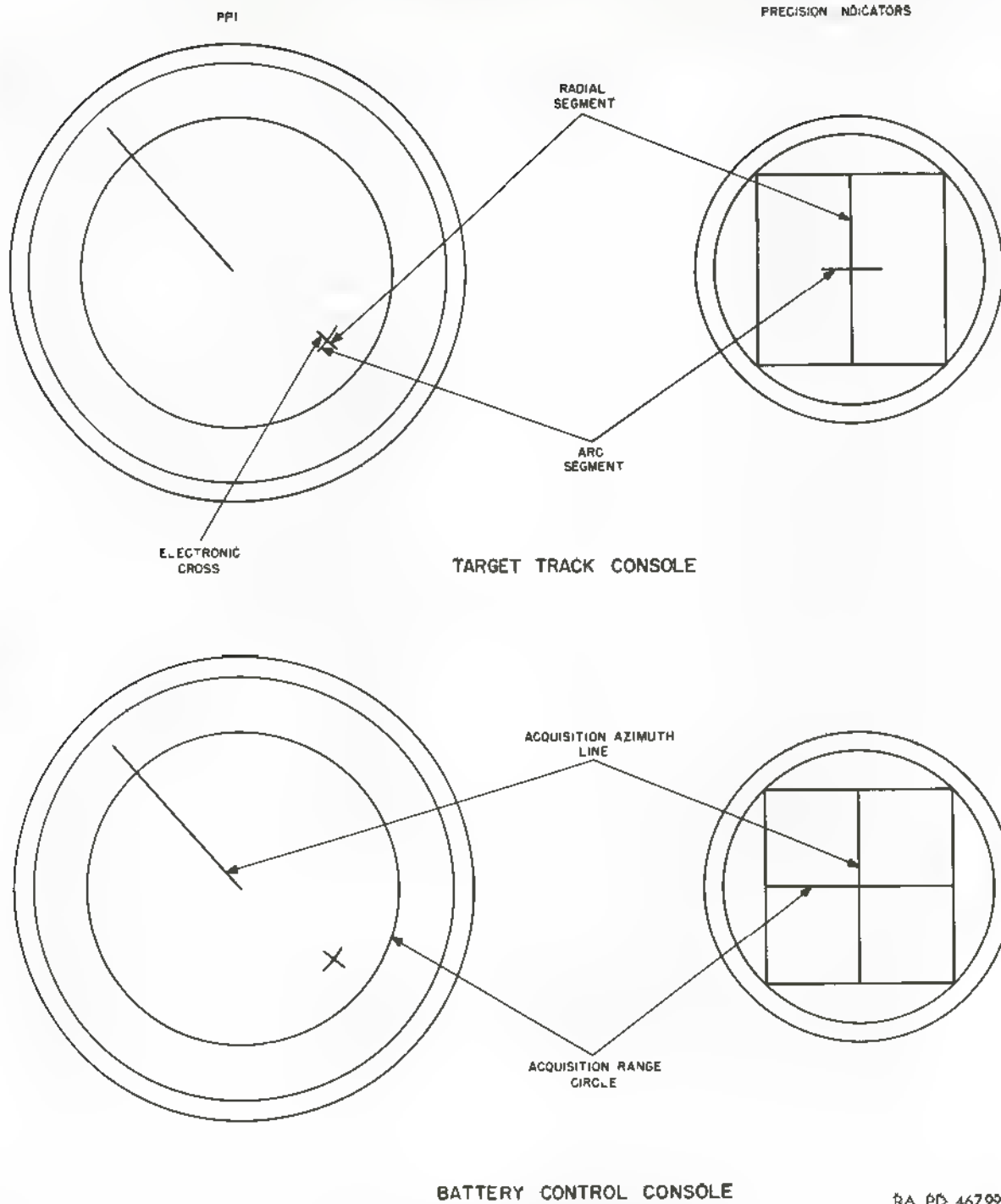
RA PD 467990

Figure 10. (U) Track and acquisition mark components.

produce the radial segment of the electronic cross (fig. 12.1). These signals originate in the external mark generator (track) and the range mark generator amplifier and are indicated by the radial segment of the electronic cross on the PPI and B scope indication. The suppressor grid of V2 is biased at –13 volts developed across resistors R14 and R19 of the voltage divider consisting of resistors R12, R14, and R19 between ground and . 250 volts. The control grid of V2 is biased at —10 volts developed across R19 of the same divider.

(5) A track azimuth mark, representing the target tracking antenna azimuth, is applied through TCK AZ MK connector J2 and coupling capacitor C5 to the suppressor grid of V2. Resistor R10 terminates the impedance of the connecting cable. Resistor R13 is the suppressor grid return. The track range gate is applied through TCK RG GATE connector J3 and coupled through contacts 1-6 of target ranging radar cross off relay K2 and capacitor C6 to the control grid of V2. When target ranging radar cross off relay K2 is operated, the track range gate is removed from the control grid of V2, and no track marks appear on the display. Resistor R11 terminates the impedance of the connecting cable and resistor R16 is the control grid return. Conduction in V2 will occur when the track azimuth mark and the track range gate are applied to V2 simultaneously. Coincidence amplifier V2 conducts during the time the track range gate is applied. The 30-microsecond track range gate represents 5000 yards and the output from V2 is a negative 5000-yard gate that forms the radial line of the electronic cross This gate is developed across plate resistor R18. Resistor R17 is a parasitic suppressor and capacitor C3 bypasses the screen grid. The negative-going gate is coupled through capacitor C9 to stage isola-

tion crystal diode CR2. The negative-going voltage, developed across resistor R22, is applied through the low forward resistance of CR2 and through resistor R24 to the control grid of clipper V3. Since CR1 and CR2 are connected plate-to-plate, the always present high back-resistance serves to prevent interaction between V1 and V2.

(6) The 0.5-microsecond acquisition-track range marks and the 5000-yard track range gate outputs of V1 and V2, respectively, are mixed in resistor R24, developed across resistors R25 and R26, and applied to the control grid of clipper 3. Clipper V3 is biased by a control grid voltage of —2 volts developed across R26 in the voltage divider consisting of R23 and R26 between —250 volts and ground. The input to V3 is either the series of 0.5-microsecond acquisition-track range marks or the 5000-yard track range gate, or both. When both arrive simultaneously, which occurs only once per revolution of the acquisition antenna at the intersection of arc segment (fig. 12.1) and the radial segment of the electronic cross, the 5000-yard gate serves as a pedestal for the 0.5-microsecond acquisition-track range mark and the input to V3 actually is the acquisition track range mark on a pedestal. However, because of the clipping action of V3, the 0.5-microsecond pulse sitting on the gate is clipped off The output developed across load resistor R27 is then either the 0.5-microsecond pulse (fig. 12) or the 5000-yard gate, but never both. The clipping action of V3 is necessary to limit the amplitude of the acquisition-track range marks and thus prevent a blooming spot from appearing at the intersection of the two lines of the electronic cross Resistor R21 (fig. 92), TM 9-1430-257-20/1) is a parasitic suppressor and capacitor C8 is a screen grid bypass.

(7) The positive-going output signal from V3 is coupled through capacitor C11,

ACQUISITION
AZIMUTH LINE

CURSOR   ACQUISITION
LINES   RANGE CIRCLE

200   200

ELECTRONIC CROSS

160   160

120   120

80   80

40   40

B SCOPE INDICATOR

TARGET RADAR CONTROL CONSOLE

RADIAL
SEGMENT
ARC
SEGMENT   ELECTRONIC CROSS

CURSOR LINE   CURSOR LINE
FOR ACQUISITION   FOR ACQUISITION
AZIMUTH   RANGE

ACQUISITION AZIMUTH
LINE

ACQUISITION RANGE
CIRCLE

PPI

BATTERY CONTROL CONSOLE   PRECISION INDICATOR

ORD G28208
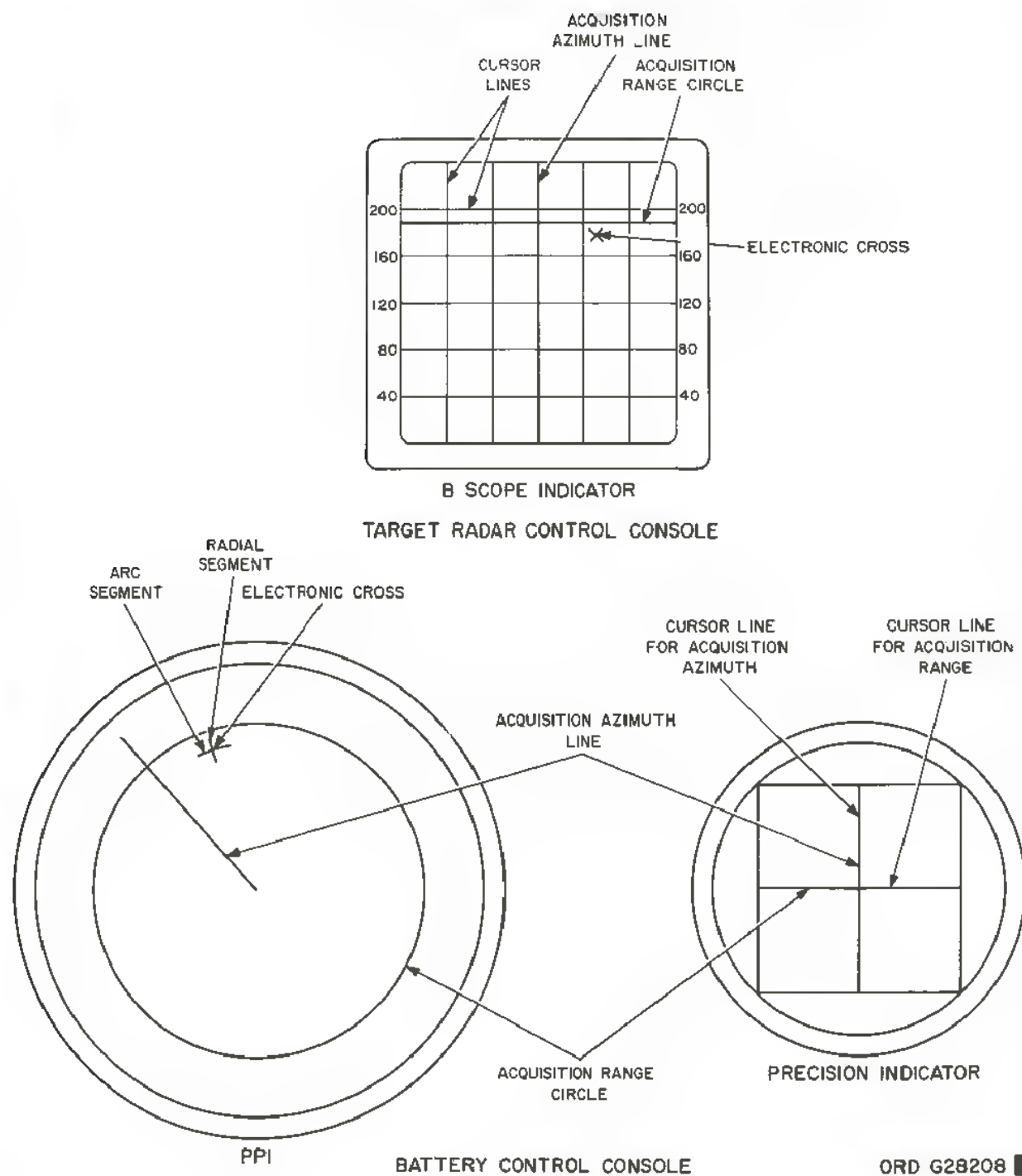
Figure 12.1 (U). Track and acquisition mark components.

developed across resistor R29, and applied to crystal diode clipper CR3. The negative portion of the signal from V3 is shunted through the low forward resistance of CR3 to ground while the positive portion is retained. This portion is applied through diode CR4 and capacitor C13 to the control grid of marker amplifier V4.

(8) A 0.3-microsecond acquisition range mark is applied through ACQ RG MK connector J4 to terminal 3 of ACQ RG MK variable resistor R41. Also, a 1,524-microsecond acquisition azimuth mark is applied through ACQ AZ MK connector J5 to the junction of resistor R42 and crystal diode CR6 Resistors R42 and R49 terminate the input impedance of the respective connecting cables. The cathode-to-cathode connection of diodes CR4, CR5, and CR6 prevents loading and interaction among the inputs. Variable resistor R41 sets the amplitude of the acquisition range mark pulses The acquisition range mark occurs at the rate of one per PPI sweep and therefore the combined sweeps occurring during one antenna revolution draw a complete circle on the PPI according to the range setting in the acquisition system (fig. 12.1). This also produces the horizontal line on the precision indicator and B scope indicators during alinement. The acquisition azimuth mark occurs once per revolution of the acquisition antenna, and therefore brightens a single PPI trace. This produces a radial acquisition azimuth line on the PPI. During alinement, it also produces the vertical acquisition azimuth line on the precision indicator and B scope indicator.

(9) All six mark signals are developed across resistor R30 and coupled through C13 to the control grid of V4. The control grid of V4 is biased by   6 volts developed across resistor R32 of the voltage divider consisting of R22 and R51 between ground and -250 volts. The grid signal developed across resistor R28 is inverted and

amplified in V4. Resistor R33 is a parasitic suppressor and capacitor C10 is a screen grid bypass.

(10) The amplified negative-going signal is coupled from the plate of V4 through capacitor C14 to the control grid of clipper V6. The control grid of V6 is biased by   1.8 volts developed across resistor R38 in the voltage divider consisting of R38 and R57 between ground and   250 volts. This bias is near the cutoff region for V6 and sets the clipping level for negative-going signals on the grid. The amplitude of range mark signals to be clipped is adjusted by means of ACQ TCK RG MK variable resistor R1 and ACQ RG MK variable resistor R41. The negative-going signal is developed across resistor R36, inverted and amplified in V6, and adjusted by means of MK AM variable resistor R50. This adjustment is used to obtain a signal level for proper mixing with the video input. Resistor R39 is a parasitic suppressor, resistor R40 isolates the plate from the screen grid, and capacitor C12 is a screen grid bypass.

(11) The positive-going signal is applied from the brush arm of R50, through resistor R52, capacitor C20, and resistor R57 to the control grids of cathode followers V7A and V7B.

(12) Acquisition video from the LOPAR is applied through LOW PAR VID IN connector J9 and coupled through contacts 4-5 of HIPAR relay K1 to the control grid (pin 2) of amplifier-mixer V8. A bias of -5 volts for the grid is developed across resistor R85 of the voltage divider made up of resistors R85 and R86 between ground and −250 volts. Resistor R84 is the grid return. Video signals more negative than −5 volts are clipped by diode CR10, which shunts them to ground through R85.

(13) Acquisition video from the HIPAR is applied through HIPAR VID IN connector J6, developed across terminating resistor R81, and applied to

terminal 3 of HIPAR VID ADJ variable resistor R72. The signal at the brush arm of R72 is coupled through capacitor C26 and contacts 3-5 of energized HIPAR relay K1 to the grid (pin 2) of V8. Relay K1 is energized by operating the RADAR SELECT switch on the IFF control-indicator to HIPAR. The action of K1 substitutes HIPAR video for LOPAR video in the presentation system. The amplitude of the HIPAR video is adjusted by R72.

(14) IFF video is applied through IFF VID connector J10, developed across terminating resistor R82, coupled through capacitor C25, and applied to the grid (pin 7) of amplifier-mixer V8. Bias of —5 volts for the grid is developed across resistor R85 of the voltage divider made up of resistors R85 and R86 between ground and —250 volts. Video signals more negative than —5 volts are clipped by diode CR11 which shunts them to ground through R85. Resistor R83 is the grid return.

(15) Composite video, made up of either HIPAR or LOPAR acquisition video and IFF video, is developed across common plate resistor R43, coupled through capacitor C15, and applied to the control grids of video amplifiers V5 and V9. Any positive-going portion of the signal across common grid return resistor R45 is shunted to ground by clipper diode CR7.

(16) A portion of the negative composite video at the grids of V5 and V9 is applied to ALARM connector J11 and used to drive the external alarm control.

(17) The negative composite video at the control grid of V9 is amplified and inverted, developed across plate resistor R79, and coupled through resistor R77 to the NOR (normal) contact of PI MKS switch S1. The cathode and suppressor grid of V9 are biased to approximately 1.8 volts by the voltage divider made up of resistor R75 and cathode resistor R78. Resistor R76 is a parasitic suppressor resistor

and capacitor C23 is a screen bypass.

(18) The negative composite video at the control grid of video amplifier V5 is amplified and inverted in the same manner as in V9 and coupled through resistor R53 to the junction of resistor R52 and capacitor C20. At this point, the composite video is mixed with the acquisition and track markers.

(19) A portion of the composite video and marks at the junction of R52 and R53 is applied to the TEST contact of PI MKS switch S1. This switch selects either the composite video without marks (normal) or the composite video with marks (test) for presentation on the precision indicator and B scope indicator.

(20) Positive video from the output of PI MKS switch S1 is coupled through capacitor C24 and resistors R67 and R68 to the control grids of parallel cathode followers V10A and V10B. A bias of —6 volts for the grids is developed across R66 of the voltage divider made up of resistors R65 and R66 between —250 volts and ground. Any video more negative than —6 volts is shunted to ground through clipper diode CR8 and resistor R66. This establishes a reference level for the output developed across common cathode resistor R69. Resistor R70 and capacitor C22 form a decoupling network for the plates of V10A and V10B. The parallel cathode followers provide sufficient power to drive the low impedance inputs of the precision and B scope indicators connected to ACQ VID connector J8. ACQ VID & TEST test point TP2 is used for monitoring the video during test procedures.

(21) Composite video from V5 and acquisition and track marks from V6 are coupled through capacitor C20 to the grid circuits of parallel cathode followers V7A and V7B. The signals are amplified in the same manner as in V10 and coupled through ACQ VID MKS connector J7 to the PPI. ACQ VID TEST & MKS test point

TP1 is used for monitoring the video during test procedures.

18.2 (U). Video and Mark Mixer 9985613

a. General. The video and mark mixer performs gating and mixing operations on six presentation mark signals and mixes IFF video and target video from either the NAR (Nike acquisition radar) or AAR (auxiliary acquisition radar). The unit combines the sum of six marks with the NAR or AAR video signals and the IFF video signals to obtain a composite video output suitable for application to the acquisition indicators. NAR video is also available for monitoring purposes. AAR or NAR video is selected by means of relay switching.

b. Detailed Theory.

(1) The video and mark mixer (fig. 42.1, TM 9-1430-257-20) supplies the IFF video and the NAR or AAR video signals; the marks which indicate the azimuth of the target tracking antenna (radial segment of the electronic cross); the range setting of the target tracking radar system (arc segment of the electronic cross); a designated azimuth (acquisition azimuth line); and a designated range (range circle) to the acquisition PPI and precision indicators.

(2) Coincidence V1 combines mark and gate signals to produce the arc segment of the electronic cross (fig. 10). These signals originate in the external mark generator (track) and the range mark generator amplifier and are indicated by the horizontal line on the track precision indicator and by the arc of the electronic cross on the PPI indicators. The suppressor grid of V1 (fig. 42.1, TM 9-1430-257-20) is biased at –5 volts developed across resistor R8 of the voltage divider consisting of resistors R4, R5, and R8 between ground and –250 volts. The control grid of V1 is biased at –11 volts developed across R8 and R5 of the same divider. The acquisition-track range mark, which occurs sever-

al times during the period of the track azimuth gate, is applied through ACQ TRK RG MK connector J1 to terminal 3 of ACQ TR. RG. MK. variable resistor R1. The low value of the resistance of R1 combined with that of resistor R15 terminates the impedance of the cable connected at J1. Resistor R1 sets the amplitude of the acquisition-track range mark. The selected voltage from R1 is coupled through capacitor C2 and developed across resistor R3, then applied to the control grid of V1.

(3) A track azimuth gate (fig. 11) that has a pulse of 711 mils duration riding on a pedestal referenced to a –70-volt level is applied through connector P1-1 to terminal 1 of WIDTH variable resistor R2. The brush arm of R2 is set to a level that allows V1 to conduct for approximately 178 mils (10°) of rotation of the acquisition antenna. The acquisition-track range marks occur at the rate of each for each PPI sweep generated, which is 400 cps when AAR is selected or 500 cps when NAR is selected. These marks are applied to the control grid of V1 and would trace a complete circle on the PPI were this tube always in a conducting stage. However, the bias on the suppressor grid keeps V1 cut off until the track azimuth gate is applied. Then the acquisition-track range marks appear at the plate of V1 as inverted 0.5-microsecond pulses which later form the arc of the electronic cross. Resistor R7 is the plate load, resistor R6 is a parasitic suppressor, and capacitor C22 is a screen grid bypass. The negative-going acquisition-track range marks are coupled through capacitor C4 to stage isolation crystal diode CR1. The negative-going signal, developed across resistor R9, is applied through the low forward resistance of CR1 and through resistor R24 to the grid of clipper V3.

(4) In a manner similar to the operation of stage V1, coincidence V2 combines mark and gate signals to produce the radial segment of the electronic cross (fig. 10). These signals originate in the external mark generator (track) and the range mark generator amplifier and are indicated by the vertial line on the track precision indicator and by the radial segment of the electronic cross on the PPIs. The suppressor grid of V2 is biased at −13 volts developed across resistors R14 and R19 of the voltage divider consisting of resistors R12, R14, and R19 between ground and −250 volts. The control grid of V2 is biased at −10 volts developed across R19 of the same divider.

(5) A track azimuth mark, representing the target tracking antenna azimuth, is applied through TRK. AZ. MK. connector J2 and coupling capacitor C5 to the suppressor grid of V2. Resistor R10 terminates the impedance of the connecting cable. Resistor R13 is the suppressor grid return. The track range gate is applied through TRK. RG. GATE connector J3 and coupled through capacitor C6 to the control grid of V2. Resistor R11 terminates the impedance of the connecting cable and resistor R16 is the control grid return. Conduction in V2 will occur when the track azimuth mark and the track range gate are applied to V2 simultaneously. Coincidence V2 conducts during the time the track range gate is applied. The 30-microsecond track range gate represents 5000 yards and the output from V2 is a negative 5000-yard gate that forms the radial line of the electronic cross. This gate is developed across plate resistor R18. Resistor R17 drops the screen voltage and capacitor C23 bypasses the screen grid. The negative-going gate is coupled through capacitor C9 to stage isolation crystal diode CR2. The negative-going voltage, developed across resistor R22, is applied through the low forward resistance of CR2 and through resistor R24 to the control grid of clipper V3. Since CR1 and CR2 are connected plate-to-plate, the always present high back-resistance serves to prevent interaction between V1 and V2.

(6) Amplifier V8A amplifies the IFF video signals to be combined with the mark signals discussed in (2) through (5) above. IFF video is applied through IFF VIDEO INPUT connector J8 to terminal 3 of IFF VIDEO variable resistor R63. The low value of resistance of R63 combined with that of resistor R64 terminates the impedance of the cable connected at J8. Resistor R63 sets the amplitude of the IFF video which is coupled directly to the control grid of V8A. Negative feedback is obtained through unbypassed cathode resistor R68. Resistor R67 is the plate load. The amplified IFF video from the plate of V8A is coupled through capacitor C28 to isolation crystal diode CR10 and to CR14 and resistor R69. Crystal diode CR14 shunts the positive portion of the IFF video to ground and retains the negative portion. The IFF video signal is coupled through isolating crystal diode CR10 and through resistor R24 to the grid of clipper V3. Diode CR10 isolates V8A from V1 and V2 to prevent interaction.

(7) The 0.5-microsecond acquisition-track range marks and the 5000-yard track range gate outputs of V1 and V2, respectively, and the IFF video output of V8A are mixed in resistor R24; developed across resistors R25 and R26; and applied to the control grid of clipper V3. Clipper V3 is biased by a control grid voltage of −2 volts developed across R26 in the voltage divider consisting of R23 and R26 between ground and −250 volts. The input of V3 is IFF video and either the series of 0.5-microsecond

acquisition-track range marks or the 5000-yard track range gate, or both. When both arrive simultaneously, which occurs only once per revolution of the acquisition antenna at the intersection of arc segment (fig. 10) and the radial segment of the electronic cross, the 5000-yard gate serves as a pedestal for the 0.5-microsecond acquisition-track range mark and the input to V3 actually is the acquisition track range mark on a pedestal. However, because of the clipping action of V3, the 0.5-microsecond pulse sitting on the gate is clipped off. The output developed across load resistor R27 is then either the 0.5-microsecond pulse or the 5000-yard gate, but never both. The clipping action of V3 is necessary to limit the amplitude of the acquisition-track range marks and the IFF video and thus prevent a blooming spot from appearing at the intersection of the two lines of the electronic cross. Resistor R21 (fig. 42.1, TM 9 1430 257-20) is a parasitic suppressor and capacitor C24 is a screen grid bypass. Inductor L5 isolates the plate from the screen grid.

(8) The position-going output signal from V3 is coupled through capacitor C11, developed across resistor R29, and applied to crystal diode clipper CR3. The negative portion of the signal from V3 is shunted through the low forward resistance of CR3 to ground while the positive portion is retained. This portion is applied through diode CR4 and capacitor C13 to the control grid of amplifier V4.

(9) A 0.5-microsecond acquisition range mark is applied through ACQ. RG. MK. connector J4 to terminal 3 of ACQ. RG. MK. variable resistor R41. Also, a 1600-microsecond acquisition azimuth mark is applied through ACQ. AZ. MK. connector J5 to the junction of resistor R42 and crystal diode CR6. Resistors R42 and R49 terminate the input imped-

ance of the respective connecting cables. The cathode-to-cathode connection of diodes CR4, CR5, and CR6 prevents loading and interaction among the inputs. Variable resistor R41 sets the amplitude of the acquisition range mark pulses. The acquisition range mark occurs at the rate of one per PPI sweep and, therefore, the combined sweeps occurring during one antenna revolution draw a complete circle on the PPI according to the range setting in the acquisition system (fig. 10). This also produces the horizontal line on the acquisition precision indicator. The acquisition azimuth mark occurs once per revolution of the acquisition antenna and, therefore, brightens a single PPI trace. This produces a vertical acquisition azimuth line on the acquisition precision indicator and a radial acquisition azimuth line on the PPIs.

(10) All six mark signals and IFF video are developed across resistor R30 and coupled through C13 to the control grid of V4. The control grid of V4 is biased by -6 volts developed across resistor R32 of the voltage divider consisting of R31 and R32 between ground and -250 volts. The grid signal developed across resistor R28 is inverted and amplified in V4. Resistor R34 is the plate load resistor for V4, resistor R33 is a parasitic suppressor, and capacitor C27 is a screen grid bypass.

(11) The amplified negative-going signal is coupled from the plate of V4 through capacitor C14 to the control grid of clipper V6. The control grid of V6 is biased by -1.8 volts developed across resistor R38 in the voltage divider consisting of R37 and R38 between ground and -250 volts. This bias is near the cutoff region for V6 and sets the clipping level for negative-going signals on the grid. The amplitude of range mark

biased at -3 volts which is developed signals to be clipped is adjusted by means of ACQ. TRK. RG. MK. variable resistor R1 and ACQ. RG. MK. variable resistor R41. The negative-going signal is developed across resistor R36, inverted and amplified in V6, and adjusted by means of MK. AMP. variable resistor R50. MARK AMP variable resistor R50 in series with cathode resistor R51 is the cathode resistance for V6. This adjustment is used to obtain a signal level for proper mixing with the video input. Resistor R39 is a parasitic suppressor, resistor R40 is the plate load, and inductor L2 isolates the plate from the screen grid. C25 is a screen grid bypass.

(12) The positive-going signal is applied from the plate of V6, through resistor R52, capacitor C33, and resistors R89 and R90 to the control grids of cathode follower V11.

(13) The NAR video output of the external switching and mixer unit is applied through NAR VIDEO INPUT connector J6 and coupled through capacitor C15 to the control grid of clipper amplifier V5. Resistor R43 is the parasitic suppressor in the plate supply of the output stage in the external switching and mixer unit (par. 17). The video signal is developed across grid return resistor R45, and the positive portions of the signal are clipped by crystal diode CR7. This clipping action and the +1.78-volt bias on the cathode limit the amplitude of the video. While signals just over noise can be seen on the PPI, strong signals are eliminated and therefore cannot cause blooming. The video is inverted to the positive phase in V5 and developed across resistor R48. Resistor R47 is a parasitic suppressor and capacitor C26 is a screen grid bypass. Inductor L1 and resistor R48 isolate the plate from the screen grid.

(14) When NAR is selected, the positive NAR video from V5 and the positive

mark signals and IFF video from V6 are mixed in the circuit consisting of resistor R52 and R53 when relay K1 is deenergized, then coupled through capacitor C33 to the control grids of mixer-cathode follower V11. V11 is biased at −6 volts developed across resistor R88 in the voltage divider consisting of R87 and R88 between ground and −250 volts. The composite signal is developed across grid return resistors R86 and R88. Negative portions of the signal below the −6-volt level are clipped by crystal diode CR8. Resistors R89, R90, and R91 are parasitic suppressors, and C34 is plate bypass. Both stators of cathode follower V11 are paralleled to obtain the power necessary to drive the external load. Cathode follower V11 isolates the mixing circuits from the load, and since the cathodes follow the grids, the positive output developed across common cathode resistor R92 is applied through ACQ/AAR VIDEO connector J7 to the external indicators. ACQ. VIDEO TEST test point TP2 is used for monitoring the video during test procedures.

(15) When AAR is selected, relay K1 is energized and the positive video from V9 and the positive mark signals and IFF video from V6 are mixed in resistors R77 and R52 and then coupled through capacitor C33 to mixer-cathode follower stage V11. The circuit action is identical to that in (14) above.

(16) Amplifiers V8B and V9 function to amplify and invert the AAR video to the correct phase. AAR video is applied through AAR VIDEO INPUT connector J9 to terminal 3 of AAR VIDEO variable resistor R65. Resistor R65 in series with the resistance of R66 terminate the impedance of the cable connected at J9. Resistor R65 sets the amplitude of the AAR video which is coupled from the brush arm of R65 through coupling capacitor C36 to the control grid of

amplifier V8B. The grid of V8B is biased at –3 volts which is developed across resistor R96. Resistor R96 is part of the voltage divider composed of resistor R95 and R96 between –250 volts and ground. Resistors R94 and R96 are the grid return to ground. Diode CR13 shunts a portion of the negative video to ground. Some inverse feedback is provided across unbypassed cathode resistor R71. Resistor R70 is the plate load. Resistor R98 is a parasitic suppressor and capacitor C38 is a plate bypass capacitor. The output video from the plate of V8B is coupled through coupling capacitor C29 to the grid of amplifier V9. Resistor R72 is the grid return for V9. Diode CR11 clips the positive portion of the signal.

(17) Amplifier V9 amplifies and inverts the negative video input to obtain the proper level and phase for mixing in mixer-cathode follower stage V11. V9 is biased at –1.7 volts caused by the positive voltage on the cathode of V9 developed across cathode resistor R76 which is part of the voltage divider composed of R73 and R76 between +150 volts and ground. Resistor R75 is the plate load. Resistor R74 is a parasitic suppressor and capacitor C30 is a screen grid bypass. Inductor L3 and resistor R75 isolate the plate from the screen grid. The suppressor grid is clamped at +1.7 volts by the voltage developed across R76. The output from the plate is mixed with the mark signals and IFF video as described in (15) above, when relay K1 is energized.

(18) AAR relay K1 selects either AAR video or NAR video to be mixed with the mark and IFF video signals. When K1 is deenergized, NAR video is selected and, when K1 is energized, AAR video is selected. When K1 is deenergized, the output of amplifier V9 is developed across resistor R93 which serves as a dummy load for V9. Resistor R78, capacitor C35, and in-ductor L4 form a decoupling network to keep video signals out of the +150-volt plate supply. When K1 is energized, the output of V9A is coupled through contacts 6 and 2 of relay K1 to the input of V11 and resistor R93 matches the plate of V5 to the input of V7.

(19) Cathode follower V7 is identical in operation to cathode follower V11. The input of V7 is NAR video only when K1 is energized. When K1 is deenergized, the input to V7 is in parallel with the input of V11 through contacts 4 and 5 of relay K1. The output at NAR VIDEO connector J11 will be either NAR video without marks and IFF video or NAR video with marks and IFF video. The output at J11 is used in a remote console for monitoring purposes.

19 (U). MTI Oscillocope 9137928

a. General. The MTI oscilloscope is a permanent unit built into the acquisition radar system. It is used specifically for monitoring purposes during MTI adjustment procedures. While the oscilloscope has the usual gain, focus, intensity, and positioning controls contained internally, the monitoring functions are dependent upon adjustment of controls located on the various chassis of the MTI system. The oscilloscope uses an 11-position switch to change the internal operation of itself and the MTI system to meet conditions of the particular MTI adjustment procedure.

b. Detailed Theory.

(1) A positive preknock pulse is applied through connector J1 and coupling capacitor C1 to the control grid of sweep gate multivibrator V1A (fig. 39, TM 9-1430-257-20). This triode in conjunction with sweep gate multivibrator V1B forms a one-shot multivibrator which produces a gate between preknock pulses. Multivibrator V1A is biased by +1.5 volts at the control grid developed across resistor R2 of the voltage divider consisting of resistors R1 and R2 between +150 volts and ground. Normally

V1A is cut off by the positive voltage on the cathode developed by the heavy conduction current of V1B through cathode resistor R4. The positive preknock pulse on the grid of V1A drives V1A into conduction and the consequent drop across plate load resistor R3 is coupled through paralleled capacitors C2 and C3 to the control grid of V1B. These capacitors are paralleled through switch S1A. Switch S1A is part of MTI CKT TEST switch S1. All the functions of switch S1 are covered in detail in c below.

(2) Sweep gate multivibrator V1B is normally conducting, due to a small positive voltage produced across resistor R7 by grid current of V1B. The negative preknock pulse from V1A drives V1B to cutoff which in turn cuts off V1B current through R4. This prolongs conduction in V1A, producing a gating period determined by the multivibrator constants of capacitors C2 and C3 and resistors R3 and R7. The resulting positive gate is applied from the junction of plate resistors R5 and R6 through capacitor C10 to the control grid of cathode-ray tube V5. This gating voltage establishes the unblanking interval for the V5 presentation.

(3) Clamped horizontal sawtooth generator V2B is normally conducting due to a small positive voltage produced

across resistor R8 by V2B grid current. The negative gate from V1A is coupled through the grid circuit of V1B and capacitor C4 to the control grid of V2B. This cuts off V2B and permits paralleled capacitors C5 and C6 to charge through resistor R9 toward +250 volts. The charging interval produces the duration of the linear sweep for deflection of the electron beam in cathode-ray tube V5. This charging interval exists during negative gate time, and on recovery of multivibrators V1A and V1B to preknock status, V2B resumes conduction. Capacitors C5 and C6 rapidly discharge through the low plate-resistance of V2B and thus produce the retrace period of V2B and thus produce the retrace period of the sweep. It should be noted that capacitor C6 is in parallel with C5 only when S1B is in the 1, 2, 4, 6, 7, 8, and 9 positions. In positions 3, 5, 10, and 11, C6 is disconnected from the circuit.

(4) The positive sweep voltage is directly applied from the junction of resistor R9 and capacitors C5 and C6 to the control grid of phase inverter sweep amplifier V3A. Increase of plate current through resistor R10 produces a linear sweep voltage which is applied to horizontal deflection plate 10 of cathode-ray tube V5. The current increase through V3A also flows through cathode resistor R14, producing a voltage rise which appears

with the input for attenuating high amplitude signal levels and thus eliminates the necessity for constantly readjusting the oscilloscope gain control. Capacitor C12 is adjusted to pass the high-frequency components of the input signal and thus retain the sharp leading edges of the original square-wave input.

(6) MTI test video, taken off the MTI video line, is applied through connector J3 to switch S1E. Similar to acquisition video, the test video is also coupled through a parallel circuit where test video bandpass variable capacitor C11 is adjusted for optimum ac signal and where resistor R40 attenuates the excessively high amplitudes of the input signal. When low levels of test pulse residue voltages are to be measured, attenuation circuit C11 and R40 is bypassed and the weak signal is applied directly to the input circuit of clamped vertical sawtooth generator V2A.

(6.1) Interference suppressor test video from the trigger pulse amplifier is applied through connector J4 to switch S1E. From S1E the video is applied direct to the input circuit of clamped vertical sawtooth generator V2A.

(7) Acquisition video, interference suppressor test video, or MTI test video can be selected by switch S1E and then coupled through capacitor C7 to the control grid of V2A. The signal is developed across resistor R20, inverted in V2A, and developed across GAIN variable resistor R18. The gain developed across R18 is low;

however, the voltage level picked off by the brush arm of R18 is adequate to vertically scan the 2-inch screen of V5. This voltage is coupled through capacitor C8 to the control grid of video amplifier V4. In systems 1034 through 1059, type 6AG7 tube V4 has been changed to the ruggedized type 6AG7Y tube. The negative-going signal is developed across resistor R24 and inverted in V4. The signal is developed across resistors R21, R22, and R23, then directly applied to vertical deflection plate 6 of V5. Inductor L1 is used for series compensation of V4. This compensation is required to obtain video peaking within the bandpass limits of the video signal. Three identical resistors, R21, R22, and R23, are series connected to maintain close resistive tolerance and to dissipate heat.

(8) The video signal is vertically positioned by means of VERT POS variable resistor R31 which is a part of a voltage divider consisting of resistors R30, R31, and R32 connected between the +250-volt supply and ground. The variable range across R31 is from +44 to +206 volts, thus providing a variable dc positive potential to vertical deflection plate 7. Adjustment of R31 positions the vertical trace of the electron beam on the screen (face) of V5.

(9) INTENSITY variable resistor R28 controls the brightness of the screen of cathode-ray tube V5 by setting the bias between the control grid and the cathode. The unblanking gate from V1B is developed across resistor R26 and applied to the

control grid of V5. This gate occurs in synchronization with the horizontal deflection voltages from phase inverter sweep amplifiers V3A and V3B and the video signal from V4. Resistor R27 is fixed to protect the -1,000v power supply in the event the cathode element within V5 is grounded. Electrostatic focusing is achieved through adjustment of FOCUS variable resistor R35 which is part of a voltage divider consisting of R33, R34, R35, and R36. The accelerating anode of V5 is connected directly to +150 volts.

(10) CARRIER LEVEL meter M1 is located on the MTI oscilloscope chassis for purposes of calibrating the amplitude of the 15-megacycle carrier generated in the external carrier oscillator. This adjustment is made at the oscillator chassis to give a 4-volt reading on meter M1. The 4-volt indication is marked by a red line on the face of the meter which indicates the required amplitude of the RF carrier.

c. Switching Procedures. The switching steps outlined in (1) through (6) below plus information contained in TM 9-1430-250-20/1 supply adequate information for understanding and performing the MTI adjustments. In outlining the function of switch S1, occasional reference is made below to several specific MTI chassis to supplement the theory of switching in the oscilloscope.

(1) Switch S1A (fig. 39, TM 9-1430-257-20) connects capacitor C3 in parallel with capacitor C2, thereby extending the gating time of sweep gate multivibrators V1A and V1B. This arrangement is used in all positions except 3, 5, 10, and 11. In these positions, only C2 is used to obtain a short duration gate which is used with rapid sweep to examine short duration pulses on the screen of the oscilloscope.

(2) Switch S1B connects capacitor C6 in parallel with capacitor C5, thereby extending the sweep time of the V2A stage. The combined capacitance is used in all switch positions except 3, 5, 10, and 11. In these positions, the elimination of C6 produces a faster sweep time useful for presenting short duration pulses.

(3) Switch S1C connects +48-volts, from the voltage divider consisting of resistors R37 and R38 between +150 volts and ground, to range phantastron diode 2 in the external switching and mixer unit. This puts the range limit from that diode near the middle of the screen of the oscilloscope. This function is performed in switch positions 1 and 9 only. In the remaining switch positions, S1C gives MTI range control to the MTI—MODE switch in the external acquisition control-indicator to allow a choice of SECTOR, 360°, or OFF in the range selection functions.

(4) Switch S1D connects +150 volts to the external delay amplifier to energize it and thereby allow the delay channel to operate. This function is used in all switch positions except 3, 6, 7, and 8. In these positions, the delay amplifier is disabled by removal of the +150 volts. Then the composite signal as it appears in the non-delay channel is observed on the oscilloscope.

(5) Switch S1E connects the attenuated acquisition video from the unit to V2B. This is performed through switch positions 1, 8, and 9 only. In position 2, S1E connects 1.2 volts ac to the input of V2A. This voltage is derived from the 6.3-volt filament ac supply by a drop across resistor R41 of the voltage divider consisting of R41 and R42. The 1.2 volts ac replaces the video signal as input to the cathode-ray tube. This voltage is used to calibrate the oscilloscope where it is used as a reference for setting the GAIN variable resistor R18 control. In switch positions 3, 4, and 6, attenuated test video pulses are applied to V2B. In positions 5, 7, and 10, test signals are also applied to V2B; however, in this case low amplitude signals are measured. This condition necessitates bypassing of the attenuation circuit consisting of C11 and R40.

(6) Switch S1 is normally left in position 2 because maximum variable range is available for MTI operation.

20. (CMHA) Alarm Control 9000450

a. General. The alarm control provides an audible warning as a supplement to visual observation. An external 4-inch speaker produces a 500-cps tone if a target signal appears in a selected sector on the acquisition PPI presentation. The alarm control utilizes preknock, video, acquisition azimuth gate, and acquisition range mark signals to produce the audible alert. The covered sector is adjustable in azimuth from 3 degrees to 360 degrees centered about the acquisition (flashing) azimuth line and extends in range from zero to full radar range, which is 200,000 yards. Alarm control - 9000450 is used in systems 1001 to 1070. Beginning with system 1071 alarm control - 9000450 is replaced by alarm control - 8158475 (par. 20.1).

b. Detailed Theory.

(1) Monostable multivibrators V7A and V7B determine the outer limit of the sector range for the alarm control circuits (fig. 26, TM 9-1430-257-20). During quiescence the control grid of V7B draws current, producing a drop across resistor R29 almost equal to the +150-volt supply. This leaves approximately +1 volt as positive bias on the grid of V7B and

fixes a reference level for one side of capacitor C15. Multivibrator V7A is cut off by the voltage developed across cathode resistor R40 by the conduction of V7B. With V7A cut off, C15 charges toward +150 volts through resistors R28 and R22. This charge sets the positive level (B, fig. 13) for all square waves that originate at V7A between preknock pulses.

A   PREKNOCK INPUT
    TO V7A

B. OUTPUT OF
    V7A

C. OUTPUT OF
    V7B

D. OUTPUT FROM
    CR7

E. INPUT TO V6B

    0.5 USEC

F   OUTPUT FROM
    V6B

RA PD 467992
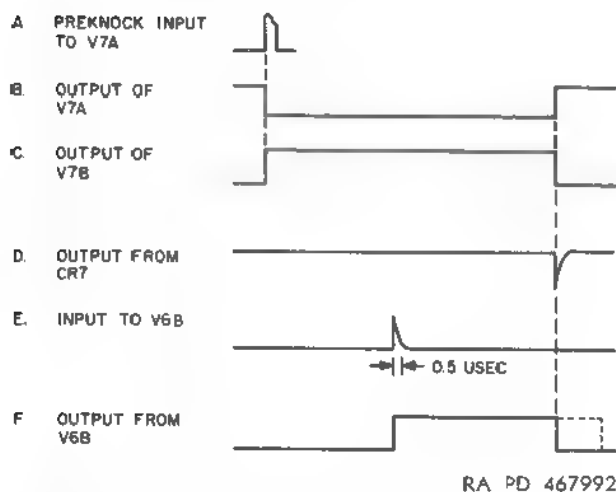
Figure 13. (U) Alarm control waveforms - V6 and V7.

(2) A positive preknock pulse (A, fig. 13) is coupled through connector J3 (fig. 26, TM 9-1430-257-20), capacitor C16, and resistor R38 to the grid of V7A. BIAS variable resistor R37 sets the bias level for V7A. The dc voltage is dropped from −250 volts across R36 and set from 0 to −10.9 volts by means of R37. Capacitor C17 decouples the preknock pulse from the −250-volt supply. The preknock pulse is developed across resistor R39 in series with the ground side of R37. The negative excursion limit of the pulse is set by R37 and clipped by crystal diode CR4. When the lower extremity of the pulse drops below the potential on the plate of CR4, this diode conducts and shunts out R39, thereby virtually grounding the pulse.

(3) The preknock pulse is applied through R38 to the control grid of V7A and causes conduction through V7A. By controlling bias on the tube, R37 controls the plate current through V7A during conduction. Consequently, R37 controls the level of the terminal voltage for charging C15. During the period that V7A is cut off, C15 charges toward +150 volts, and during conduction the plate voltage of V7A drops. Electron current flows from ground through R40 and through V7A to the plate side of C15 for a duration established by the prevailing clamping level of CR4. In this manner the pulse width of the square wave can be varied from 0 to approximately 1,300 microseconds.

(4) In systems 1001 through 1058, the value of C15 is 1,100 micromicrofarads. Beginning with system 1059, the value of C15 has been changed to 1,300 micromicrofarads. The negative-going square wave (B, fig. 13), applied from V7A to the grid of V7B, is inverted at the plate to produce a positive square wave (C, fig. 13) at the junction of resistor R30 (fig. 26, TM 9-1430-257-20) and the plate of V7B. Capacitors C3B and C7A bypass the +150-volt plate supply, and resistor R24 is a parasitic suppressor. The leading edge of the output square wave from V7B is in time coincidence with the preknock pulse. The space between the leading edge and the trailing edge of the square wave is variable in time representing zero range to full radar range. The output square wave is differentiated by capacitor C13 and resistor R21; the positive swing (leading edge) of the differentiated pulse is clipped by the blocking action of crystal diode CR7. The differentiated negative pulse (trailing edge) (D, fig. 13) is applied to bistable multivibrators V6A and V6B.

(5) Bistable multivibrators V6A and V6B determine the inner limit of the sector range for the alarm control circuit. Multivi-

brator V6A is cut off by the voltage developed across cathode resistor R34 caused by conduction of V6B. The negative output of V6B is coupled from the junction of the plate and resistor R26 through resistor R32 and capacitor C12 to the control grid of V6A, thereby cutting off V6A. The positive output from the plate of V6A is coupled from the junction of the plate and resistor R25 through resistor R31 and capacitor C11 to the control grid of V6B, thereby holding V6B at full conduction. This establishes the negative level of the output square wave (F, fig. 13) from V6B.

(6) The acquisition range mark (E, fig. 13) is coupled through connector J2 (fig. 26, TM 9–1430–257–20) and capacitor C14 to the cathode of conducting triode V6B. The acquisition range mark is a positive 0.5-microsecond pulse that varies along the time base according to the acquisition radar range setting. The positive pulse on the cathode cuts off V6B and flips V6A to full conduction, thereby producing a positive-going square wave (F, fig. 13) from the plate of V6B. Duration of this square wave is terminated by application of the differentiated negative pulse (D, fig. 13) from V7B to the grid of V6A, thereby cutting V6A off. In all ranges from the acquisition radar range setting to the limit of the radar range, V6A and V6B establish the leading edge and V7A and V7B establish the trailing edge of the sector range waveform.

(7) Gate mixer V4 is a coincidence tube that combines the acquisition azimuth gate with the range gate pulse from V6B (F, fig. 13). The acquisition azimuth gate (A, fig. 14) is applied through connector P1–1 to terminal 1 of AZ variable resistor R12. The gate developed across R12 is picked off by the brush arm and applied to the control grid of V4. The acquisition azimuth gate is a sinusoidal voltage with a pip at the peak of each alternation of the sinusoid. The frequency of the sine

wave is determined by the speed of rotation of the acquisition antenna, one revolution per sine wave cycle. The center of the pip occurs in coincidence with the acquisition azimuth line (flashing line on the PPI).

(8) Variable resistor R12 regulates the amplitude of the acquisition azimuth gate that is applied to V4. Because of the negative dc reference, the lower the amplitude of the acquisition azimuth gate applied to V4 the narower the alarm control azimuth sector will be. This limit approaches 53 mils (3°) when the dc base line is near −70 volts. This condition is encountered when R12 is set fully counterclockwise. Then V4 is cut off except for a short time at the pip of the acquisition azimuth line. Since this pip appears at the peak of the sinusoid, the alarm sector is centered about it. With resistor R12 set fully clockwise, the control grid of V4 is at ground potential at all times and the sector azimuth coverage is 6,400 mils (360°).

(9) The range gate pulse (F, fig. 13), applied through resistor R19 to the suppressor grid of V4, occurs at the radar pulse repetition frequency, and its duration determines the range over which the alarm control will operate. Capacitor C10 charges to average suppressor current and sets the bias level of V4. Resistor R19 prevents excessive loading of multivibrator V6B and together with R26 provides a grid leak discharge path for C10. Mixer V4 is driven to conduction only on simultaneous application of positive-going pulses to the control grid and the suppressor grid. The input range gate pulse to the suppressor grid is shown in an expanded form (F, fig. 13) for purposes of clarifying the discussion. In reality, the range gate pulse can be extended to 1,300 microseconds maximum duration and many such pulses (B, fig. 14) can be gated through V4 depending

A   INPUT TO V4

53.2 MILS (3°)

0

DC LEVEL
SETTING
OF R12

7ll
MILS
(40°)

–70V

6400 MILS (360°)

B   OUTPUT FROM V4

C.   INPUT TO VI

D   OUTPUT FROM V2
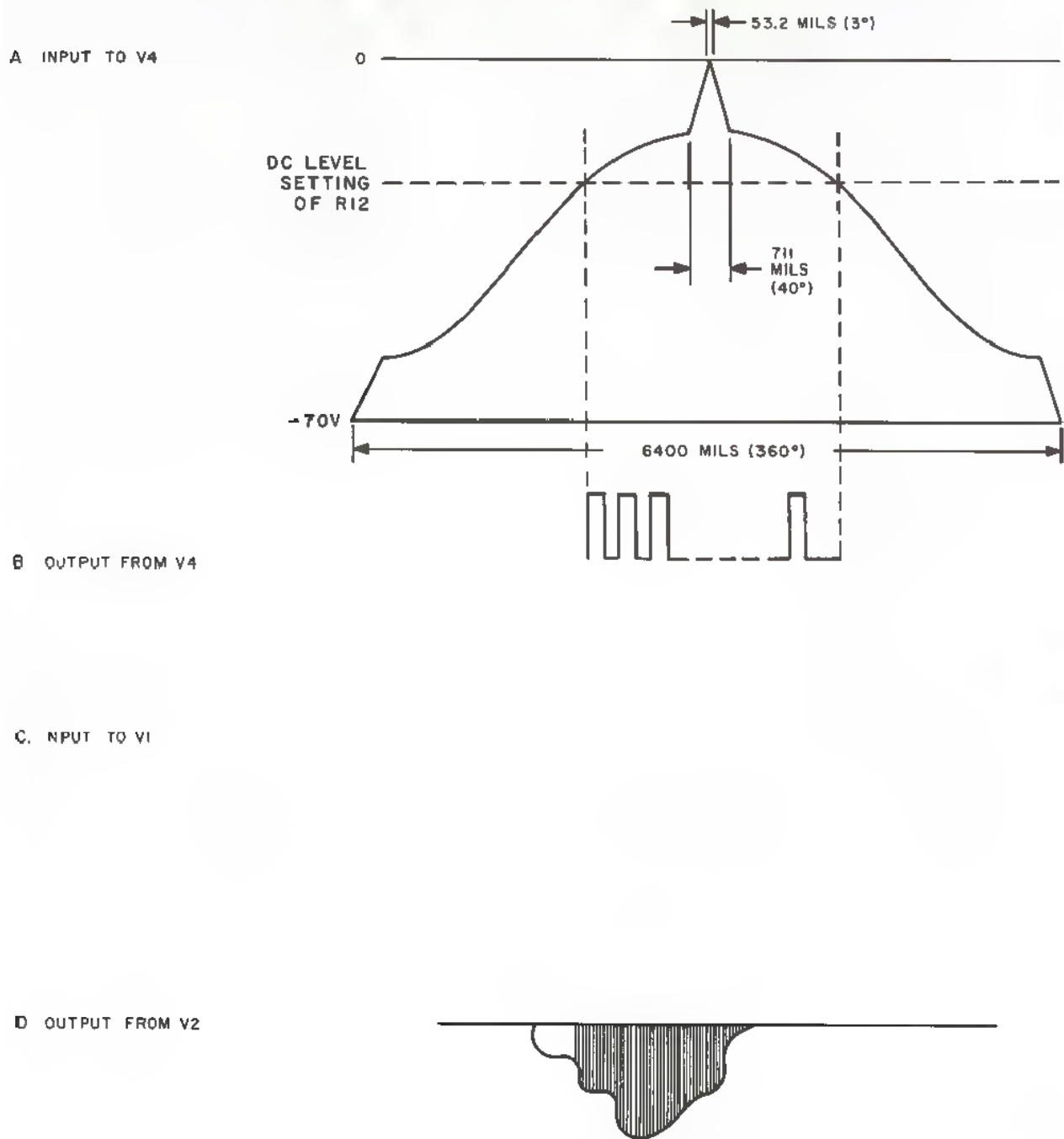
RA PD 467993

Figure 14. (U) Alarm control waveforms—V1 through V4

144

upon the duration (set by R12) of the acquisition azimuth gate.

(10) Assume R12 is set to the dc level indicated by the dotted horizontal line in A, figure 14. On conduction of V4, a series of range gate pulses (B, fig. 14) are passed through V4 during the interval between the dotted vertical lines and are developed across plate load resistor R15 and decoupled from the power supply by capacitor C7B. The range gate pulses, coupled through capacitor C8, are then applied to the control grid of gate amplifier V5.

(11) The positive portion of each gate pulse is clipped by crystal diode CR8. The remaining portion is inverted in gate amplifier V5, and then developed across plate load resistor R17. Resistor R16 is a parasitic suppressor, and capacitor C7C bypasses the power supply. Voltages developed across cathode resistor R14 are sampled at test point TP1 with an external oscilloscope when making internal adjustments. The negative portions of the positive gate pulses from the plate of V5 are clipped off by crystal diode CR5. Crystal diodes CR8 and CR5 provide a quick recovery path for coupling capacitors C8 and C9, respectively. This prevents signal biasing by allowing C8 and C9 sufficient time to recharge between successive gate pulses when alarm sector range is fully extended. The clipping level of CR5 is set at −13.15 volts by the voltage divider consisting of resistors R18 and R20 connected to the −250-volt supply. The series of range gate pulses (B, fig. 14) is coupled from the junction of C9 and CR5 to video and gate mixer V2.

(12) Video amplifier V1 (fig. 26, TM 9-1430-257-20), video and gate mixer V2, and audio amplifier V3 combine the video signals with the 500-cps range gates from V5. Video signals (D, fig. 14) are coupled through connector J1 and capacitor C1 to the control grid of V1. Be-

cause of rapid recovery requirements the control grid of V1 is terminated by crystal diode CR1 instead of the customary grid return resistor. The positive portion of the signal above the dc level is clipped by CR1. Since CR1 does not shunt the negative signals, its back resistance (approximately 50,000 ohms) serves as the grid return. The negative signals are developed across this resistance and appear inverted and amplified at the plate of V1. Resistor R2 is the plate load and R1 is a parasitic suppressor. Capacitor C3A bypasses the power supply and cathode resistor R3 provides the bias for V1. A clipped and inverted facsimile of the input video signal is applied from the plate of V1, through coupling capacitor C2 to the control grid of V2. Again due to recovery requirements, the signal level is clipped by crystal diode CR2. The clipping level can be adjusted by means of VID ALARM THRESHOLD variable resistor R5 located in the acquisition control-indicator. Resistor R5 (fig. 21, TM 9-1430-257-20) is the grid return, and resistor R4 (fig. 26, TM 9-1430-257-20) and capacitor C20 form a decoupling network used to prevent video signals from entering the −250-volt supply. The 500-cps series of range gates is applied to the suppressor grid of V2.

(13) Any video signal appearing in the sector arrives in coincidence with the series of 500-cps gates and drives V2 into conduction. These signals are inverted in V2 and developed across plate load resistor R7 (D, fig. 14). The screen grid voltage is dropped through resistor R41 and bypassed by capacitor C19. Resistor R6 is a parasitic suppressor and capacitor C3C is a plate bypass.

(14) A pulse stretcher consisting of crystal diode CR3, capacitor C4, and resistor R9 is included in the plate circuit of V2. When V2 conducts, the plate drops due to electron current conduction. Since the

cathode of CR3 is now at a lower level than the plate of CR3, current flows from V2 through CR3 and charges C4. When V2 is swinging toward cutoff, the plate voltage rises and blocks CR3. The junction of R6, R7, and C4 also rises, and C4 can discharge toward this junction only through R9. The delaying action of this RC circuit extends the duration of the audio signal that is coupled through capacitor C5 and developed across resistor R10, then applied to audio amplifier V3. This stage amplifies the audio and drives output transformer T1. Capacitor C18 resonates the transformer primary at an audible frequency (500-cps). This resonant circuit is a frequency selective circuit used to eliminate the noise content of the audio signal.

(15) The audio is coupled to an external speaker from impedance matching terminals 3 and 5 of the secondary of T1. These terminals are coupled through connector P1-3 and P1-4 to the speaker, which is mounted in the upper right-hand corner of the horizontal plotting-board cover (A6, fig. 3, TM 9-1430-257-20). Volume is regulated by means of video alarm volume control variable resistor R31 (A5, fig. 3, TM 9-1430-257-20) located next to the loudspeaker terminals behind the horizontal plotting-board cover.

(16) The auto alarm is energized by closing switch S8 (fig. 21, TM 9-1430-257-20) which is on the same shaft as VID ALARM THRESHOLD variable resistor R5. Closure of S8 energizes video alarm relay K1 (fig. 26,

TM 9-1430-257-20). In turn, 6.3 volts is applied to the filaments of all vacuum tubes except V6, through K1 relay contacts 7 and 12. The filament of V6 is energized through contacts 5 and 11. In order to maintain minimum difference of potential between the cathode and filament of V6, the filament is returned to -250 volts through limiting resistor R23.

20.1 (CMHA) Alarm Control - 8158475

a. General. Beginning with system 1071, alarm control - 9000450 (par. 20) is replaced by alarm control - 8158475. The alarm control provides an audible warning as a supplement to visual observation. An external 4-inch speaker produces a 500-cps tone if a target signal appears in a selected sector on the acquisition PPI presentation. The alarm control utilizes preknock, video, acquisition azimuth gate, and acquisition range mark signals to produce the audible alert. The covered sector is adjustable in azimuth from 3 to 360 degrees centered about the acquisition (flashing) azimuth line and extends in range from zero to full radar range, which is 250,000 yards.

b. Detailed Theory.

(1) Monostable multivibrators V7A and V7B (fig. 26.1, TM 9-1430-257-20) determine the outer limit of the sector range for the alarm control circuits. During quiescence V7B is conducting and V7A is cut off. The control grid of V7B is clamped at approximately -225 volts by action of clamper V5B which fixes a reference level for one side of capacitor C15. Clamper V5B is essentially part of a voltage divider consisting of resistor R42 and C19 in parallel, V5B, and resistor R29

which is the plate load resistor for V5B and the grid load resistor of V7B. Resistor R42 and R14 form a voltage divider between -250 volts and ground to produce cathode bias voltage for V5B. Capacitor C19 maintains the voltage drop across R42 at a constant potential. When the grid of V7B tends to go more positive than -225 volts, V5B increases conduction which maintains the grid of V7B at -225 volts. When the grid of V7B tends to go more negative than -225 volts, V5B reduces conduction allowing normal operation of V7B to take place. Resistor R40 is a common cathode resistor for V7A and V7B. Resistor R24 in parallel with capacitor C9 prevents switching transients in the cathode circuit from triggering the multivibrators. Resistor R30 is the plate load resistor of V7B. Multivibrator V7A is cut off by the voltage developed across R40 during the conduction of V7B. With V7A cut off, clamper V5A maintains the plate of V7A and the other side of C15 at approximately ground potential. This action establishes the positive level (B, fig. 13) for all square waves that originate at V7A between preknock pulses. Resistors R22 and R28 are the common plate load resistors of V7A and V5A. Capacitor C3B is a decoupling capacitor preventing rf signals of V7A from entering the +150-volt supply.

(2) A positive preknock pulse (A, fig. 13) is coupled through connector J3 (fig. 26.1, TM 9-1430-257-20), capacitor C16 and resistor R38 to the control grid of V7A. The setting of BIAS variable resistor R37 controls the bias level for V7A which is varied from -233 to -250 volts. Variable resistor R37 and resistor R36 form a voltage divider between -250 volts and ground for developing the bias voltage for V7A. Capacitor C17 decouples the preknock pulse from the -250-volt supply. The preknock pulse is developed across resistor R39, part of R37, and R38. The negative excursion limit of the pulse is set by R37 and clipped by crystal diode CR4. When the lower extremity of the pulse drops below the plate potential of CR4, this diode conducts and shunts R39, thereby virtually grounding the pulse.

(3) The preknock pulse applied through R38 to the control grid of V7A drives V7A into conduction. By controlling the bias on V7A, R37 controls the plate current through V7A during conduction. Consequently, R37 controls the level of the terminal voltage for charging C15. During the period that V7A is cut off, C15 charges toward +150 volts. However, when C15 is charged slightly above ground potential (approximately +0.5 volts) V5A conducts keeping C15 at ground potential. When V7A conducts, plate voltage of V7A and V5A decreases, cutting off V5A. Electron current flows from ground through R24, R40, and V7A to the plate side of C15 for a duration established by the setting of R37. In this manner the pulse width of the square wave at the plates of V7A and V7B can be varied from 0 to 1600 microseconds (minimum).

(4) The negative-going square wave

(B, fig. 13), applied from the plate of V7A through C15 to the grid of V7B, is inverted by V7B producing a positive-going square wave (C, fig. 13) at the plate of V7B. The leading edge of the output square wave from V7B is in time coincidence with the preknock pulse. The space between the leading and trailing edges of the square wave is variable in time (0 to 1600 microseconds) representing zero to full radar range. The output square wave is differentiated by capacitor C13 and resistor R21. The positive swing (leading edge) of the differentiated pulse is clipped by the blocking action of crystal diode CR7. The negative swing (trailing edge) (D, fig. 13) is applied to bistable multivibrator V6A.

(5) Gate mixer V4 is a coincidence tube that combines the acquisition azimuth gate and the acquisition range mark. The acquisition azimuth gate (A, fig. 14) is applied through connector P1-1 and developed across AZ variable resistor R12. The gate developed across R12 is picked off by the brush arm and applied to the suppressor of V4. The acquisition azimuth gate is a sinusoidal voltage with a pip at the peak of each alternation of the sinusoid. The frequency of the sine wave is determined by the speed of rotation of the acquisition antenna, one revolution per sine wave cycle. The center of the pip occurs in coincidence with the acquisition azimuth line (flashing line on PPI). The acquisition azimuth gate at the brush arm of R12 will not drive V4 into conduction unless the control grid is raised above cutoff by the acquisition range mark. The acquisition range mark (E, fig. 13), coupled through connector J2, is differentiated by capacitor C21 and resistor R16 at the control grid of V4, resulting in an extremely sharp leading edge of the pulse. The acquisition range mark is a positive 0.5-microsecond pulse that varies along the time base according to the acquisition radar range setting. Control grid bias for V4 is -13.5 ±2.5 volts developed by the voltage divider consisting of resistors R20 and R18 connected between -250 volts and ground.

(6) Variable resistor R12 regulates the amplitude of the acquisition azimuth gate that is applied to the suppressor grid of V4. Because of the negative dc reference, the lower the amplitude of the gate applied to V4, the less time the suppressor grid is above cutoff. Consequently, the alarm control azimuth sector is narrower. The sector approaches 53 mils (3 degrees) when the dc level (setting of R12)' is near -70 volts. Then the suppressor grid of V4 is cut off except for a short time at the pip of the acquisition azimuth gate. Since this pip appears at the peak of the sinusoid, the alarm sector is centered about it. When the setting of R12 is near ground potential, the suppressor grid of V4 is above cutoff for the entire period of the acquisition azimuth gate. This results in an azimuth sector coverage of 6400 mils (360 degrees).

(7) The differentiated acquisition range mark at the control grid

of V4 occurs at the radar pulse repetition frequency and determines the range over which the alarm control operates. Mixer V4 conducts only when the suppressor grid and control grid are simultaneously above cutoff. When V4 conducts, the signal at the plate is a series of negative-going pulses. The number of pulses is determined by the azimuth sector coverage (setting of R12). The negative-going pulses at the plate of V4 are differentiated by capacitor C8 and resistor R17. The negative swing (leading edge) is coupled through crystal diode CR5 and applied to bistable multivibrator V6B. The positive swing (trailing edge) is clipped by the blocking action of CR5. Resistors R13 and R15 are plate load resistors. Resistor R13 is also a screen dropping resistor and capacitor C7B is a screen bypass capacitor.

(8) Bistable multivibrators V6A and V6B produce the range gate pulse for gating video and gate mixer V2. Two pulses are required to complete one cycle of operation for V6A and V6B. When power is initially applied to the alarm control either V6A or V6B conducts. After the first complete cycle of multivibrator action V6B is normally conducting and V6A is cutoff by the voltage drop developed across common cathode resistor R34. Capacitor C14 prevents cathode signals of V6A and V6B from entering the -250-volt supply. The negative pulse coupled through CR5 is coupled through capacitor C11 and resistor R31 in parallel to the grid of V6B. The negative pulse at the grid

of V6B, cuts off V6B resulting in a positive pulse at the plate. The positive pulse at the plate is coupled through capacitor C12 and resistor R32 in parallel with the grid of V6A and drives V6A into conduction. Both V6A and V6B will remain in this state until another trigger changes the condition. The negative pulse coupled through CR7 is coupled through C12 and R32 in parallel with the grid of V6A, cutting off V6A. The resultant positive pulse at the plate of V6A is coupled through C11 and R31 to the grid of V6B, driving V6B into conduction. The pulse coupled through CR5 determines the start of the output pulse from V6B and is variable along the time base as the acquisition radar range setting is varied. Termination of the output pulse from V6B is determined by the pulse coupled through CR7. This pulse is variable from 0 to 1600 microseconds (minimum) as determined by the setting of R37. The output pulse at the plate of V6B (F, fig. 13) is a square wave variable from 0 to 1600 microseconds. The leading edge is determined by the pulse coupled through CR5 and the trailing edge by the pulse coupled through CR7.

(9) Video signals (C, fig. 14) are coupled through connector J1 and capacitor C1 to the control grid of V1. Because of rapid recovery requirements the control grid of V1 is terminated by crystal diode CR1 instead of the customary grid return resistor. The positive portion of the signal above the dc level is clipped by CR1. Since CR1 does not shunt the negative sig-

nals, its back resistance (approximately 50,000 ohms) serves as the grid return. The negative signals are developed across this resistance and appear inverted and amplified at the plate of V1. Capacitor C3A bypasses the power supply and cathode resistor R3 provides the bias for V1. A clipped and inverted facsimile of the input video signal is applied from the plate of V1, through coupling capacitor C2 to the control grid of V2. Again due to recovery requirements, the signal level is clipped by crystal diode CR2. The clipping level can be adjusted by means of VID ALARM THRESHOLD variable resistor R5 (fig. 21, TM 9-1430-257-20) located in the acquisition control-indicator. Resistor R5 is the grid return, and resistor R4 (fig. 26, TM 9-1430-257-20) and capacitor C20 form a decoupling network used to prevent video signals from entering the -250-volt supply. The 500-cps series of range gates is applied to the suppressor grid of V2.

(10) Any video signal appearing in the sector arrives in coincidence with the series of 500-cps gates and drives V2 into conduction. These signals are inverted in V2 and developed across plate load resistor R7 (D, fig. 14). The screen grid voltage is dropped through resistor R41 and bypassed by capacitor C7A. Resistor R6 is a parasitic suppressor and capacitor C3C is a plate bypass.

(11) A pulse stretcher consisting of crystal diode CR3, capacitor C4, and resistor R9 is included in the plate circuit of V2. When V2 conducts, the plate drops due to electron current conduction. Since the cathode of CR3 is now at a lower level than the plate of CR3, current flows from V2 through CR3 and charges C4. When V2 is swinging toward cutoff, the plate voltage rises and blocks CR3. The junction of R6, R7, and C4 also rises, and C4 can discharge toward this junction only through R9. The delaying action of this RC circuit extends the duration of the audio signal that is coupled through capacitor C5 and developed across resistor R10, then applied to audio amplifier V3. This stage amplifies the audio and drives output transformer T1. Capacitor C18 resonates the transformer primary at an audible frequency (500 cps). This resonant circuit is a frequency selective circuit used to eliminate the noise content of the audio signal.

(12) The audio is coupled to an external speaker from impedance matching terminals 3 and 5 of the secondary of T1. These terminals are coupled through connector P1-3 and P1-4 to the speaker, which is mounted in the upper right-hand corner of the horizontal plotting-board cover (A6, fig. 3, TM 9-1430-257-20). Volume is regulated by means of video alarm volume control variable resistor R31 (A5, fig. 3, TM 9-1430-257-20) located next to the loud speaker terminals behind the horizontal plotting board cover.

(13) The auto alarm is energized by closing switch S8 (fig. 21, TM 9-1430-257-20) which is on the same shaft as VID ALARM THRESHOLD variable resistor

R5. Closure of S8 energized video alarm relay K1 (fig. 26, TM 9-1430-257-20). In turn, 6.3 volts ac is applied to the filaments of all vacuum tubes except V6, through K1 relay contacts 7 and 12. The filament of V6 is energized through contacts 5 and 11. In order to maintain minimum difference of potential between the cathode and filament of V6, the filament is returned to −250 volts dc through limiting resistor R23.

20.2 (U). Fast AGC Amplifier 9990768

a. General. The fast AGC amplifier provides amplification of the bypass video, generates two video gate pulses (video gate 1 and video gate 2) and a jam strobe (JS) blanking pulse, and develops bias voltage used in the main IF amplifiers.

b. Detailed Theory.

(1) Resistor R2 is connected through bypass video connector J1 to the plate of amplifier V8B in the main acquisition IF amplifier (fig. 26.2, TM 9-1430-257-20), and functions as a plate dropping resistor to develop the bypass video. Capacitor C1 and resistor R1 provide filtering for the +150 volt supply. From R2, the signal is coupled through capacitor C2, developed across resistor R4 and coupled through parasitic suppressor resistor R3 to the input grid of amplifier V1. Crystal diode CR1 clamps out any positive going signals. Cathode bias for V1 is provided by resistor R6 and by capacitor C23, whose value is such that high frequency noise will be shunted out by increased bias. Resistor R67 is a screen grid dropping resistor, and resistor R5 is plate load for V1. Normal coupling from the plate of V1 to the grid of amplifier V2A is through capacitor C3 and C4 and resistor R8. When AGC ON relay K2 is energized, contacts 4-5 of K2 open, disconnecting C4, and while contacts 3-5 close, connecting resistor R7 in parallel with resistor R8, decreasing the time constant of coupling network. This fast time constant will differentiate large clutter and jamming signals in the bypass video. Crystal diode CR2 maintains the positive going video while bypassing unwanted negative signals. V2A amplifies the video signal, developing it across the plate resistance. Part of the developed video is fed from the wiper arm of BYPASS VID GAIN variable resistor R10 through capacitor C5 to BYPASS VIDEO OUT connector J2. BYPASS VID test point TP1 enables monitoring of the video output. The output of V2A is also coupled through capacitor C6 and parasitic suppressor resistor R12 to the control grid of high gain amplifier V3. Resistor R13 develops the signal, with crystal diode CR3 bypassing unwanted positive signals. Zener diode CR19 maintains a constant voltage on the screen grid, while unbypassed resistor R16 in the cathode increases stability. Resistor R14 and capacitor C24 act as a rf decoupling network for the +250 volt supply. AGC TST test point TP2 provides monitoring of V3 output. The signal is developed by V3 plate load resistor R15 and coupled through capacitor C8, resistor R17, a fast reacting network consisting of resistors R18, R19, R20, and capacitor C9, C10 and crystal diode CR5 to the grid of cathode follower V4A. With normal signals and without excessive clutter, C9 is charged through R20 and R19 to an average dc level, which in turn sets the conduction level of V4A. When excessive clutter starts, C9 charges to a higher positive level. Increasing the dc level ungates CR5, which couples the differentiated clutter noise directly from V3 through R18 and C10. CR4 removed negative going signals.

(2) From the plate of cathode follower V4A, the video signal is gated by crystal diodes CR6 through CR9. With AJD ON relay K1 deenergized, positive and negative going 23 microsecond gates are fed, respectively, through contacts 1-9 and 3-10 of K1

and resistors R22 and R23 to the diodes. The purpose of gating the bypass video when not in AJD is to provide a reference bias level for the AGC circuit so that fast AGC will take effect quickly when switching to AJD operation. After the video is switched through CR6 through CR9, the signal is coupled through resistor R73 and across capacitors C25 and C11 to the control grid of cathode follower V4B. If the AJD mode is in operation, contacts 8-12 of K1 close and the signal is applied directly from the gating diodes to the grid of V4B. With K1 deenergized, C11 and C25 charge to a given dc level through R73. Excessive clutter raises this dc level of C11 and C25, ungating crystal diode CR20 and permitting C11 and C25 to charge through R72, greatly reducing the time constant of the charging network. The change in time constant differentiates the clutter, leaving the target IF signal stronger than the total returns.

(3) The cathode circuit of V4B is composed of resistors R24, R26, and AGC ADJ variable resistor R25. R25 is adjusted when installed in the operating system. The voltage level from R25 is fed through resistor R27 to the grid 3 of amplifier V5. The signal is cathode coupled to cathode 7 of V5, where it is amplified and then coupled from the plate through resistor R33 to the control grid of amplifier V6A. The output of V6A is coupled through capacitor C12 in parallel with resistor R37 to the control grid of cathode follower V6B. C12 increases the response of the dc coupling between V6A and V6B. The output of V6B is coupled through parasitic suppressor resistor R40 to the control grid of driver V7A. V7A and V7B form a degenerative feedback output stage providing a stable dc level. From the plate of V7A the signal is coupled through resistor R43 and capacitor C15 to the grid of V7B. The cathode voltage of V7B is provided by the −250v supply. The plate output signal of V7B is fed through contacts 2-6 of energized, AGC ON relay K2. Also from the plate of V7B the signal is fed back to the cathode of V7A to provide degeneration, and through resistors R30, R29, and R28 to provide in-phase polarity to the grid of V5. For stages V5 through V7, resistors R31, R35, and R42 are plate dropping resistors, and resistors R33, R34, R37, R38, R43, and R44 are dc coupling resistors. Resistor R41 and capacitor C13 provide decoupling and isolation of +150v supply in the plate circuit of V7A.

(4) Multivibrator V9 is a modified, cathode coupled, one shot multivibrator. A positive preknock pulse is coupled from PREKNOCK IN connector J3 through capacitor C16 and crystal diode CR10 to control grid 2 of V9. Resistors R49 and R51 block negative signals from pin 2 of V9. When a positive signal is applied on pin 2 of V9, there is a decrease in voltage at plate 1, an increase in positive bias at cathode 8, and a decrease in plate current and an increase in plate voltage at plate 6. This condition causes C19 to discharge through GATE LG variable resistor R57 sufficiently to cut off the current at plate 6, causing C18 to charge. After 23 microseconds, the charging of C18 through R50 and R51 makes grid 2 sufficiently negative to cut off the current at plate 1. Capacitor C17 increases response for C18 and R50. From the junction of resistors R52 and R53, negative-going square waves are fed to VID GATE 2 OUT connector P1-3, to crystal diodes CR14, CR15, and to GATE 2 test point TP5. From the junction of R54 and R55, positive-going square waves are fed to VID GATE 1 OUT connector P1-1, to crystal diodes CR12, CR13, to GATE 1 test point TP4, and through capacitor C21 and resistor R64 to the grid of amplifier V2B. Resistors R63 and R64 provide a bias of negative 60 volts to the grid of V2B.

When a positive going 68 volt square wave is coupled through C21 to V2B grid of the signal is amplified and coupled through capacitor C22 to JS BLANKING OUT connector P1-5. Multivibrator V8 is used in conjunction with zenner diodes CR11 and CR16 to provide sharp on-off operation of V9 and to maintain the square wave outputs at a plus and minus 68 volts level. V8 is normally conducting which provides maintenance current for CR11 and CR16. When V9 plate voltage changes, this voltage is applied to the grids and cathodes of V8, which limits overshoots on V9. The 68 volt square wave outputs are fed through contacts 3-10 and 1-9 of deenergized relay K1 in normal or AGC operation mode. The 23-microsecond square wave ungates the diode bridge at the output of V4A and allows the bias level of the amplifier and driver output to be established for jamming signal during the preknock to sync pulse period. This action insures that all target returns will be amplified at a level for maximum detection of targets during jamming or excessive clutter.

(5) Relay K1 is energized when AJD switch S20 in the acquisition and IFF control-indicator is set to AJD position, closing contacts 11-6 and providing a ground path for AGC ON relay K2, and thereby insuring that K2 is always energized when using the AJD mode of operation. K2 can be energized independently by setting GAIN variable resistor R3 in the acquisition and IFF control-indicator fully clockwise which closes switch S22 and provides a relay ground for K2. Resistors R47 and IF GAIN ADJ R48 through contacts 1-6 of deenergized K2 is a manual IF gain adjustment. Resistor R70 connected to the −250 volt supply maintains the filament circuit of V9 at −250 volts dc level, thereby preventing damaging from the cathode of V9 which operates near a −250 volt level. Voltage networks composed of R59 through R62 provide a constant ungating voltage for crystal diode bridge CR6 through CR9 during AJD operation.

21 (U). 4-KC Oscillator 8512062

a. *General.* The 4-kc oscillator generates a 4-kc sine-wave carrier signal for use in the indicator system of the acquisition radar.

b. *Detailed Theory.*

(1) Oscillators V1A and V1B (fig. 28, TM 9-1430-257-20) form a push-pull oscillator. The frequency of oscillation (4-kc) is determined by the resonant frequency of the tank circuit composed of inductor L1 and capacitors C1, C2, and C3. Regenerative feedback from the plate circuit of V1A to the grid circuit of V1A is accomplished by the autotransformer action of L1 and by the coupling action of C3. Regenerative feedback from the plate circuit of V1B to the grid circuit of V1B is accomplished by the autotransformer action of L1 and by the coupling action of C1. Degenerative feedback from the plate circuit of V1A to the grid circuit of V1A is provided by C1 and C2 in series. Degenerative feedback from the plate circuit of V1B to the grid circuit of V1B is provided by C3 and C2 in series. The degenerative feedback offsets some of the regenerative feedback and prevents V1A and V1B from being driven alternately into cutoff and into saturation, thus preserving the sinusoidal waveshape of the oscillator output. Resistors R1 and R3 are grid return resistors for V1A and V1B, respectively.

(2) The plate voltage of the oscillator is determined by setting ACQ ADJ variable resistor R5, a part of the voltage divider consisting of R4, R5, and R6. The plate voltage determines the amplitude of the 4-kc sinewave signal supplied by the oscillator to push-pull power amplifiers V2 and V3. Capacitor C4 keeps the 4-kc signal out of the power supply.

(3) Push-pull power amplifiers V2 and V3 amplify the 4 kc sinewave signal received from V1. Resistors R7 and R12

isolate the oscillator from the power am-

plifiers. The 4-kc signal at the plate of V1A is coupled through R7 and capacitor C5 to the grid of V2. Grid signals of V2 are developed across grid resistor R9. The 4-kc signal at the plate of V1B is coupled through R12 and capacitor C6 to the grid of V3. Grid signals of V3 are developed across grid resistor R11. Resistors R10 and R19, common cathode resistors for V2 and V3, provide degeneration, thus preserving the sinusoidal waveshape of the 4-kc signal. Resistors R10 and R19 are in parallel to provide greater power handling ability of the circuit. Resistors R8 and R13 provide degenerative feedback for minimizing harmonic distortion in the output

(4) The 4-kc output signal from V2 and V3 is fed through connector P1-9 and 11 to the primary winding of output transformer T3. Transformer T3, shown in phantom in figure 28, TM 9-1430 257-20, is mounted separately from the chassis of the 4-kc oscillator assembly. The secondary winding of T3 supplies the 4-kc signal to the input of cathode follower V4 through P1-3. At the input of V4, the 4-kc signal is impressed across a voltage divider consisting of resistor R14, LINE ADJ variable resistor R18, and resistor R15. The setting of R18 determines the amplitude of the 4-kc signal coupled through C7 to the grids of V4.

(5) Cathode follower V4 is a dual-triode tube whose like elements are paralleled externally to provide greater power handling ability. Bias voltage is obtained from the junction of cathode resistors R16 and R17, which are shunted by inductor L2. The inductor and cathode resistors in parallel establish the quiescent state of V4. The inductor serves as the load impedance across which the 4-kc output signal is developed. Capacitor C8 prevents dc voltage, present at the cathode, from entering the external line slew resolver through P1-5. This line slew resolver

acts as an inductive load to the cathode follower output. Capacitor C9, connected in shunt with this inductive load, effectively cancels current lag caused by the load, thereby minimizing power loss in the output line.

(6) CARRIER test point TP1 provides means for checking the voltage or waveshape of the signal input to cathode follower V4. ACQ test point TP2 provides means for checking the voltage or waveshape at terminal 2 of output transformer T3. LINE test point TP3 provides means for checking the voltage or waveshape of the signal output of V4.

22 (U). 20—30-Second Delay Timer 7620519

a. General. The 20–30-second delay timer is used to delay the application of plate voltage to thyratron rectifier tubes in the low-voltage power supplies. Although the delay timer is used in the acquisition radar to provide a 20-second delay, it is capable of providing from 18 to 30 seconds of delay. The delay period is determined by the setting of delay time variable resistor R11.

b. Detailed Theory.

(1) The —28 volts, connected across start relay K2 (fig. 29, TM 9-1430 257 20), energizes K2 and opens the relay contacts. This disconnects resistor R4 from the timer. Phase B of the 120-volt ac supply is connected across primary winding 1 2 of power transformer T1. Secondary winding 3–5 of transformer T1 supplies 750 volts ac to the plates of rectifiers V1A and V1B.

(2) The dc output of rectifiers V1A and V1B is filtered by R3 and C2 and then impressed across the voltage divider consisting of R6 and reference V2. The voltage drop across R6 is applied from cathode to plate of timers V3A and V3B, causing the plates to be positive with respect to the cathodes. Reference V2 maintains a constant 150 volts dc across a resistance-capacitance network comprised of R11, R5, and C1. Since the plate of V2 is connected to ground, the cathode of V2 is at —150 volts relative to

the plate. Capacitor C1 cannot change instantaneously; therefore, the entire 150 volts initially is dropped across R11 and R5. As a result, the grids of V3A and V3B are made 150 volts negative with respect to the cathode; plate current in V3A and V3B is cut off.

(3) Capacitor C1 now starts to charge exponentially, causing the voltage across R11 and R5 to decrease from 150 volts toward ground. As the voltage across R11 and R5 decreases, the grid bias of V3A and V3B decreases. After 20 seconds (assuming that R11 is set properly), the grid to cathode potential of V3A and V3B is reduced sufficiently to permit V3A and V3B to conduct. The plate current of V3A and V3B energizes end relay K1, causing the relay contacts to close. The contacts of K1, when closed, complete an external circuit through terminals 1-2 of connector P1. This circuit applies plate voltage to external thyratron rectifiers. When the —28-volt dc supply is removed from the delay timer circuit, start relay K2 connects resistor R4 across capacitor C1. This provides a discharge path for the capacitor and makes it ready for another timing operation.

22.1 (U). 5-Minute Delay Timer 9145194

a. General. The 5-minute delay timer delays the application of high voltage to the acquisition modulator, thereby delaying the application of high voltage to the magnetron. The 5-minute delay period allows the magnetron filament to reach proper operating temperature before high voltage is applied to the cathode.

b. Detailed Theory.

(1) Phase A of the 120-volt ac supply, applied at connector P1-14 (fig. 90, TM 9-1430-257-20) is applied to terminal 3 of timer M1 and to CR1. Phase A is rectified by half-wave selenium rectifier CR1. The rectified voltage, after being filtered by resistor R1 and capacitor C1, energizes start relay K1. Energizing K1 completes acquisition high-voltage interlock and indicator circuits and also starts the delay period by energizing the timing motor and solenoid in interval timer M1. Contacts 5-11 of K1 close, completing a portion of the acquisition high-voltage interlock circuit. Contacts 4-10 of K1 close, completing the circuit to the HIGH VOLTS PRE HEAT indicator lamp on the acquisition power control panel. Contacts 2-9 close, completing the ground circuit of the —28-volt supply to the for escape solenoid K30. The ground connection to motor B1 is made through contacts 3-10 of deenergized relay K2 and energized escape solenoid K3.

(2) When energized, the solenoid in timer M1 acts as an electromagnetic clutch to establish the mechanical drive between the motor and the sensitive switch. The motor is geared down. A spring-loaded lever, mounted on the shaft of the motor, is driven for 5 minutes through an angular rotation to actuate the sensitive switch. In the activated position, the switch completes the ground circuit of the —28-volt supply to energize end relay K2, marking the end of the 5-minute delay period. Contacts 10-4 of energized relay K2 breaks the 120v PAA return, thus stopping the motor. Contacts 5-11 of K2 close, completing the circuit controlling the application of acquisition high voltage. Contacts 7-12 close, applying —28 volts to the HIGH VOLTS READY indicator lamp on the acquisition power control panel. The path through the 5-minute delay timer for the +320 volts is from terminal 6 of connector P1 through contacts 2 and 9 of K2 through the heating element of thermal relay K4 to terminal 8 of connector P1.

(3) The heater element across terminals 2-3 of K4 is in series with the +320-volt plate supply to the acquisition trigger amplifier When excessive current is drawn by the acquisition trigger amplifier, the heater element of K4 causes the bimetallic contacts across terminals 5 and 7 of K4 to open the acquisition high-voltage interlock circuit.

(4) The sensitive switch in timer M1, once actuated, remains in the actuated position until the solenoid is deenergized by the removal of power from the 5-minute delay timer. When input power is removed, the spring-loaded lever, operating through an escapement attached to the shaft of the motor, resets the sensitive switch to the start position in approximately 3 seconds.

23 (U). 15-Minute Delay Timer 7614632 and Acquisition 5-Minute Delay Timer 9142969

a General. The 15-minute delay timer delays the application of high voltage and +320 volts to the acquisition modulator, thereby delaying the application of high voltage to the magnetron. The 15-minute delay period allows the magnetron filament to reach proper operating temperature before high voltage is applied to the magnetron cathode.

b Detailed Theory.

(1) Phase A of the 120-volt ac supply, applied at connector P1-14 (fig. 30, TM 9 1430 257 20) is rectified by half-wave selenium rectifier CR1. The rectified voltage, after being filtered by resistor R1 and capacitor C1, energizes start relay K1. Energizing K1 completes acquisition high-voltage interlock and indicator circuits and also starts the delay period by energizing timing motor B1 and escape solenoid K3 Contacts 5-11 of K1 close, com-

pleting a portion of the acquisition high-voltage interlock circuit. Contacts 4-10 of K1 close, completing the circuit to the HIGH VOLTS PRE-HEAT indicator lamp on the acquisition power control panel. Contacts 2 9 close, completing the ground circuit of the −28-volt supply to B1 and K3 The ground connection to B1 is made through the movable arm of normally closed sensitive switch S1.

(2) Escape solenoid K3, when energized, acts as an electromagnetic clutch to establish the mechanical drive between B1 and S1. Motor B1 is geared down. A spring-loaded lever, mounted on the shaft of B1, is driven for 15 minutes through an angular rotation to actuate S1 In the actuated position, S1 deenergizes B1 and completes the ground circuit of the −28-volt supply to energize end relay K2. Energizing K2 marks the end of the 15-minute delay period which began when K1 was energized. Contacts 5-11 of K2 close, completing the circuit controlling the application of acquisition high voltage. Contacts 7-12 close applying −28 volts to the HIGH VOLTS READY indicator lamp on the acquisition power control panel Other contacts of K2 complete the circuit for the application of +320 volts to the acquisition trigger amplifier of the acquisition modulator. The path through the 15-minute delay timer for the +320 volts is from terminal 6 of connector P1 through contacts 2, 9, 4, and 10 of K2 through the heating element of thermal overload relay K4 to terminal 8 of connector P1.
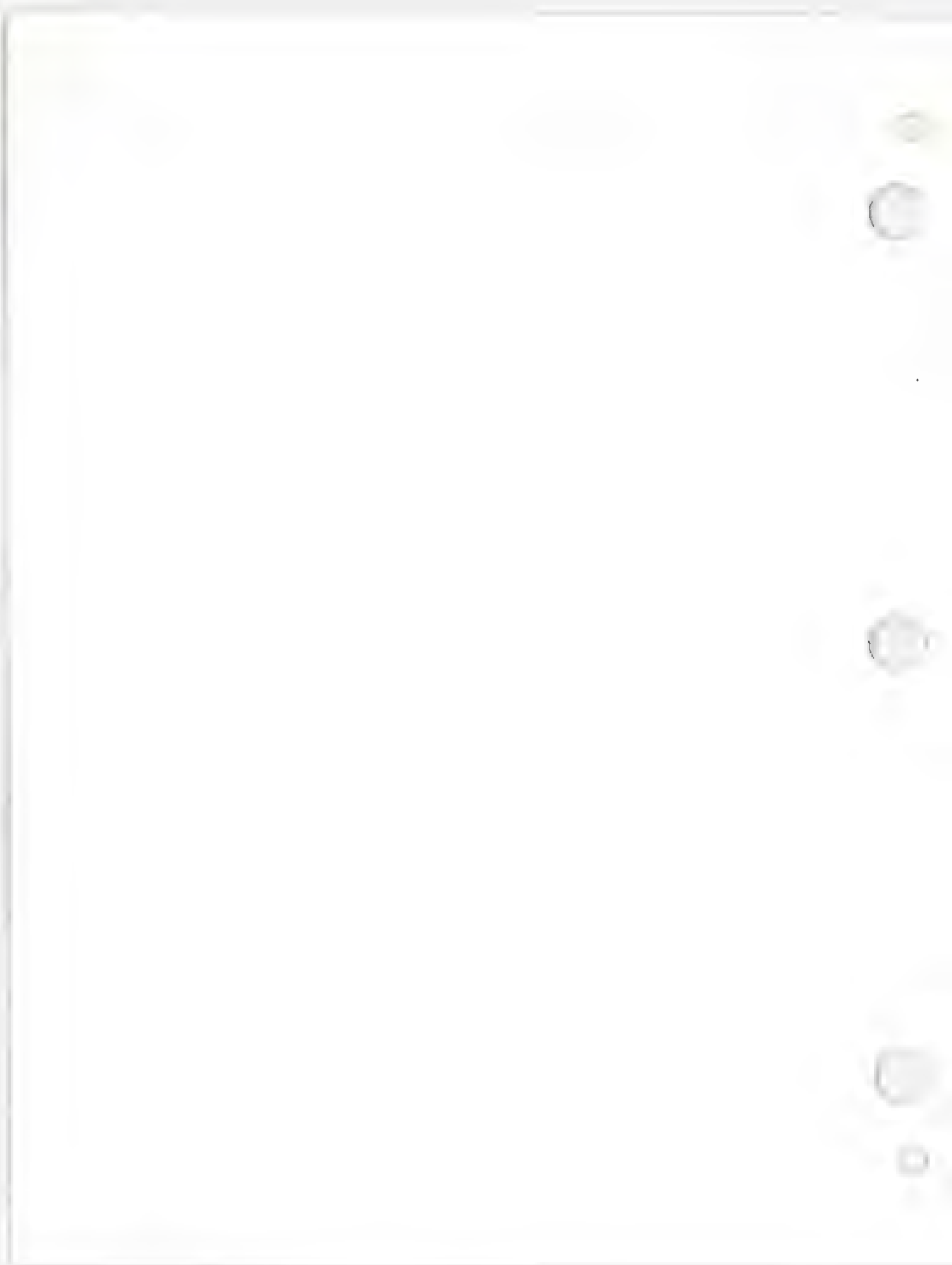
(3) The heater element across terminals 2-3 of K4 is in series with the +320-volt plate supply to the acquisition trigger amplifier. When excessive cur-

rent is drawn by the acquisition trigger amplifier, the heater element of K4 causes the bimetallic contacts across terminals 5 and 7 of K4 to open the acquisition high-voltage interlock circuit.

(4) Sensitive switch S1, once actuated, remains in the actuated position until escape solenoid K3 is deenergized by the removal of power from the 15-minute delay timer. When input power is removed, the spring-loaded lever, operating through an escapement attached to the shaft of motor B1, resets sensitive switch S1 to the start position in approximately 3 seconds.

c. Acquisition 5-Minute Delay Timer-9142969.

(1) Beginning with system 1287, acquisition 5-minute delay timer - 9142969 replaces 15-minute delay timer - 7614632 in order to reduce warm up time of the acquisition radar. The acquisition 5-minute delay timer - 9142969, uses a different timer unit requiring differences in its associated circuitry. The theory of the 15-minute delay timer covered in paragraphs a, b, and c applies for the acquisition 5-minute delay timer with substitution of 5-minute delay time for 15-minute delay time throughout the discussion. Other differences are discussed in (2) through (6) below.

(2) Phase A of the 120-volt supply applied to rectifier CR1 (fig. 30.1, TM 9-1430-257-20) through connector P1-14, is also applied to terminal 1 of timing motor B1.

(3) With sensitive switch S1 in the open position, closed contacts

2 and 9 of energized start relay K1 completes ground to escape solenoid relay K3 only.

(4) The ground connection to B1 is made from connector P1-15 through contacts 10 and 3 of deenergized K2 and through the contacts of energized K3.

(5) Energized K2 breaks the ground applied through contacts 3 and 10 to B1, ending the 5-minute delay period which began when K1 was energized.

(6) The path through the 5-minute delay timer for the +320 volts is from terminal 6 of connector P1 through contacts 2 and 9 of K2 through the heating element of thermal overload relay K4 to terminal 8 of connector P1.

24. (U) ±320V or +220V Power Supply 9140697

a. General. The ±320v or +220v power supply consists of two channels which are interconnected or strapped to provide various regulated dc voltages for use in the acquisition radar system. The three optional methods for strapping the power supply are shown as A, B, and C. When strapping method A is used, the power supply provides outputs of +320 volts and -320 volts. When strapping method B is used, the power supply provides outputs of +220 volts, +70 volts, and -250 volts. When strapping method C is used, the power supply provides two +320-volt outputs. Each channel of the power supply contains a full-wave thyratron-rectifier stage and a driver (regulator) stage.

b. Detailed Theory.

(1) Power supply strapped to produce two +320-volt outputs (C-strapping).

(a) The input to the power supply is furnished by the 3-phase, 400-cps power line.

Phase A enters at connector J1-A (fig. 31, TM 9-1430-257-20); phase B enters at J1-B; phase C enters at J1-K and L; and neutral enters at J1-C and J. Phase A to Phase C applies 208 volts ac to the primary winding of grid transformer T2; phase B to neutral applies 120 volts ac to the primary winding of plate transformer T1; and phase C to neutral applies 120 volts ac to the primary winding of filament transformer T3. Phase B is delayed externally for approximately 20 seconds to allow the filaments of rectifiers V10, V11, V30, and V31 to become heated before voltage is applied to the plates. Applying plate voltage before the cathode is heated to emission can result in pieces literally being pulled out of the cathode. When the power supply reaches proper operating temperature, thermostatic switch S1 operates and starts blower motor B1. B1 maintains the temperature of the power supply within the operating range. Capacitor C42 prevents pitting or burning of the contacts of S1. The channel containing rectifiers V10 and V11 and drivers V12A and V12B is referred to as channel A. The channel containing rectifiers V30 and V31, reference V33, and drivers V32A and V32B is referred to as channel B.

(b) In channel A, terminal 4 of T1 is connected to circuit ground through inductor L12 and connector J1-P. A sinusoidal 450 volts is applied to the plates of V10 and V11 from terminals 3 and 5 of T1. A sinusoidal 21 volts is applied to the grids from terminals 3 and 5 of T2. The sinusoidal voltage on the grids lags the sinusoidal voltage on the plates by 90° because of the phase difference in the sources supplying power to T2 and T1, respectively. Also present on the grids is a dc voltage applied from the plate of driver (regulator) V12B through terminal 4 of T2. Thus, the dynamic grid voltage for V10 and V11 is a composite voltage, one part of which is the 400-cps sine-wave signal from T2, and the other part of which is the dc voltage from the plate of V12B. The dc voltage from the plate of V12B varies inversely with changes in channel A output voltage, thereby either raising or lowering the level of the sine-wave signal on the grids of V10 and V11. Since V10 and V11 are gas-filled thyratron tubes, the grids control the start of conduction. Conduction starts when the plate is positive and a critical value of grid voltage is reached. Figure 15 indicates that if the level of the sine wave on the grids were raised to a greater extent than shown, the grid voltage would cross the conduction curve earlier in the positive half-cycle of plate voltage and make the period of rectifier conduction longer. Conversely, if the level of the sine wave on the grids were lowered, the grid voltage would cross the conduc-

tion curve later than shown in the half-cycle and make the period of rectifier conduction shorter. After conduction starts, the grid voltage exercises no control, and plate current is determined by plate voltage. Plate current continues to flow until plate voltage drops below the positive value necessary to maintain ionization of the gas in the tube. The dc charge built up across filter capacitors C14 and C17 as a result of thyratron rectification is directly proportional to the period of rectifier conduction. The capacitors, in conjunction with inductor L13, form a capacitor-input pi-type filter for reducing ripple in the dc output of the rectifiers. Resistors R11 and R12 limit the grid current of V10 and V11, respectively. Inductors L10 and L11 in the plate circuit of V10 and V11, respectively, and the two networks (R10, C10, C11 and R13, C13, C12) in the plate-to-cathode circuit of V10 and V11, respectively, suppress noise voltages inherent in thyratron operation. Inductor L12 suppresses undesirable frequencies which might originate in the unit powered by the power supply.

(c) Driver V12B controls the period of conduction of rectifiers V10 and V11 and, thereby, regulates the +320-volt output of channel A. Only one section of dual-triode tube V12 is used. Driver V12B senses any change in the dc output voltage of channel A and applies the change, in amplified and inverted form, to the grids of V10 and V11. The grid of V12B is connected to V ADJ SEC 1 (+) variable resistor R22. Variable resistor R22 is part of a voltage divider consisting of R21, R22, and R23. (Resistors R24 and R25 are not included in the circuit for strapping method C.) The voltage divider is connected between the +320-volt output (connector J1-D) and the regulated input reference of -250 volts (connector J1-F). Variable resistor R22 is adjusted to obtain an output of +320 volts at connector J1-D. Due to the voltage divider, the grid of V12B is slightly negative with respect to the cathode. To illustrate the regulation provided by V12B, suppose a change in external load requirements causes channel A output voltage to decrease from +320 volts to +317 volts. Because of the voltage - divider arrangement, slightly less than half of
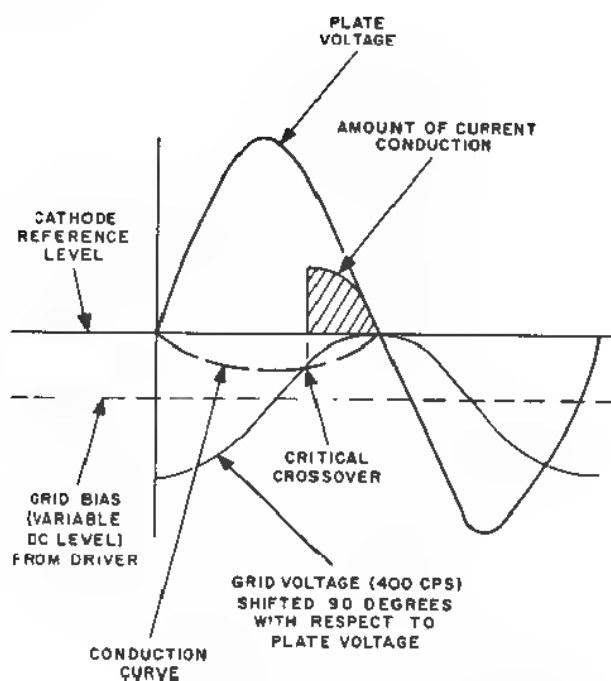
RA PD 467994

Figure 15 (U) Control of rectifier conduction

this voltage change appears at the grid of V12B. Since the channel output voltage is decreased by 3 volts, the grid of V12B becomes approximately 1.5 volts more negative. A more negative grid reduces current flow through V12B, causing the plate potential of V12B to rise or become more positive. Since the plate of V12B is connected to the grids of V10 and V11 through terminal 4 of T2, there is a rise in the dc voltage on the grids of V10 and V11. Thus, the period of conduction of V10 and V11 increases and returns the output voltage of channel A to the original value of +320 volts. Conversely, if channel A output voltage tends to rise above the +320-volt value, the grid of V12B becomes more positive and causes an increase in the current flow through V12B. The plate potential of V12B drops, causing dc voltage on the grids of V10 and V11 to decrease. Therefore, the period of conduction of V10 and V11 decreases to return the output voltage of channel A to the desired +320-volt level.

(d) Crystal diodes CR10 and CR11, with center-tapped winding 9-10–11 of T1, comprise a full-wave rectifier circuit which provides an additional +25 volts of plate voltage for V12B. This additional voltage allows the grids of V10 and V11 to go more positive than the cathodes, permitting regulatory action over a wider range when the channel output voltage tends to decrease. To illustrate the need for the additional +25 volts, assume that the top of plate load resistor R20 is connected to the channel output at J1-D instead of being connected to CR10 and CR11. With V12B conducting, there would then be some voltage dropped across R20, and the grids of V10 and V11 would be at some negative potential with respect to their cathodes. If the channel output voltage were to decrease

sufficiently to increase the negative bias voltage on the grid of V12B to plate current cutoff, the plate voltage of V12B could rise only to the value of the channel output voltage. Consequently, the grids of V10 and V11 could never go positive with respect to their cathodes, and an adequate range of regulation for decreases in channel output voltage could not be realized. Capacitor C15 and resistor R20 constitute an RC filter for the voltage from CR10 and CR11. Capacitor C16 is connected from the plate to the grid of V12B to prevent random fluctuations in channel output voltage from operating the regulation circuit. Resistor R19 prevents oscillations in V12B.

(e) Channel B is identical to channel A except for the driver (regulator) stage. The driver stage in channel B employs both sections of a dual triode, V32. Driver V32B controls regulation of the +320-volt output of channel B in the same manner as described for V12B of channel A. Driver V32A is cathode coupled to V32B. The grid of V32A is connected to circuit ground through resistor R35 and the parallel combination of resistors R34 and R47. Reference V33, shunted across the parallel combination of resistors R34 and R47, remains deionized and has no function in this particular application of the power supply. The cathodes of V32A and V32B are connected to the junction of resistors R36 and R37 on a voltage divider composed of R36, R37, and resistor R38. The voltage divider is connected between circuit ground (J2–C) and the externally supplied −250-volt reference input (J2–T). The cathode voltage of V32A and V32B is determined by the voltage divider and the total current through both V32A and V32B. The purpose of V32A is to keep the total current through V32A and V32B constant, thereby maintaining

CONFIDENTIAL

the cathodes of V32A and V32B at a constant potential. If V32A were not included in the circuit, changes in current through V32B would produce changes in the cathode potential of V32B. If this were the case, the voltage at the cathode of V32B could not serve as reference for output voltage changes sensed by the grid of V32B. Due to the cathode coupling between V32A and V32B, a change in current through V32B causes an equal but inverse change in the current through V32A. As a result, the total current through V32A and V32B remains constant. In strapping method C, just described, resistors R44 and R46 are not connected to the power supply circuit.

(2) *Power supply strapped to produce +220-volt, +70-volt, and −250-volt outputs (B-strapping).*

(a) The theory of the power supply strapped to produce a +220-volt, a +70-volt, and a −250-volt output (B-strapping) is similar to that of the power supply strapped for two +320-volt outputs (C-strapping).

(b) Channel A produces the +220-volt output. Channel B, when used in conjunction with an external regulator circuit, produces the +70-volt and −250-volt outputs.

(c) In channel A, the only change from C-strapping is in the grid circuit of driver V12B. Strapping to produce a +220-volt output adds resistors R24 and R25 in series with resistors R21, R22, and R23. The addition of resistors R24 and R25 permits the grid voltage of V12B to be set at a more positive value by means of V ADJ SEC 1 (+) variable resistor R22. As a result, the plate voltage of V12B is lower than in C-strapping. The lower plate voltage of V12B shortens the period of conduction of V10 and V11, thus causing the output of channel A to be +220 volts. Driver V12B is refer-

enced by the −250 volts developed in channel B.

(d) Channel B is externally connected to a 250, +250, or +150-volt regulator at connectors J1 H and G. In the absence of the externally connected regulator, channel B would develop a +320-volt output between J1–H and G. However, such an output would be floating or unreferenced to circuit ground. The regulator effectively connects a voltage divider, grounded at some point, across J1–H and G. A ground reference is established at a point on the effective voltage divider, which causes +70 volts to appear at J1–H and −250 volts to appear at J1–G. The 250 volts at J1 G is held constant by the action of the external regulator and is used to reference the driver (regulator) stage in each channel of the power supply. The +70 volts at J1–H is adjusted by V ADJ SEC 2 (− or +) variable resistor R42. Resistor R34 and V33 comprise a voltage divider connected between the +70-volt output terminal and the −250-volt output terminal. The constant 150-volt drop across V33 fixes a constant −100 volts on the grid of V32A. The cathodes of V32A and V32B are connected to the −250-volt reference through resistor R37. The cathode voltage is derived from the difference between the −250-volt reference and the voltage dropped across resistor R37. The voltage drop across resistor R37 is held constant by the constant current through V32A and V32B. Since the −250-volt reference and the voltage across resistor R37 are constant, it follows that the cathode voltage of V32A and V32B is also of constant value. The constant potential at the cathodes of V32A and V32B is used to reference output voltage changes that are sensed by the grid of V32B. Resistor R47 is connected across V33 to protect V32A

CONFIDENTIAL

and V32B during maintenance procedures involving the removal of V33 from its tube socket. Because of the manner in which the circuit is wired, resistor R34 is automatically disconnected when V33 is removed from the tube socket. Therefore, were it not for the action of resistor R47, the grid of V32A would be left floating and possible damage to the power supply could result. Resistor R47 returns the grid of V32A to −250 volts when V33 is removed from the tube socket, thus preventing excessive current from being drawn through V32A. In B-strapping, resistors R36 and R38 are not connected to the power supply circuit.

(3) *Power supply strapped to produce a +320-volt and a −320-volt output (A-strapping).*

(a) The theory of the power supply strapped to produce a +320-volt and a −320-volt output (A-strapping) is similar to that of the power supply strapped for a +220-volt, a +70-volt, and a 250-volt output (B-strapping).

(b) Channel A produces the +320-volt output; channel B produces the 320-volt output. Strapping in channel B grounds connector J2-F, thereby grounding the filament cathodes of rectifiers V30 and V31. Circuit ground is thus made common to both the +320-volt and −320-volt circuits. Since circuit ground cannot vary, it provides a stable reference for each channel.

(c) In channel A, the voltage divider composed of resistors R21, R22, R23, and R24 is connected between the +320-volt output and the −320-volt output of the power supply. This voltage divider provides the proper bias for the grid of driver V12B. The V ADJ SEC 1 (+) variable resistor, R22, is adjusted to provide a +320-volt output at J1-D.

(d) In channel B, resistor R34 and V33 are connected in series across the −320-volt output of the channel. Since the drop across V33 cannot change, a change in the −320-volt output will be developed across resistor R34 and be felt on the grid of V32A. The cathodes of V32A and V32B will follow the grid voltage change of V32A and alter conduction in V32B to the extent necessary for returning the output to −320 volts. A change in the −320-volt output also appears on the grid of V32B through voltage dividing resistors R41, R42, R43, and R44. The change in voltage on the grid of V32B opposes the action of the change in voltage at the cathode of V32B However, the change in voltage at the grid of V32B, due to the divider action, is proportionately less than the change in voltage felt on the cathode. Consequently, the cathode voltage change is more effective in controlling current flow through V32B. To illustrate this, assume that the output voltage of channel B goes to −322 volts. The grid of V32A becomes 2 volts more negative by the change felt across resistor R34 The cathodes of V32A and V32B follow the grid voltage of V32A. This causes V32B to increase conduction, resulting in a greater drop across load resistor R40. The drop across R40 is used to decrease the conduction time of V30 and V31 and thereby to restore the channel output to −320 volts. When the output voltage of the channel changes to −322 volts, the 2-volt change in output causes the grid of V32B to feel a voltage change of somewhat less than 1 volt. This change on the grid tends to decrease current flow through V32B. However, since the voltage change on the cathode at this time is more than twice as large as that on the grid, the cathode voltage will overcome the effect

of the grid voltage. Resistors R25 and R38 are shorted out and play no part in circuit operation

(e) When adjusting the power supply strapped for A-strapping, channel B should be adjusted before channel A. This is necessary because channel B supplies the —320 volts required for obtaining the proper bias for V12B. Therefore, V ADJ SEC 2 (· or +) variable resistor R42 must be adjusted to provide a 320-volt output from channel B before V ADJ SEC 1 (+) variable resistor R22 is adjusted to provide a +320-volt output from channel A.

25. +270V, —28V, and +75V or +175V Power Supply 8019210 or 9986425

a. General. The +270v, —28v, and +75v or +175v power supply is a 3-channel circuit which supplies unfiltered +270 volts, filtered —28 volts, and regulated +175 volts to various portions of the radar course directing central. The +175-volt channel may be connected to provide regulated +75 volts in place of the regulated +175 volts.

b. Detailed Theory.

(1) +270-volt channel. The +270-volt channel is a full-wave voltage rectifier employing two thyratron tubes, rectifiers V1 (fig 32, TM 9-1430-257-20) and V2. The control grid of each rectifier is connected to filaments through terminal 4 of filament transformer T2. This common connection between grids and filaments prevents the grids from exercising control, thus permitting the rectifiers to act as gas diodes. The input to the primary winding of T2 is 120 volts ac from phase C and neutral of the 3-phase, 400-cps power line. The input to the primary winding of power transformer T1 is 208 volts ac supplied from phase A to phase B of the 3-phase, 400-cps power line. The input to T1 is delayed externally for approximately 20 seconds to allow the filaments of V1 and V2 to heat before voltage is applied to the plates. Transformer T1 steps up

the 208-volt ac input to provide 600 volts ac across secondary winding 3 5. The center tap of the secondary winding is grounded to divide the 600 volts ac equally between the plates of V1 and V2. The 300 volts ac, applied between plate and ground of each tube, is rectified in the conventional manner. An unfiltered +270-volt output is taken from the filaments which appear across connectors J1-A and F.

(2) 28-volt channel. The —28-volt channel is a full-wave, selenium, bridge-type rectifier. The input to the primary winding of power transformer T3 is 120 volts ac supplied from phase C to neutral of the 3-phase, 400-cps power line. Transformer T3 steps down the 120-volt ac input to provide 39 volts ac across secondary winding terminals 3 and 8. The secondary winding can also be tapped at terminals 4, 5, 6, and 7 to provide four additional ac voltages ranging from 31 volts to 37 volts in increments of 2 volts. Terminal 6 supplies 35 volts ac to selenium bridge CR1 through CR4. The selenium bridge rectifies this ac voltage to produce the 28-volt output of the channel. Inductor L1 and capacitor C1 filter the —28-volt output. Rectifier output fuse F1 protects the —28-volt channel. Fuse indicator light I1 is a blown fuse indicator associated with F1.

(3) +75-volt or +175-volt channel.

(a) The +75-volt or +175-volt channel, consisting of voltage regulator V3 and resistor R1, provides either regulated +75 volts or regulated +175 volts to the computer or acquisition radar system, respectively. Regulator V3 is a gas-filled triode-type regulator connected as a diode. The output voltage of the channel depends upon the input voltage and the input connections.

(b) When the channel is connected to supply +75 volts to the computer, a +320-volt input is applied across the voltage divider consisting of resistor R1 and

V3. The cathode of V3, in this application, is connected to circuit ground. The voltage drop across V3 is the +75-volt output of the channel. Regulator V3 holds the +75-volt output constant over a fairly wide range of current drawn by the external load.

(c) When the channel is connected to supply +175 volts to the acquisition radar system, a +250-volt input is applied across the voltage divider consisting of V3 and the external load. Regulator V3 drops 75 volts of the +250-volt input. The remaining +175 volts, which is dropped across the external load, represents the output of the channel. Resistor R1 plays no part in this application of the channel.

26.(U) -1000V Power Supply 8519068

a. General. The -1000v power supply is a sealed unit which provides high voltage dc for the cathode-ray tube in the MTI oscilloscope. The power supply contains a power transformer, 32 silicon-diode rectifiers, a filter, and a bleeder network. The 32 silicon diodes are connected to form a full-wave bridge rectifier with eight silicon diodes in each leg of the bridge. The filter consists of one inductor and one capacitor. The bleeder network is composed of four identical resistors connected in series-parallel.

b. Detailed Theory. Refer to D32, figure 25, TM 9-1430-257-20. The input to the primary winding of the power transformer is 120 volts ac, 400 cps. The input is applied across terminals 1 and 3 of the transformer from phase B to neutral of the 3-phase, 400-cps power line. An input of 125 volts ac or 115 volts ac can be substituted across ter-

minals 1 and 2 or terminals 1 and 4 respectively, without affecting the output voltage. The line voltage is stepped up from primary to secondary, and a high voltage ac appears across the secondary winding of the transformer. This voltage is rectified by the silicon bridge and filtered by the inductor and capacitor. The rectified output appearing across terminals 5 and 6 of the power supply is 1,000 volts dc. Terminal 6 is positive with respect to terminal 5. The resistive bleeder network discharges the capacitor when input voltage to the transformer is removed.

27. (U)   +250 or +150 Volt Regulator 9137641

a. General. The +250 or +150 volt regulator is used with the ±320v or +220v power supply (par. 24) to provide the acquisition radar system with low impedance plate and bias supply voltages of +250 or +150 volts. Two optional methods of external connections (strapping) are used to obtain the desired output voltage.

b. Detailed Theory.

(1) Operation of regulator using +250-volt strapping.

(a) The input voltage of +320 volts from the ±320v or +220v power supply is applied to connectors P1-3 and 5 (fig. 33, TM 9-1430-257-20). The +320 volts is distributed to the +320-volt fused circuit and to the regulator circuit. On the fused circuit the +320-volt circuit path is through fuse F1 to connectors P1-7 and 9 where it is distributed to the acquisition radar system. Resistor R1 and the built-in resistance of fuse indicator light I1, which are normally bypassed by fuse F1, limit the current flow in the +320-volt path when fuse

F1 opens. The current flow through the resistors causes fuse indicator light I1 to illuminate. In the regulator circuit, the +320 volts is applied directly to the plates of series voltage regulators V1A, V1B, V2A, V2B, V3A, and V3B. The regulators, which are in series with the input voltage and the external load, present a constant 70-volt load to the input voltage. Dropping this 70 volts from the -320-volt inputs results in a regulated +250 volts which are applied to connectors P1-8 and 10 and to the control bias circuit. Capacitor C1 bypasses to ground any ac components of the output voltage.

(b) The control bias circuit, composed of voltage amplifiers V4A and V4B and driver V5, detects any change in the +250 volts, amplifies this change, and feeds a corrective bias to the grids of the regulators. The +250-volt output is applied through BALANCE variable resistor R21 to terminal 2 of impedance network Z1 where it is algebraically added to a -250-volt reference voltage. The reference voltage is applied to terminal 4 of Z1 through connector P1-4 from the ±320v or +220v power supply. The algebraic difference of the two voltages is applied from terminal 1 of Z1 to the grid of V4A as a bias voltage. Any ac components are developed across C5 and appear at the grid of V4A. If the +250-volt output increases, the resultant voltage at the grid of V4A increases, caus-

ing V4A to conduct more heavily. Resistors R8 and R9 form a voltage divider which determines the plate potential of V4A. The increased conduction of V4A causes an increase in the voltage drop across cathode resistor R12. Since the cathodes of V4A and V4B are common, the potential difference between the plate and cathode of V4B decreases, causing a decrease in the conduction of V4B. The RC network composed of resistor R13 and capacitor C2 bypasses to ground any sudden fluctuation of voltage appearing at the plate of V4B. Resistors R10, R11, R14, and R15 form a voltage divider which determines the plate potential of V4B and the grid potential of V5.

(c) The increased voltage on the plate of V4B is coupled by the RC network composed of resistor R14 and capacitor C3 to the grid of V5. The increased voltage on the grid of V5 causes V5 to conduct more heavily, and the voltage drop across plate load resistor R16 is increased, resulting in a decrease of potential at the plate of V5. The screen grid potential of V5 is determined by the voltage divider composed of resistors R18, R19, and R20. The decrease in potential at the plate of V5 is coupled by resistors R2 through R7 to the grids of V1A, V1B, V2A, V2B, V3A, and V3B. The decrease of potential on the grids causes V1A, V1B, V2A, V2B, V3A, and V3B to conduct less, and the voltage drop

across the regulators increases. The increased voltage drop across the regulators causes the regulated output voltage to decrease toward the original +250-volt level. The RC network composed of resistor R17 and capacitor C4 prevents any sudden fluctuation of voltage from appearing at the grids of the regulators. The regulator action reverses when the output voltage decreases.

(2) *Operation of regulator using +150-volt strapping* The regulator performs the same circuit functions for the +150-volt output as for the +250-volt output. A −220-volt input voltage from ±320v or +220v power supply is applied through connectors P1-3 and 5 to fuse F1 and the plates of the series regulator tubes. The +150-volt strapping bypasses resistor R1 in the fused +220-volt circuit to compensate for the reduced input voltage. The same −250-volt reference source is algebraically added to the regulator output in impedance network Z1. The 250 volts is now applied through resistors R22 and R23 to terminal 3 of impedance network Z1 instead of terminals 3 and 4. This compensates for the lower regulation voltage by placing an additional resistance in the −250-volt path. The

junction between plate load resistors R9 and R11 of V4 is removed from ground and maintained at a +150-volt level. The junction between screen dropping resistors R18 and R19 is now placed at ground potential. These two circuit changes are necessary so that the bias voltage on the grids of V1A, V1B, V2A, V2B, V3A, and V3B is the same for the +150-volt regulation. Regulators V1A, V1B, V2A, V2B, V3A, and V3B present the same 70-volt load to the input voltage resulting in +150 volts at connectors P1 8, 10, and 12.

(3) *Filament circuit.* The filaments of series regulators V1A, V1B, V2A, V2B, V3A, and V3B are heated by 6.3 volts at 17 amperes delivered from the parallel-connected secondary windings (terminals 3, 4 and 5, 6) of filament transformer T1. The filaments of V4A, V4B, and V5 are heated by 6.3 volts at 1.5 amperes delivered from the secondary winding (terminals 7-9) of filament transformer T1. Terminal 1 of the primary winding of T1 is connected to the 120-volt, 400-cps phase C voltage source through connector P1-14. Terminal 2 of the primary winding of T1 is connected to ac neutral through connector P1-15.

28 (U). −250, +250, or +150 Volt Regulator 7620552

a. General. The −250, +250, or +150 volt regulator is used with the ±320v or +220v power supply (par. 24) to provide the acquisition radar system with low impedance plate and bias supply voltages of +250, −250, +150, and +70 volts. Three optional methods of external connections (strapping) are used to obtain the desired output voltage.

b. Detailed Theory.

  (1) *Operation of regulator using −250-volt and +70-volt strapping (A-strapping).*

    (*a*) The output voltage of +320v volts from the ±320v or +220v power supply is applied between connectors P1–8 and 2 (fig. 34, TM 9–1430–257–20) to the plates of series regulators V4A, V4B, V5A, and V5B. The regulators and cathode resistors R13 through R16 are connected in series with the input voltage and the external load and present a constant 70-volt load to the input voltage. The regulating control circuit which is composed of input amplifier V1, reference tube V2, and driver V3 is connected in parallel with the external load. When the −250-volt and +70-volt strapping is used, the ground reference point (connector P1–6) is between the cathode circuit of V4A, V4B, V5A, and V5B and the plate circuit of V1, V2, and V3. This divides the +320-volt input into two potentials of +70 and −250 volts. The +70-volt potential is between connectors P1–8 and 4 and the −250-volt potential is between connectors P1–2 and 4.

    (*b*) The −250-volt regulation is obtained by controlling the current flow in V4A, V4B, V5A, and V5B with the grid bias voltage that is coupled from the plate of V3. Reference tube V2 provides a constant 108-volt drop within limits established by current-limiting cathode resistors R6 and R7 and the current-handling capacity of the tube. The voltage drop across V2 places −108 volts on the cathode of V1 with respect to ground. The voltage divider consisting of resistors R2, R3, and R23 establishes a dc level of 110 volts at the control grid of V1. This provides a grid bias of −2 volts. Bypass capacitors C2 and C3 prevent transients from appearing on the grid of V1 and the cathode circuits of V1, V2 and V3, respectively.

    (*c*) If the regulated −250-volt output increases, the control grid of V1 becomes more negative, causing the current flow through plate load resistor R4 to decrease and the plate potential to increase. The increase of potential at the plate of V1 is coupled to the grid of driver V3 by the RC network composed of resistor R5 and capacitor C4 and causes grid potential to rise with respect to cathode potential. The quiescent grid potential of −2 volts is determined by the voltage divider consisting of resistors R5, R10, and R11, and the cathode potential is determined by the current flow through resistor R8. The increase of grid potential causes V3 to conduct more heavily, resulting in an increase in current flow through plate load resistor R12. This causes a decrease in plate potential at the plate of V3 which is coupled by resistors R17, R18, R19, and R20 to the grids of V4A, V4B, V5A, and V5B, causing the series regulators to conduct less. This results in an increase of plate potential which returns the output voltage to the −250-volt level. In effect, the static resistance of V4A, V4B, V5A, and V5B has increased to counteract the increase in output voltage. An opposite reaction occurs when the output voltage decreases. Capacitor C1 couples to ground any ac components in the output voltage. The RC networks composed of resistor R21, capacitor C6, and resistor R9, capacitor C5 in the plate circuits of V3 and V2, respectively, prevent any

sudden change in the output voltage from appearing on the grids of V4A, V4B, V5A, and V5B and the cathode of V3.

(2) *Operation of regulator using +150-volt strapping (B-strapping)*. The operation for the +150-volt strapping of the regulator is the same as explained for the —250-volt and +70-volt strapping with the exception that the ground reference point has been changed from connectors P1–4 and 6 to connectors P1–2 and 3. The lower input voltage of +220 volts received at P1 8 and 10 from the +320v or +220v power supply is compensated for by the 150-volt strapping connections which short out resistors R3, R7, and R11. Shorting these resistors adjusts the bias requirements of V1 and V3 for the application of lower voltage to the plates. Reference V2 establishes a potential of approximately +42 volts on the cathodes of V1 and V3. The voltage divider consisting of R23 and R2 maintains the control grid of V1 at a potential of +40 volts. Thus, the grid of V1 is still 2 volts negative with respect to the cathode, as it was with the +250-volt and +70-volt strapping. Since the bias of V1 is the same, the same controlling current is conducted through V1 and V3 to the control grids of V4A, V4B, V5A, and V5B. Regulators V4A, V4B, V5A, and V5B and cathode resistors R13 through R16 form a regulated voltage divider maintaining a constant 70-volt drop. This 70-volt drop establishes the +150-volt output potential between P1–4 and 6 and ground. The regulation of the +150 volts is the same as ex-plained for the -250-volt and +70-volt operation.

(3) *Operation of regulator using +250-volt strapping (C-strapping)*. Operation for the +250-volt strapping of the regulator is the same as for the +150-volt strapping of the regulator with the exception that resistors R3, R7, and R11 are now in the circuit to maintain the bias requirements of V1 and V3 for the higher input voltage of +320 volts. The +320 volts is received from the ±320v or +220v power supply at P1–8 and 10. The output voltage of +250 volts is taken from P1–4 and 6.

(4) *Filament circuit*. The filaments of the —250, +250, or +150 volt regulator are heated by 6.3 volts at 6 amperes delivered from the parallel connected secondary windings (3, 4 and 5, 7) of filament transformer T1. Terminal 2 of the primary winding of T1 is connected to the 120-volt, 400-cps phase C voltage source through P1–14. Terminal 1 of the primary winding of T1 is connected to ac neutral through P1–15.

29 (U). Acquisition HV Power Supply 9138109

a. General. The acquisition HV power supply furnished 4000 to 8000 volts at 1 ampere to the acquisition modulator. The amplitude of this voltage is controlled magnetically through an included saturable reactor.

b. Detailed Theory.

(1) A 120-volt, 3-phase, 400-cps voltage is applied through the series coils of saturable reactor L1 (fig. 44, TM 9–1430–257–20) to delta-wye-connected transformer T1. A variable transformer in the ex-

ternal acquisition control-indicator sets the input voltage level to transformer T3, which in turn controls the level of the dc voltage applied from full-wave crystal bridge rectifier CR1 to winding 7 8 of saturable reactor L1. The dc voltage across winding 7–8 saturates the cores of the other three windings of L1. The greater the dc current flow through winding 7–8, the more saturated the cores become and the lower the effective inductance of the other windings. This lowers the inductance and the voltage that is dropped across the windings. As a higher voltage is applied to T1, a higher dc voltage is available from the power supply.

(2) The 3-phase voltage is stepped up by transformer T1 and rectified by the action of 3-phase full-wave rectifiers V1 through V6. The plates of rectifiers V1, V2, and V3 are connected to the respective windings of the secondary of T1 (wye portion) and to the filaments of counterpart rectifiers V4, V5, and V6. The filaments of V1 through V6 are energized from the secondary of transformer T2. One secondary winding is used for the filaments of V1, V2, and V3, since the high voltage is taken from this point. Separate windings are required for the filaments of V4, V5, and V6, since the filaments of these tubes are at a different potential with respect to ground. If the induced secondary voltage is positive at terminal 4 of T1 (with respect to terminal 5), electron current flows from terminal 5 of T1 through V4, overcurrent relay K1, resistors R4, R3, R2, R1, the power supply filter, and V2 to terminal 4 of T1. This conduction path shunts the load, and its admittance during no-load conditions is very low. With a load applied, the electron current path is from ground through the load to the junction of resistor R1 and capacitor C1B, then through inductor L2 to the filaments of V1, V2, and V3. It is only during this load condition that

the 1-ampere current potentialities of the power supply are utilized.

(3) The positive high-voltage output of the power supply appears between the filaments of V1, V2, and V3, and ground. Because of the high ripple frequency (2,400 cps) between these two points, very little filtering is necessary, and a small filter can be used. Inductor L2 and capacitors C1A and C1B form a choke-input filter for the rectifiers. Resistors R1, R2, and R3 form a voltage divider to provide a voltage, proportional to the output voltage, for front-panel metering. These resistors also serve as a bleeder network for the power supply to discharge the filter capacitors when the input power is removed. Overcurrent relay K1 provides overload protection for the power supply by opening an interlock circuit when excessive current is drawn. To protect personnel from high voltages, ~~a~~ shorting switch S1 grounds the filter capacitors when the cabinet door is opened. Protector blocks TY1 and TY2 are safety devices which minimize the effect of sudden voltage changes by a compensating change in the resistance of the protector block. Resistor R4 shunts the external current reading meter.

interlock switch S1 opens an interlock circuit and

(4) Each tube conducts for 120° and remains cut off for 240° of the applied voltage. However, one tube is cutting on and one tube is cutting off every 60° This results in a ripple frequency of 2,400 cps which is six times the supply frequency. This provides ease in filtering the 4,000- to 8,000-volt output. Table III shows the tubes that conduct various times throughout the cycle.

(5) Figure 16 is a simplified schematic of the acquisition HV power supply. Figure 17 shows the ac voltages that are applied from the secondary of T1 to the rectifier tubes. Assume that the ac voltages are just passing through time t_1 (0°) toward t_2 (60°). Phase A, connected to the plate of V3, is more positive

Table III. Tubes Conducting During Different Intervals of Time

Interval of time	Tube conduction
Between t₁ (0°) and t₂ (60°)	V4 and V3
Between t₂ (60°) and t₃ (120°)	V4 and V2
Between t₃ (120°) and t₄ (180°)	V6 and V2
Between t₄ (180°) and t₅ (240°)	V6 and V1
Between t₅ (240°) and t₆ (300°)	V5 and V1
Between t₆ (300°) and t₇ (360°)	V5 and V3

than phase B or C; and V3 conducts carrying current through the load, provided either V4, V5, or V6 conducts. Phase C, connected to the cathode of V4, is more negative than the other two phases. Thus, V4 conducts and current flows through V4, the load, V3, T1 terminals 6 to 5, and back to V4. Tubes V3 and V4 continue to conduct until t₂ is reached, at which time phase B becomes more positive than phase A. Thus, V3 cuts off and V2, the plate of which is connected to phase B, conducts. Tube V4 continues to conduct because phase C is still more negative than phase A or B. Tube V4 continues to conduct until t₃ is reached, at which time phase A

becomes more negative than phase C. Tube V4 cuts off and V6, the cathode of which is connected to phase A, conducts. Since phase B is still more positive than the other two phases, V2 continues to conduct. Thus, from time t₃ to time t₄, V6 and V2 conduct. At time t₄, phase C becomes more positive than phase B. At this time V2 cuts off and V1, the plate of which is connected to phase C, cuts on. Since phase A is still more negative than the other two phases, V6 continues to conduct. Thus, from time t₄ to time t₅, V6 and V1 conduct. At t₅, phase B becomes more negative than phase A; at this time V6 cuts off and V5, the cathode of which is connected to phase B, conducts. Phase C is still more positive than the other two phases; therefore, V1 continues to conduct. Thus, V5 and V1 conduct from time t₅ to time t₆. At time t₆, phase A comes more positive than phase C, V3 cuts on, and V1 cuts off. Tube V5 continues to conduct. Thus, V5 and V3 conduct from time t₆ to time t₇. At t₇, phase C becomes more negative than phase B, V5 cuts off, and V4 conducts. Tube V3
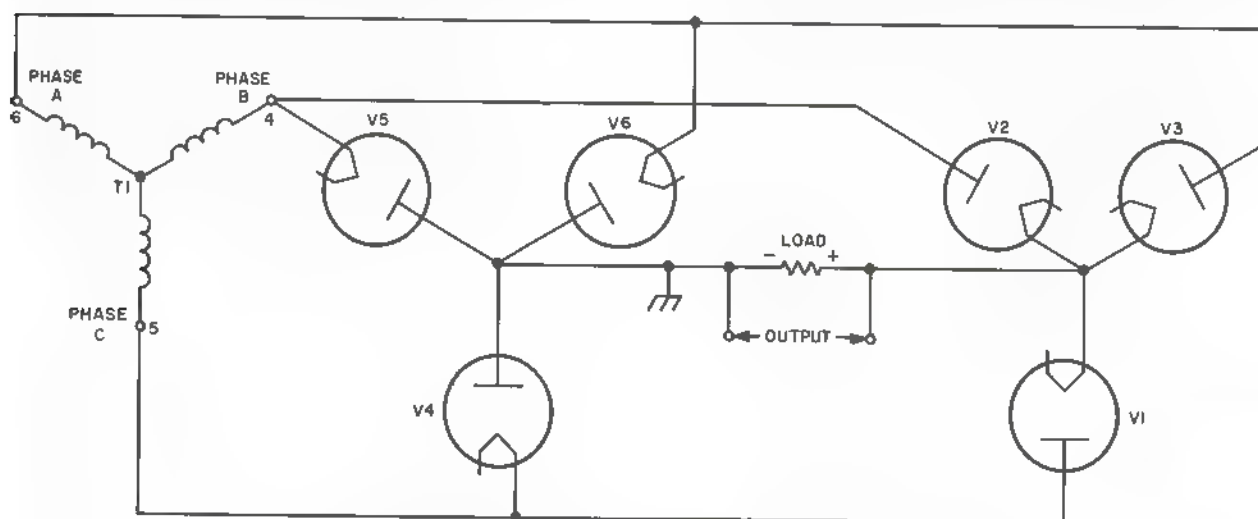
RA PD 467995

Figure 16 (U) Acquisition HV power supply—simplified schematic diagram
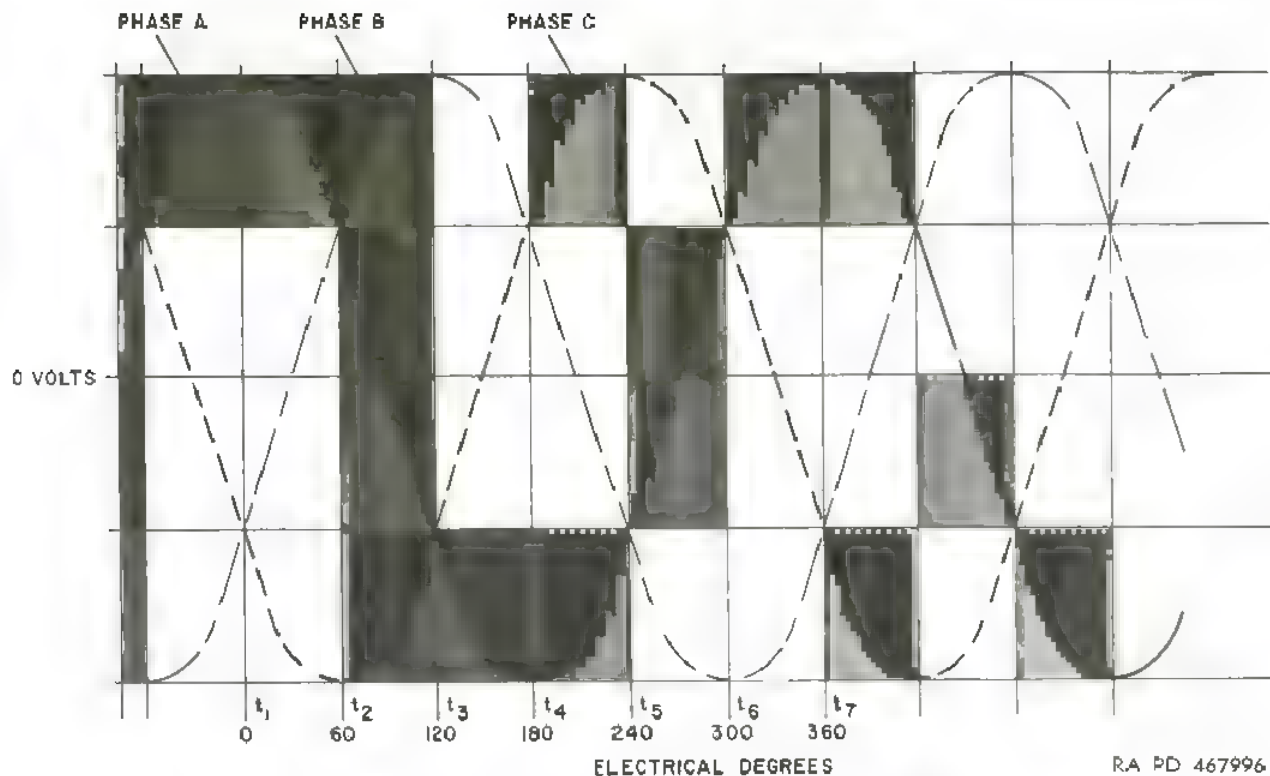
Figure 17. (U) Voltage applied from T1 secondary to rectifiers.

continues to conduct and the cycle of events is repeated.

30. Acquisition Power Control Panel 8513518

a. General. The acquisition power control panel distributes primary power to the acquisition radar system. The unit provides protective fusing of the primary power circuits and metering of acquisition power supply voltages.

b. Detailed Theory.

(1) *MAIN POWER switch S4.* With MAIN POWER switch S4 (fig. 27, TM 9-1430-257-20) placed in the ON position, 120-volt, 3-phase, 400-cps primary power is distributed through the acquisition power control panel to the trailer mounted tracking station, computer power supply group, and various circuits of the acquisition radar system.

(2) *EQPT VENT switch S7.* With S4 in the ON position and EQPT VENT switch S7 placed in the ON position, operating voltage is applied to the centrifugal fan in the acquisition power supply cabinet to provide ventilation and cooling. EQPT VENT switch S7 is mounted behind the acquisition power control panel and is normally left in the ON position.

(3) *ACQUISITION POWER switch S6.* With ACQUISITION POWER switch S6 placed in the ON position, primary power is distributed to the filament circuits, dc power supplies, and control circuits of the acquisition radar system.

(4) *ACQ MOTORS switch S5.* With S6 in the ON position and ACQ MOTORS switch S5 placed in the ON position, primary power is distributed to the acquisition antenna drive motors and antenna blowers. ACQ MOTORS switch S5 is mounted behind the acquisition power control panel and is normally left in the ON position.

(5) PLATE VOLTS switch S9. PLATE VOLTS—READY indicator light I31 illuminates approximately 20 seconds after S6 is placed in the ON position to indicate that plate voltage may be applied to the acquisition radar power supplies. The 20-second delay is furnished by the 20-30-second delay timer located in the acquisition power supply group. Acquisition power supply plate voltage is delayed to allow the filaments of the thyratron rectifiers to heat before plate voltage is applied. When PLATE VOLTS switch S9 is placed in the ON position I31 is extinguished and PLATE VOLTS—ON indicator light I32 is illuminated. Plate volts on relays K1 and K2 are energized with S9 in the ON position, and primary power is applied through contacts of K1 to the acquisition power supplies. Capacitor C2 and resistor R3 suppress transients developed in the relay circuit. The 15-minute delay timer in the acquisition power supply group applies operating ground to high-voltage on relays K3 and K4 15 minutes after S6 is placed in the ON position. Capacitor C1 and resistor R2 suppress transients developed in the relay circuit. HIGH VOLTS—READY indicator light I35 illuminates when the acquisition HV power supply is ready to be energized. The delay furnished by the 15-minute delay timer provides sufficient time for the acquisition magnetron filament to heat before application of high voltage. With K3 and K4 energized, I35 is extinguished and HIGH VOLTS—ON indicator light I36 is il-

luminated. Primary power for the acquisition HV power supply is applied through contacts of energized K3. The noise generator is disabled when K4 is energized. The +1550-volt relay K5 is also energized at the termination of the 15-minute delay period to apply primary power to the acquisition PPI HV power supply. Varistor CR1A protects K5 from overvoltage and contact arcing. High VOLTS — PREHEAT indicator light I33 illuminates when primary power is applied to the acquisition radar system filament circuits, and HIGH VOLTS—HOT indicator light I34 illuminates when the acquisition radar system filaments become sufficiently heated for safe operation.

(6) INTLK OVERRIDE switch S10. INTLK indicator light I30 illuminates to indicate the interlock switches are operating. Interlock switches on equipment located in the trailer mounted director station and the battery control console can be bypassed by holding INTLK OVERRIDE switch S10 in the ON position. With S10 in the ON position, I30 remains illuminated. Operation of S10 does not affect the delay timing circuits in the acquisition power supply group.

(7) BATTLE SHORT switch S1. Operation of BATTLE SHORT switch S1 enenergizes battle short relay K6. With K6 energized, all interlock and delay timing circuits are bypassed to permit immediate application of acquisition power supply low voltages. Varistor CR1B protects K6 from overvoltage

(8) *TRACK TRANSMITTER FILA-MENTS switch S2.* Operation of TRACK TRANSMITTER FILA-MENTS switch S2 provides −28 volts dc to the track radars to activate the filament circuits. TRACK TRANS-MITTER FILAMENT indicator light I29 illuminates when S2 is placed in the ON position.

(9) *PHASE switch S8.* PHASE switch S8 selects the phase of the acquisition power control panel line voltage to be monitored on LINE VOLTS meter M2. ADJUST PHASE C knob (resistor R1) is adjusted to provide the desired voltage for phase C circuits. Application of voltage to ADJUST PHASE C variable resistor R1 is controlled by VOLTS ADJ switch S11. Switch S11 is mounted behind the acquisition power control panel and is normally locked in the IN position.

(10) *VOLTS CHECK switch S3.* VOLTS CHECK switch S3 selects the acquisition power supply voltage output to be monitored by VOLTS CHECK meter M1. Resistors R4 through R24 form the meter range multiplier network and provide suitable meter ranges for voltage indications.

(11) *Blown fuse indicators.* All fuses mounted on the acquisition power control panel have a blown fuse indicator light to facilitate fuse replacement and to aid in locating defective circuits

30.1 (U). Acquisition Power Control Panel 9144931

a General. The acquisition power control panel distributes primary power to the acquisition radar system. The unit provides protective fusing of the primary power circuits and metering of acquisition power supply voltages.

b. Detailed Theory. Acquisition power control panel 9144931 (fig. 88, TM 9-1430 257-20/1) is the same as acquisition power control panel 8513518, discussed in paragraph 30, except for the following modifications:

(1) ACQUISITION POWER switch S6 is replaced by PRESENTATION POWER switch S5.

(2) ACQ MOTORS switch S5 is replaced by BARBETT AC POWER switch S6. With PRESENTATION POWER switch S5 in the ON position and BARBETT AC POWER switch S6 in the ON position, primary power is distributed to the LOPAR antenna-receiver-transmitter group. To supply dc to the acquisition antenna-receiver-transmitter group, it is necessary to operate BARBETT DC switch S12 to the ON position. This switch energizes associated relays in the LOPAR relay assembly, which pass the dc voltage.

31 (U). Trigger Pulse Amplifier 9136410

a. General. The trigger pulse amplifier has two functions. One function provides a trigger pulse for the IFF transponder The second function provides interference suppression for received signals.

b. Detailed Theory.

(1) *Trigger pulse circuit.*

(a) The trigger pulse circuit (fig. 44.1, TM 9-1430 257-20) is made up of electron tube V6 and associated circuits. During quiescence, −23 volts is developed across resistor R47 of the voltage divider consisting of resistors R47, R46, and R53 between ground and −250 volts. This bias voltage keeps the input side of pulser V6 cut off. A second bias voltage of −23 volts is developed across resistor R51 of the voltage divider consisting of resistors R51, R52, and R53 between ground and −250 volts. This bias voltage keeps the output side of V6 cut off During pulse time, a preknock pulse of 1-microsecond duration and 20- to 40-volt amplitude is coupled through connector J8 and capacitor C19 to the grid on the input side of V6. The amplitude of the pulse overcomes the bias, causing the input side to conduct.

(b) When the input side of V6 conducts, plate current is drawn through winding 2–1 of pulse transformer T1. In turn, a voltage is induced in winding 4–3 having

a positive polarity at terminal 3. This voltage is applied to the control grid on the output side of V6 and drives the output side into conduction. This causes more current to flow in winding 2-1 of T1 and produces a higher positive voltage at terminal 3. The grid goes more positive, and more plate current flows. This action continues at a rapid rate until grid current flows and saturation is reached. The grid current changes capacitor C20 to a value more positive than before. At saturation, the current through winding 2-1 becomes constant and no voltage is induced at terminal 3 of T1. Since no positive voltage is coupled to the grid except the change in capacitor C20, the bias quickly asserts itself, driving the grid toward cutoff. Plate current decreases and the magnetic field in T1 begins to collapse. This induces a negative potential at terminal 3 which aids the fixed bias in driving the grid more negative. The plate current continues to decrease, inducing an even more negative potential at terminal 3 and the grid. This action continues until the tube is cut off. The fixed bias then holds the tube cut off until the next input pulse. Capacitor C17 and resistor R50 and capacitor C16 and R53 are decoupling networks to keep the trigger pulse out of the +250-volt and −250-volt power supplies. Capacitor C15 and resistor R45 make up a decoupling network to keep signals out of the +150-volt power supplies.

(c) The circuit constants of the trigger pulse circuit are chosen so that tube current through cathode resistors R48 and R49 produces an output pulse identical to the preknock pulse if output connector J9 is terminated with a 75-ohm load. This pulse is coincident with, but electrically isolated from, the preknock pulse.

(2) *Interference suppression circuits.*

(a) When interference suppressor relay K1 is not energized, bypass video enters the assembly at connector J3, passes through contacts 10-3 and 1-9 of relay K1, and leaves the assembly at connector J4. MTI video enters at J5, passes through contacts 12-8 and 6-11 of K1, and leaves the assembly at connector J6.

(b) When INT SPR switch S20 on the acquisition control-indicator is operated, relay K1 on the trigger pulse amplifier operates. When K1 operates, the bypass video from J3 passes through contacts 10-4 of relay K1 and is terminated in resistor R37. Interference suppressor (IS) video from the trigger pulse amplifier passes through contacts 2-9 of K1 and leaves the assembly at J4. Thus IS video is substituted for bypass video in the presentation system. MTI video from J5 is applied through contacts 12-7 of K1 to a coincidence circuit, and the MTI video which is in coincidence with the IS video is passed through the assembly at J6. This video replaces the MTI video in the presentation systems. The outputs of the trigger pulse amplifier which replace the bypass video and MTI video will hereafter be identified as IS (interference suppres-

sor) video and MTI-IS video, respectively.

(c) The IS circuit is a coincidence circuit which compares the content of the delay and non-delay video channels and rejects any information which is not in both channels. Any interference which occurs during one pulse repetition period but not in the next is rejected.

(d) Composite non-delay video, consisting of a positive preknock pulse followed by a negative test pulse and negative video, is applied at connector J2, coupled through capacitor C2, developed across resistor R5, and impressed on the grid of video amplifier V2B. The positive preknock pulse is shunted to ground by diode CR2. The negative test pulse and negative video are amplified and inverted by V2B, developed across plate resistor R6, and coupled through capacitor C5 to the control grid of coincidence amplifier V3 as positive pulses, developed across resistor R24. Bias for the control grid of V3 is developed across the voltage divider made up of resistor R20, variable resistor R18, and resistor R15 between ground and -250 volts.

(e) Composite delay video, consisting of a negative preknock pulse followed by a positive test pulse and positive video, is applied at connector J1, coupled through capacitor C1, developed across resistor R1, and impressed on the grid of video amplifier V1A. The negative preknock pulse is

shunted to ground by diode CR1. The positive test pulse and positive video are amplified and inverted by V1A, coupled through capacitor C4, developed across resistor R11, and impressed on the grid of video amplifier V2A. The signal is amplified and inverted by V2A, coupled through capacitor C7, developed across resistor R23, and impressed on the suppressor grid of coincidence amplifier V3 as a positive test pulse and positive video. Bias for the suppressor grid is developed across the voltage divider made up of variable resistor R16 and resistor R14 between ground and -250 volts. Resistor R26 is the screen dropping resistor, and capacitor C12 is the screen bypass.

(f) If the signals on the control grid and suppressor grid of V3 are positive and coincident, V3 produces a negative output. If the signals are not positive and coincident, V3 remains cut off. The negative output pulses from V3 are coupled through capacitor C8, developed across resistor R30, and applied to the grid of paraphase amplifier V1B through parasitic suppressor resistor R44. Amplifier V1B is biased on by +16.5 volts developed across the voltage divider consisting of resistors R32 and R31 between ground and +150 volts. Diode CR4 clamps the grid of V1B to a potential not greater than +16.5 volts. Negative signals on the grid of V1B produce positive sig-

nals at the plate and negative signals at the cathode. The positive signals from the plate are coupled through capacitor C10, developed across resistor R22, and applied to the suppressor grid of coincidence amplifier V5. Negative signals at the cathode of V1B are coupled through capacitor C18, developed across resistor R35, and applied to connector J4 through contacts 2-9 of relay K1. The IS video output at J4 is used to drive the bypass video circuits in the presentation system. A second negative output is taken from the junction of V1B cathode resistors R36 and R34 and coupled through capacitor C14 to the BY-PASS side of MTI - BYPASS switch S1. When S1 is operated to BYPASS the IS video is applied to test connector J7.

(g) The MTI - IS coincidence circuit uses MTI video and IS video to produce an output free of random interference and stationary object video. MTI video from connector J5 passes through contact 12-7 of relay K1 and is developed across resistor R8. Diode CR3 shunts any positive video to ground, and the negative video is applied to the grid of video amplifier V4A. The signal is amplified and inverted by V4A, coupled through capacitor C6, developed across resistor R21, and applied to the control grid of coincidence amplifier V5 as positive video. Bias for the

control grid is developed across the voltage divider consisting of resistor R20, variable resistor R19, and resistor R15 between ground and -250 volts. Bias for the suppressor grid is developed across the voltage divider consisting of variable resistor R17 and resistor R14 between ground and -250 volts. Resistor R29 and capacitor C13 are the screen dropping resistor and screen bypass, respectively.

(h) If the MTI video pulses at the control grid and IS video pulses at the suppressor grid of V5 are positive and coincident, V5 produces negative signals which are coupled through capacitor C9, developed across resistor R38, and coupled through parasitic suppressor resistor R40 to the grid of video amplifier V4B. V4B is biased on by +10 volts developed across the voltage divider consisting of resistors R43 and R39 between ground and +150 volts. Diode CR5 clamps the grid of V4B to a potential not greater than +10 volts. Negative signals on the grid of V4B produce negative signals at the cathode. These signals are coupled through capacitor C11, developed across resistor R42, and applied to the MTI side of MTI - BYPASS switch S1 and through contacts 5-11 of relay K1 to connector J6. The negative MTI - IS video at J6 replaces the MTI video in the presentation system.

31.1 (U). Interference Suppressor Pulse Amplifier-Generator 9160170

a. General. The interference suppressor pulse amplifier-generator has two functions. One function provides a trigger pulse for the IFF transponder. The second function provides interference suppression for received signals.

b. Detailed Theory.

(1) *Trigger pulse circuit.*

(a) The trigger pulse circuit (fig. 44.1, TM 9-1430-257-20/1) is made up of pulser V6 and associated circuits. During quiescence, —23 volts is developed across resistor R47 of the voltage divider consisting of resistors R47, R46, and R53 between ground and —250 volts. This bias voltage keeps the input side of pulser V6 cut off. A second bias voltage of -23 volts is developed across resistor R51 of the voltage divider consisting of resistors R51, R52, and R53 between ground and 250 volts. This bias voltage keeps the output side of V6 cut off. During pulse time, a preknock pulse of 1-microsecond duration and 20 to 40-volt amplitude is coupled through connector J8 and capacitor C19 to the grid on the input side of V6. The amplitude of the pulse overcomes the bias, causing the input side to conduct.

(b) When the input side of V6 conducts, plate current is drawn through winding 2–1 of pulse transformer T1. In turn, a voltage is induced in winding 4–3 having a positive polarity at terminal 3. This voltage is applied to the control grid on the output side of V6 and drives the output side into conduction. This causes more current to flow in winding 2-1 of T1 and produces a higher positive voltage at terminal 3. The grid goes more positive and more plate current flows. This action continues at a rapid rate until grid current flows and saturation is reached. The grid current changes capacitor C20 to a value more positive than before. At

saturation, the current through winding 2-1 becomes constant and no voltage is induced at terminal 3 of T1. Since no positive voltage is coupled to the grid except the change in capacitor C20, the bias quickly asserts itself, driving the grid toward cutoff. Plate current decreases and the magnetic field in T1 begins to collapse. This induces a negative potential at terminal 3 which aids the fixed bias in driving the grid more negative. The plate current continues to decrease, inducing an even more negative potential at terminal 3 and the grid. This action continues until the tube is cut off. The fixed bias then holds the tube cut off until the next input pulse. Capacitor C17 and resistor R50 and capacitor C16 and R53 are decoupling networks to keep the trigger pulse out of the +250-volt and 250-volt power supplies. Capacitor C15 and resistor R45 make up a decoupling network to keep signals out of the +150-volt power supply.

(c) The circuit constants of the trigger pulse circuit are chosen so that tube current through cathode resistors R48 and R49 produces an output pulse identical to the preknock pulse if output connector J9 is terminated with a 75 ohm load. This pulse is coincident with, but electrically isolated from, the preknock pulse.

(2) *Interference suppression circuits.*

(a) When interference suppression relays K1 and K2 are not energized, bypass video enters the assembly at connector J3, passes through contacts 10-3 and 1-9 of relay K1, and leaves the assembly at connector J4. MTI video enters at J5, passes through contacts 2-4 and 6-8 of K2, and leaves the assembly at connector J6.

(b) When INTFER SUPPR switch on the LOPAR control-indicator is operated, relays K1 and K2 on

the interference suppressor pulse amplifier-generator operate. When K1 and K2 operate, the bypass video from J3 passes through contacts 10 4 of relay K1 and is terminated in resistor R37. Interference suppressor (IS) video from the trigger pulse amplifier passes through contacts 2–9 of K1 and leaves the assembly at J4. Thus IS video is substituted for bypass video in the presentation system. MTI video from J5 is applied through contacts 2–5 of K2 to a coincidence circuit, and the MTI video, which is in coincidence with the IS video, is passed through contacts 1–6 of K2 and leaves the assembly at J6. This video replaces the MTI video in the presentation system. The outputs of the interference suppressor pulse amplifier-generator which replace the bypass video and MTI video will hereafter be identified as IS (interference suppressor) video and MTI-IS video, respectively.

(c) The IS circuit is a coincidence circuit which compares the content of the delay and nondelay video channels and rejects any information which is not in both channels. Any interference which occurs during one pulse repetition period but not in the next is rejected.

(d) Composite nondelay video, consisting of a positive preknock pulse followed by a negative test pulse and negative video, is applied at connector J2, coupled through capacitor C2, developed across resistor R5, and impressed on the grid of video amplifier V2B. The positive preknock pulse is shunted to ground by diode CR2. The negative test pulse and negative video are amplified and inverted by V2B, developed across plate resistor R6, and coupled through capacitor C5 to the control grid of coincidence amplifier V3 as positive pulses developed across resistor R24. Diode CR7 clamps the grid of V3 to a potential not greater than zero volts. This

clamping insures that all video signals start from the same reference level.

(e) Composite delay video, consisting of a negative preknock pulse followed by a positive test pulse and positive video, is applied at connector J1, coupled across capacitor C1, developed across resistor R1, and impressed on the grid of video amplifier V1A. The negative preknock pulse is shunted to ground by diode CR1. The positive test pulse and positive video are amplified and inverted by V1A, coupled through capacitor C4, developed across resistor R11, and impressed on the grid of video amplifier V2A. The signal is amplified and inverted by V2A, coupled through capacitor C7, developed across resistor R23, and impressed on the suppressor grid of coincidence amplifier V3 as a positive test pulse and positive video. Diode CR8 clamps the suppressor grid of V3 to a potential not greater than 0 volts. Bias for the suppressor grid is developed across the voltage divider made up of delay video suppression variable resistor R16 and resistor R14 between ground and −250 volts. Resistor R26 is the screen dropping resistor, and capacitor C12 is the screen bypass.

(f) If the signals on the control grid and suppressor grid of V3 are positive and coincident, V3 produces a negative output. If the signals are not positive and coincident, V3 remains cut off. The negative output pulses from V3 are coupled across capacitor C8, developed across resistor R30, and applied to the grid of paraphase amplifier V1B through parasitic suppressor resistor R44. Amplifier V1B is biased by +16.7 volts developed across the voltage divider consisting of resistors R32 and R31 between ground and +150 volts. Diode CR4 clamps the grid of V1B to a potential not greater than +16 7 volts. Negative signals on the grid of V1B produce positive signals

at the plate and negative signals at the cathode. The positive signals from the plate are coupled through capacitor C10, developed across resistor R22, and applied to the suppressor grid of coincidence amplifier V5. Negative signals at the cathode of V1B are coupled through capacitor C18, developed across resistor R35, and applied to connector J4 through contacts 2–9 of relay K1. The IS video output at J4 is used to drive the bypass video circuits in the presentation system. A second negative output is taken from the junction of V1B cathode resistors R36 and R34 and coupled through capacitor C14 to the BYPASS side of MTI-BYPASS switch S1. When S1 is operated to BY-PAS, the IS video is applied to test connector J7.

(g) The MTI-IS coincidence circuit uses MTI video and IS video to produce an output free of random interference and stationary object video. MTI video from connector J5 passes through contacts 2–5 of relay K2 and is developed across resistor R8. The signal is amplified and inverted by V4A, coupled through capacitor C6, developed across resistor R21, and applied to the control grid of coincidence amplifier V5 as positive video. Bias for the control grid is developed across the voltage divider consisting of resistor R20, MTI Video suppression variable resistor R19, and resistor R15 between ground and –250 volts. Bias for the suppressor grid is developed across the voltage divider consisting of bypass video suppression variable resistor R17 and resistor R14 between ground and –250 volts. Resistor R29 and capacitor C13 are the screen dropping resistor and screen bypass respectively.

(h) If the MTI video pulses at the control grid and the IS video pulses at the suppressor grid of V5 are positive and coincident, V5 produces negative signals which are coupled through capacitor C9, developed across resistor R38, and coupled across parasitic suppressor resistor R40 to the grid of video amplifier V4B. Diode CR5 clamps the grid of V4B to a potential not greater than 0 volts. Negative signals on the grid of V4B produce negative signals at the cathode. These signals are coupled through capacitor C11, developed across resistor R42, and applied to the MTI side of MTI-BYPASS switch S1 and through contacts 1–6 of relay K2 to connector J6. The negative MTI–IS video at J6 replaces the MTI video in the presentation system.

31.2 (U). LOPAR Relay Assembly 9143901

a. General. The LOPAR relay assembly contains four relays used to apply ac and dc power to the low-power acquisition system and a relay to switch the HIPAR pre-trigger or the MTI auto sync pulse into the acquisition-track synchronizer. This makes it possible to operate the HIPAR without energizing the LOPAR.

b. Detailed Theory.

(1) High voltage preheat relay K3 (fig. 89, TM 9 1430–257–20/1) is energized by –28 volts supplied at the end of the delay period by the 5-minute delay timer. Relay K3 applies generator excitation and –28 volts to the LOPAR circuits. It also applies –28 volts to relays K1 and K2.

(2) Barbette dc on relay K1 and barbette power on relay K2 are energized when BARBETT DC switch S12 on the acquisition power control panel is ON. These relays apply both dc and ac power to the LOPAR antenna-receiver-transmitter group.

(3) +320V overload relay K4 is also energized by BARBETT DC switch S12 if thermal overload relay K4 on

the 5-minute timer is closed. Relay K4 provides +320 volts to the precision indicator and 28 volts to high volts on relay K3 in the acquisition power control panel.

(4) High power select relay K5 is energized when the RADAR SELECT switch on the IFF control-indicator is operated to LOPAR. Relay K5 switches the input of the acquisition-track synchronizer from hipar pre-knock trigger pulses to MTI auto sync pulses. Termination resistor R75 and contacts 1, 6, and 8 of relay K5 form a termination circuit.

31.3 (U). Acquisition Interference Suppressor 9990600

a. General. Acquisition interference suppressor 9990600 is part of the antijam display. All system video signals pass through this unit except jam strobe. The video inputs to the acquisition interference suppressor are: bypass video, delay video, non-delay video, and MTI video. The video output may be processor, interference suppressor, or normal video, depending on the mode selected, and will appear as processor feedback, bypass video, processor video, or MTI video. In the normal mode of operation the bypass video and the MTI video are passed through the unit without alteration while the delay and non-delay videos are not used.

b. Detailed Theory.

(1) MTI video is applied through MTI IN connector J5 (fig. 44.2, TM 9-1430-257-20), coupled through capacitor C27, developed across resistor R61, and applied to the base of emitter follower Q3. Diode CR33 clips the positive portions of the MTI video. Emitter followers Q1 through Q3 make up a transistor driven AND gate having high input impedance to minimize loading of the input sources. When operating in the normal mode, relay K1 is deenergized and —3 volts is developed at the junction of R67 and R68 in the voltage divider network made up of resistors R67 through R70 connected between —250 volts and ground. The —3 volts is applied

through contacts 5 and 11 of K1 and resistors R62 and R63 to transistors Q2 and Q1, respectively, fixing their base voltage and permitting MTI video to transfer through the AND gate. The MTI video signal is developed across emitter resistor R64 and is coupled through diode CR27, developed across resistor R50, and applied to the grid of cathode follower V1B. Diodes CR25, CR26, and CR27 isolate the three transistor stages and are part of the AND gate circuit. The output signal which is developed across resistor R56 is applied directly to the grid of cathode follower V4B. Diode CR29 prevents damage to V4B if tube V1 is removed with power on. The output of cathode follower V4B is developed across resistor R57, coupled through capacitor C25, and applied across resistor R58 to MTI OUT connector J6.

(2) When K1 is energized, the —3-volt bias is removed from the base of emitter followers Q1 and Q2 and the MTI video signal output at connector J6 is dependent on the coincidence of delay, non-delay, and MTI video signals at the AND gate. The output of the AND gate is the smallest of three inputs, and since the delay and non-delay video signals are always larger than the MTI video, they act as gates for the MTI video. The amplitude of the output signal is determined by the amplitude of the MTI input signal. When the video signals are not coincidental, there is no output from the AND gate and extraneous noise and jamming signals are blocked.

(3) Bypass video is applied through BYPASS IN connector J3. During the normal mode of operation the bypass video is coupled through contacts 10 and 3 of K1 and through contacts 1 and 9 of K1 directly to BYPASS/ PROC VID connector J4. During the interference suppressor mode of operation, bypass video is terminated through contacts 10 and 4 of energized K1 and resistor R1 to ground.

(4) During the interference suppressor mode of operation a signal on the BY-PASS PROC VID connector J4 is dependent on the time coincidence of the delay and non-delay video input signals. This random signal suppression reduces the effectiveness of random noise and side lobe jamming as well as railing, walking pulses, and friendly interference signals.

(5) Non-delay video is applied through NON DELAY VID IN connector J2, through secondary winding 5-6 of transformer T1, coupled through capacitor C18, developed across resistor R43, and applied to the control grid of amplifier V7. Diode CR21 clips positive portions of the non-delay video. The non-delay video signal is amplified and inverted in V7, developed across plate load resistor R44, and coupled directly to grid 7 of bypass amplifier V6 and control grid 7 of multiplier V3.

(6) Delay video, which is delayed for 1 pulse repetition period from the non-delay video, is applied through DE-LAY VID IN connector J1, coupled through capacitor C1, developed across resistor R2, and applied to the grid of amplifier V1A, where it is amplified and inverted. Degenerative feedback to stabilize the amplifier gain is obtained through unbypassed cathode resistor R4. The output of V1A is developed across plate load resistor R3, coupled through secondary winding 3-4 of T1, coupled through capacitor C2, developed across resistor R5, and applied to the control grid of amplifier V2. Diode CR2 clips any positive portions of the video signal. The signal is amplified and inverted by V2, developed across plate load resistor R6 and coupled directly to grid 3 of V6 and to control grid 1 of V3.

(7) The suppression of random signals and the amplification of sweep-to-sweep coincident signals is accomplished by the application of the delay and non-delay video signals to the two control grids of V3, which is a dual control pentode. The interdependent control characteristics of the two grids of this tube permit biasing to points where the stage acts as an effective coincidence circuit. The amplitude of the signal present at control grid 1 may be considered as a controlling voltage that determines the multiplying constant for the signal present on grid 7. The output of V3 is developed across plate load resistor R12, coupled through capacitor C8, developed across resistor R15 and coupled through grid current limiting resistor R14 to the grid of amplifier cathode follower V4A. Since the gain of V6 is almost negligible with K2 deenergized, it contributes almost nothing to the input of amplifier cathode follower V4A. Resistor R13 is the screen grid dropping resistor for V3 and C7 is the screen grid bypass capacitor. Diode CR6 shunts positive portions of the input signal for V4A to ground. The operating level of the grid of V4A is set by the +120 volts developed across diode CR7, in the CR7-resistor R16 voltage divider and regulator circuit connected between +150 volts and ground.

(8) Output amplifier cathode follower stage V4A has two outputs. One output is developed across resistor R19 and coupled through capacitor C10 and contacts 2-9 of energized K1 to BYPASS PROC VID connector J4. Resistor R18 is an unbypassed cathode resistor which with R19 forms a voltage divider for obtaining the proper level output signal from the cathode. Another output signal from V4A is developed across plate resistor R17, coupled through capacitor C9, and applied to PROC FB connector J7.

(9) TEST switch S1 selects either MTI video or processor video to be applied through capacitor C17 to TEST OUT connector J8 for monitoring purposes.

(10) When relay K2 is energized, relay K1 becomes deenergized because ground connection is broken through contacts 7 and 12 of K2. The cathode circuits

of V6 are changed by the application of +150-volts through contacts 2-9 and 4-10, respectively, of K2 to terminal 1 of PROC ADJ 2 variable resistor R35 and terminal of PROC ADJ 1 variable resistor R37. This action causes the operating voltage on the cathodes of V6 to shift so that the gain of each section of V6 may have a maximum gain of 0.4. The gains of the bypass amplifiers are now controlled by adjustment of variable resistors R35 and R37. During the processor mode of operation, the proportion of delay and non-delay video that bypasses the multiplier stage can be independently controlled by the gain setting of the respective section of bypass amplifier V6, which is essentially operating in parallel with V3. The inputs to V6 are the same as the inputs to V3 and the outputs of both stages are developed across common plate load resistor R12.

(11) The bias of V3 is determined by the plate of V2 for grid 1 and the plate current of V7 for grid 7. This requires that the plate current of V2 and V7 be held constant for long periods of time to prevent performance degradation. The video gate, used to generate the video "quiet period" in the MTI system is used to operate gates for sampling the grid signals of multiplier stage V3. Video gate 1 is applied through connector P1-1 and coupled through capacitor C13 to the gate shaping circuit composed of diodes CR8, CR9, CR10, CR11, capacitor C14, resistors R22, R23, R24, and R25. The action of the gate shaping circuit is explained in (12) below.

(12) The operation of the video gates used in this circuit at a 150-volt reference requires that the video gate input be ac coupled. The gates must carry approximately 0.5 milliamps during the ON time, and must be back biased to cause adequate isolation during OFF time. The charge accumulated on coupling capacitor C13 when the input gate signal is positive shall be discharged through resistor R23 during the OFF time while the input gate signal is negative. The input signal is referenced to +142 volts which is obtained from the voltage divider network composed of resistors R26 and R28 between +150-volts and ground. Capacitor C14 stabilizes this voltage and holds it constant. When the positive input gate signal is coupled through capacitor C13 the +210 total voltage is the sum of the reference voltage and the +68 volt input signal. This voltage will close the gate switches for 23 microseconds, and the gate output will rise to +150-volts. After the 23 microsecond interval, the voltage across resistor R23 goes negative and the gate switches open. The gate output will at this time return to +142-volts and remain there until the next positive gate pulse is applied at connector P1-1 at the end of the sweep time of approximately 2000 microseconds. The video gate 2 signal is equal but opposite in polarity to the video gate 1 signal discussed. The input to the gates is prevented from rising above 210 volts in each channel by zener diodes CR9 and CR10 which are 68-volt diodes. The input voltage to the gates is prevented from dropping below 142-volts by the reference voltage established in the voltage divider consisting of resistors R26 and R28.

(13) For correct operation of the bias control loop, it is necessary that there be no signal present on the multiplier grid during the time between preknock and the leading edge of the test pulse. The preknock pulse, which is the opposite polarity of the video, is inserted into the circuit through the secondary windings of transformer T1. This distorted pulse prevents the charging of the short time constant coupling capacitors at the input of amplifiers V2 and V7 by the test pulse which is applied during the "quiet period".

(14) During the 23.5-microsecond ON time of the diode gates, a 7-microsecond positive signal and receiver noise are applied to the input of the two gates. One input is from the plate circuit of V7, and is applied at the junction of CR16 and CR17. The other signal is applied from the plate circuit of V2 to the junction CR14 and CR15. Since the gates are ON at this time, the positive 7-microsecond pulse and receiver noise are passed through the gates and applied to the grid of V5A or V5B Since AGC amplifiers V5A and V5B are identical, only the stage V5B will be discussed The grid of V5B is biased at a voltage between 0 and −10 volts by the voltage divider consisting of resistor R49 and BIAS ADJ variable resistor R48 between −250-volts and ground The amount of bias is determined by the brush arm setting of R48. C21 is a holding capacitor to hold the reference bias voltage constant. The 7-microsecond pulse and receiver noise are applied through capacitor C24 and diode CR23, developed across resistors R47 and R46, and applied to the grid of V5B. The positive pulse is blocked from the grid bias reference circuit by diode CR24, but is passed through CR23. Holding capacitor C20 is charged in the discharge path holds the current in V5B fairly constant for a long period of time. The discharge path for C20 is through resistor R46. The output of V5B is developed across plate resistor R45 and coupled through zener diode CR22 to holding capacitor C19. The voltage drop across normally conducting zener diode CR22 is held constant at 68 volts so that the screen grid of V7 is operating at a relatively low potential. This action tends to hold the gain of V7 constant for the long period of time between the video gate ON pulses. During the gate ON time, normal receiver noise causes the holding capacitor C19 to charge to a value determined by the noise level. The effect of the 7-microsecond test pulse which is applied during the preknock to sync time is offset by the application of a distorted preknock pulse of the opposite polarity which is coupled through the secondary windings of transformer T1. Therefore, the receiver noise level which is applied during the gate ON time determines the charge on holding capacitor C19 and establishes the gain level for V7 during the remainder of the sweep time.

32 (U). Miscellaneous Cabinet-Mounted Components in Director Station Group 8513626

a. General. In addition to the chassis covered in paragraphs 10 through 31, the director station group contains cabinet-mounted line attenuation, line compensation, and line decoupling circuits which are covered in this paragraph.

Note. The key letter-number combinations shown in parentheses in *b* below refer to zone locations in figure 25, TM 9–1430–257–20, unless otherwise indicated.

b. Detailed Theory.

(1) Frame-mounted test pulse adjust variable resistor R1 (D25) is located on the MTI frame in the director station group. Resistor R1 is inserted across the connecting cable between connector J3 (C14) on the acquisition-track synchronizer and connector J2 (B26) on the carrier oscillator. Since the test pulse is a critical reference voltage in the MTI system, compensation for line losses is necessary. Correct pulse amplitude is obtained when R1 is adjusted to provide a pulse amplitude of 5 divisions on the MTI oscilloscope.

(2) In the MTI frame, the +150-volt, +250-volt, and the −250-volt lines are decoupled through the RC circuits composed of resistor R4 (D27) and capacitor C1, resistor R2 and capacitor C2, and resistor R3 (D28) and capacitor C3, respectively. These networks ground transients to keep these spurious voltages out of the power supplies. Capacitor C8 (C28) performs a like function in the +250-volt supply line to the MTI synchronizer. The 6.3-volt filament voltage circuit to the MTI synchronizer is decoupled by capacitors C6 and C7. Capacitors C4 (C26) and C5 perform the same function in the MTI video amplifier filament supply line.

(3) The IF attenuator (fig. 18) compensates for the wide variations in gain that occur because of the cumulative effect of the tube circuit differences through twelve stages of amplification in the IF preamplifier (par. 72) and the IF amplifier (par. 10). The output from the IF preamplifier is applied through connector J1

to the brush arm of switch S1A. With the switch in the 0-db position, only the circuit consisting of resistors R32, R33, and R34 is connected into the series circuit between J1 and the output cable at connector P1. This circuit matches the output of the IF preamplifier to the input of the IF amplifier and establishes the zero reference for evaluating attenuation levels. As DB switch S1 is advanced, resistors R32, R33, and R34 are progressively connected to similar circuits, providing 0 to 20 db of attenuation in 5-db steps. As S1 is advanced, larger values of resistance are inserted in series with the signal leads. Simulated IF signals from radar signal simulator AN/MPQ-36 are applied through connector J2 to the matching attenuator path composed of resistors R35 and R36. This IF signal is applied directly to output connector P2 and is not controlled by the setting of switch S1.

(4) Note that the resistance of R5 is greater than R2, R8 is greater than R5, and R11 is greater than R8. Also note the progressive decrease in the resistance shunting the signal to ground. Resistor R1 is greater than R4, and R7 is greater than R10, thus allowing more signal current to return to ground as more attenuation is desired. The output from the IF attenuator is applied from the junction of resistors R34 and R35 through connector P1 to the external IF amplifier (C22).

(5) Terminating resistor R75 (C21) is a plug-in terminating resistor built into connector P74 for terminating the track range gate input to the video and mark mixer (par. 18). Resistor R6 (D9) is a load resistor for the +270-volt output of the +270v, −28v, and +75v or +175v power supply (par. 25).

(6) Transformers T1 (D13), T4 (A23), T5 (A19), and T6 (A23) are filament supply transformers for supplying 6.3 volts ac to the filament circuits of the chassis housed in the director station group. Secondary winding 3–4 of T1 supplies 6.3 volts ac to the MTI video amplifier (B26), carrier oscillator (B27), and MTI
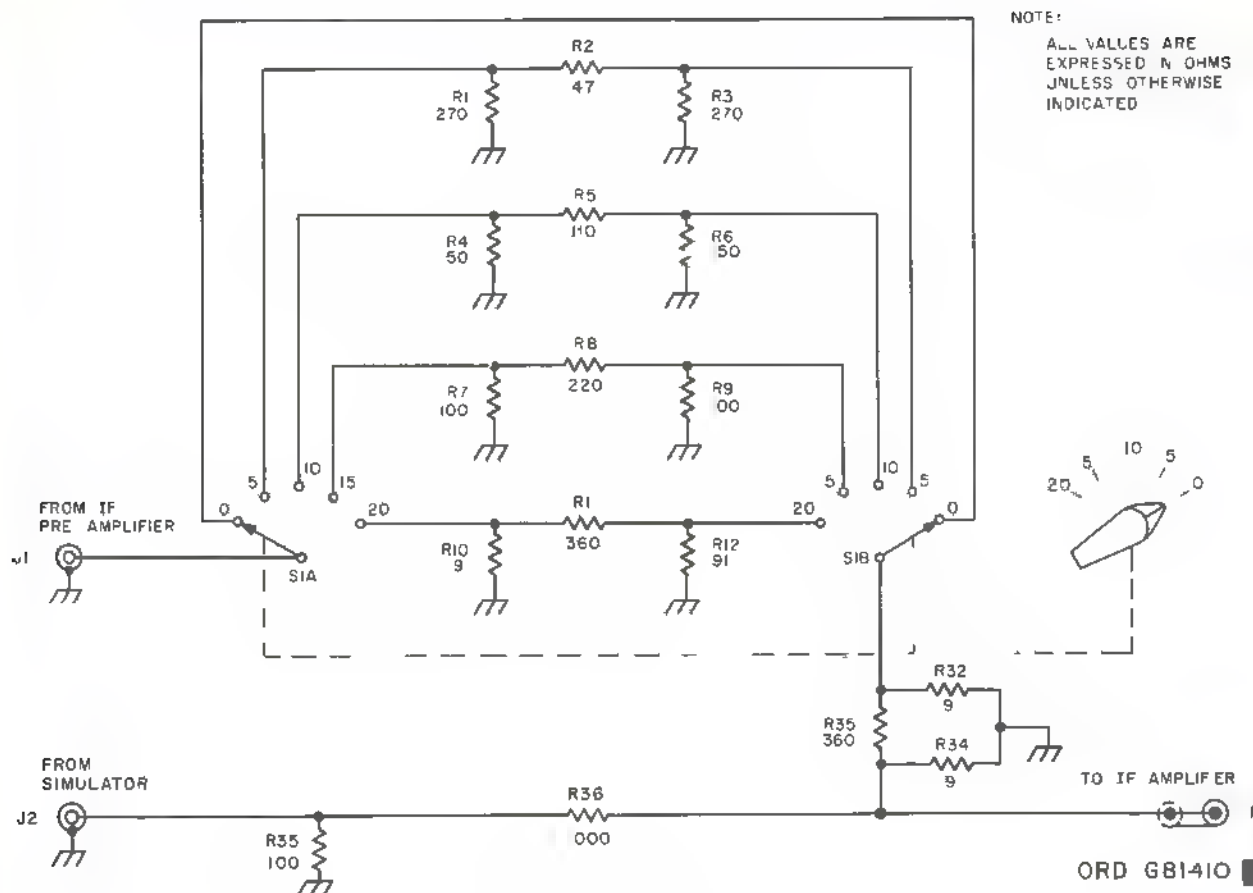
Figure 18 (U).   IF attenuator—simplified schematic diagram

oscilloscope (B29). Secondary winding 5-6 of T1 supplies the carrier oscillator (B27) and delay amplifier (B30). Secondary winding 7-8-9 of T1 supplies the trigger pulse generator (B22). Secondary winding 3-4 of T4, in parallel with winding 5-6, supplies the acquisition-track synchronizer (C14) and the video and mark mixer (D19). Secondary winding 7-8 of T4, in parallel with winding 9-10, supplies the alarm control (A14). Windings 3-4 with 5-6 and 7-8 with 9-10 are paralleled to provide greater current handling abilities. Secondary winding 11-12 of T4 supplies 6.3 volts ac, referenced at −250 volts dc, to the alarm control (A14), 4-kc oscillator (C14), and switching and mixer unit (B18). Secondary winding 3-4 of

T5 supplies 6.3 volts ac, referenced at −1000 volts dc, to the MTI oscilloscope (B29). Secondary winding 3-4 of T6 supplies regulated 6.3 volts ac to the switching and mixer unit (B18). Transformer T2 (D16) provides 120-volt ac generator excitation voltage to the servo systems in the acquisition radar system. Transformer T3 (C15) is the output load of the 4-kc oscillator and is discussed in paragraph 21.

(7) Fuse F1 (A8) protects the ±320v or +220v power supply from failures in the −250, +250, or +150 volt regulator. In systems 1001-1048, F1 is a 2-ampere fuse. In systems 1049 and above, F1 is a 1-ampere fuse. Indicator light I1 is a blown fuse indicator light which aids in locating a blown fuse

or malfunctioning circuit. Fuses F4, F5, and F6 (D4) protect the 120-volt, 3-phase circuits. This 3-phase voltage is supplied to radar signal simulator AN/MPQ-36. Fuse F7 (A10) protects the —250, +250, or +150-volt regulator from overload by radar signal simulator AN/MPQ-36. Fuse F8 (B10) protects the 28-volt circuit from overload by radar signal simulator AN MPQ-36. Fuse F9 (D3) protects the —24-volt circuit from overload in the FUIF interconnecting box.

(8) Interlock switches S3 (C11) through S8 (B6) protect the low-voltage circuits that supply the high-voltage circuits. When a door on the director station group or a slide is pulled out, one of the switches breaks the low-voltage circuit, thereby interrupting high-voltage circuit operation. This protects maintenance personnel from possible injury due to electric shock.

(9) BAL-NORMAL switch S9, GRD connector J56, and NVTS connector J55 provide facilities for balancing the +250 or +150-volt regulator, using the null voltage test set.

(10) Adapter Z60 (A17) and bridging unit Z61 (B13) are used to bridge existing circuits into radar signal simulator AN/MPQ-36. Z60 is used to bridge the IFF signals and Z61 is used to bridge the synchronizing pulse circuit.

c. *Differences Among Models.*

(1) MWO 9-1400-263-30 modifies the director station group to accept an auxiliary acquisition radar. Video and mark mixer 9142873 is replaced by video and mark mixer 9985613. Acquisition track synchronizer 9142937 is replaced by acquisition track synchronizer 9988748. Wires are changed and connections are added for the AAR capability. The theory of the miscellaneous cabinet mounted components is the same as in b above. Refer to figure 25.1, TM 9-1430-257-20

for the schematic reference showing changes made by MWO 9-1400-263-30.

(2) MWO 9-1400-268-50 modifies the director station group to add facilities for the antijam display capability. Trigger pulse amplifier 9160170 is replaced by acquisition interference suppressor 9990600. Acquisition power control panel 8153518 is modified. Switching and mixer unit 8513387 is replaced by electronic gate 9990560. Carrier oscillator 8513287 is replaced by delay line driver 9990570. Acquisition IF amplifier 7621810 is replaced by main acquisition IF amplifier 9990755. Alarm control 8158475 is replaced by fast AGC amplifier 9990768. Also, if MWO 9-1400-263-30 is not incorporated, the acquisition track synchronizer 9142937 is replaced by acquisition track synchronizer 9988748 and video and mark mixer 9142873 is replaced by video and mark mixer 9985613. The theory of the miscellaneous cabinet mounted components is the same as in b above. Refer to figure 25 2 or 25.3, TM 9-1430-257-20, for the schematic reference showing changes made by MWO 9-1400-268-50.

32.1 (U). Miscellaneous Cabinet-Mounted Components in Director Station Group 9145166

a. *General.* The director station group contains cabinet-mounted line attenuation, line compensation, and line decoupling circuits which are covered in this paragraph.

b. *Detailed Theory.* The theory of the miscellaneous cabinet-mounted components (fig. 86, TM 9-1430-257-20) is the same as that described in paragraph 32 except for HIPAR relays K1 and K2. HIPAR relays K1 and K2 are energized when the RADAR SELECT switch on the IFF control-indicator is set to HIPAR. Contacts of relays K1 and K2 select the appropriate signals for LOPAR or HIPAR operation.
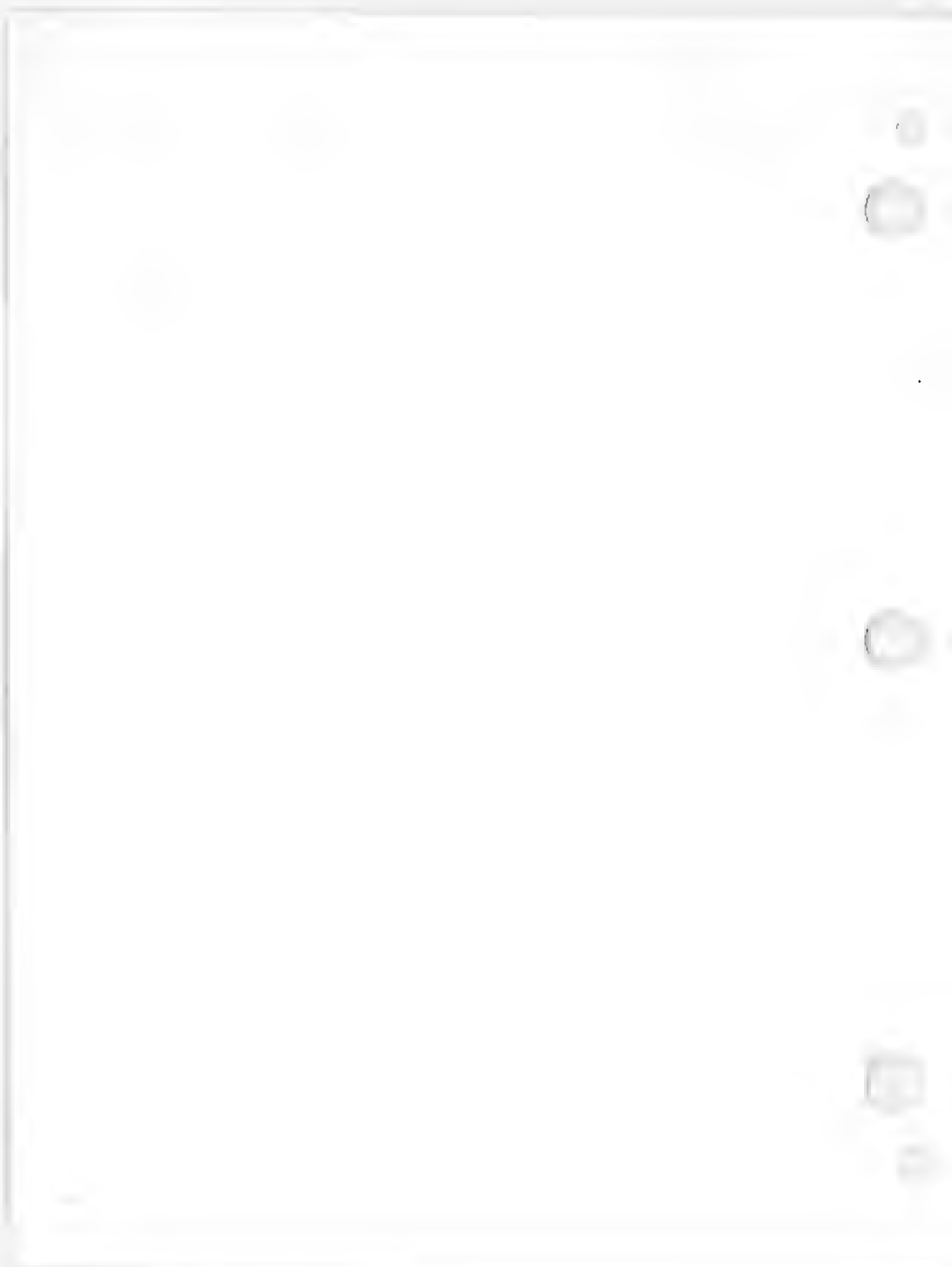
CHAPTER 3

BATTERY CONTROL CONSOLE

---

33. (CMHA) PPI 9142868
   a. General.

Note. The key letters shown in parentheses in (1) and (2) below refer to figure 19.

   (1) The PPI in the battery control console presents targets video (A) together with marks to designate range and azimuth settings of the acquisition and target tracking radar systems. The PPI display contains a rotating sweep (D) that rotates in synchronism with the acquisition antenna. The video and marks are presented on the rotating sweep. A choice of three range sweeps is available: 60,000, 120,000, or 250,000 yards.

   (2) The marks visible on the screen of the PPI in normal operation include acquisition range marks that occur once for every radial sweep and thereby describe a circle called the acquisition range circle (C) for indicating the range of a designated target; a flashing azimuth line (B) that occurs once every revolution of the acquisition antenna for indicating the azimuth of a designated target; the electronic cross (E) for indicating the azimuth and range settings of the target tracking radar system; and FUIF symbols for designating the status of a target. FUIF symbols are a defocused spot (F) indicating that another battery is tracking the target; a full circle (G) around the target indicating that the target is a foe; and a semicircle (H), concave down, around the target indicating that the target is a friend.

   (3) The PPI (fig. 4, TM 9-1430-257-20) contains 12 subassemblies listed in (a) through (f) below.
      (a) Modulation eliminator 8517883 or 9007951.
      (b) Sweep generator 8518032.
      (c) PPI dc amplifier 9005503 (2).
      (d) PPI video amplifier 9142869.
      (e) PPI marker generator 9007680.
      (f) Electronic gate 8517934 or 9007695 (6).

   b. Block Diagram Analysis (fig. 20).
   (1) The inputs to the modulation eliminator are the modulated 4-kc signals from the resolver amplifier in the acquisition antenna pedestal and a 4-kc reference carrier from the 4-kc oscillator. The modulated 4-kc signal inputs represent the outputs of the north-south (N-S) and east-west (E-W) windings of the acquisition azimuth resolver. The modulated 4-kc signals are converted into two sine waves by the modulation eliminator. The frequency of these sine waves is such that 1 cycle represents one revolution of the acquisition antenna. Thus, there are two quadrature sine-wave voltages from the modulation eliminator which represent the north-south and east-west components of the acquisition antenna azimuth. The output sine wave alternate above and below zero reference level.

(2) The two demodulated sine-wave voltages are applied to the sweep generator where they develop sawtooth sweep voltages. Sweep gate pulses developed in the PPI video amplifier are also applied to the sweep generator and are used to fix the duration of the sawtooth sweep voltages.

The duration of the sweep determines whether the range represents 60,000, 120,000, or 250,000 yards. The amplitude of each sawtooth sweep voltage varies in proportion to the acquisition antenna azimuth position.

(3) Electronic gates Z1 through Z6

A	— TARGET VIDEO	E	ELECTRONIC CROSS
B	FLASHING AZIMUTH LINE	F	IFF SYMBOL — BATTERY
C	ACQUISITION RANGE CIRCLE	G	IFF SYMBOL — FOE
D	ROTATING SWEEP	H	IFF SYMBOL — FRIEND

ORD G29137
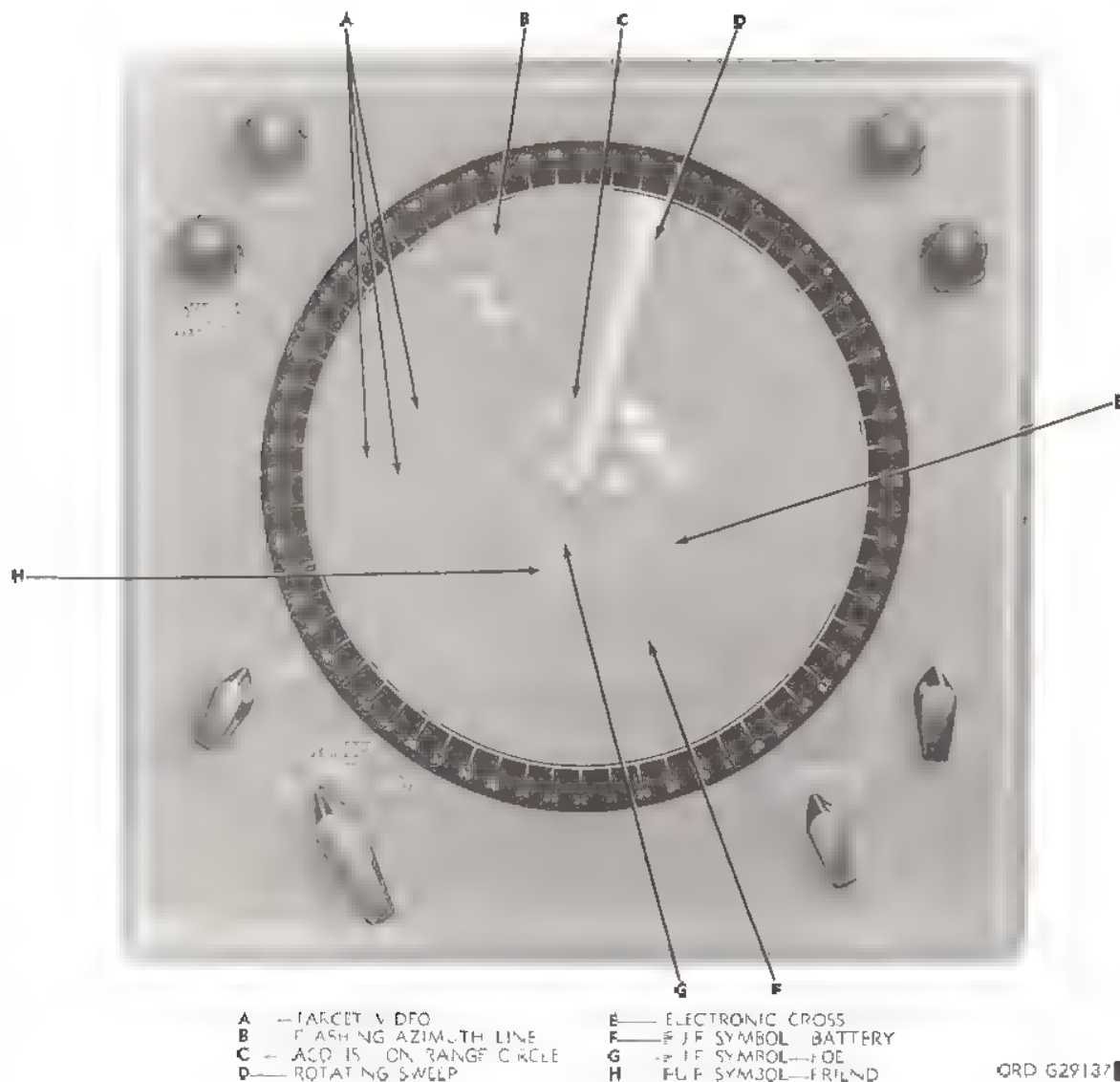
Figure 19. (CMHA) PPI—presentation.

are controlled by the gate control pulses from the PPI marker generator. The electronic gates are connected so that Z2 and Z4 are closed when Z1, Z3, Z5, and Z6 are open and vice versa. Thus, the PPI dc amplifiers receive either the N-S and E-W sawtooth sweep voltages from the sweep generator or the X analog and Y analog voltages from the FUIF equipment. Electronic gates Z5 and Z6 switch resistors R7 and R8 into the X analog and Y analog circuits when Z2 and Z4 are closed. This is done to maintain a constant load on the X analog and Y analog circuitry.

(4) The sawtooth sweep voltages from the sweep generator are then applied to the PPI dc amplifiers through Z1 and Z3. Each PPI dc amplifier provides an amplified push-pull output representing the input sawtooth sweep voltage. The two push-pull sawtooth sweep voltage outputs are then applied to the electrostatic deflection plates of cathode-ray tube V1. One PPI dc amplifier drives the north-south deflection plates and the other PPI dc amplifier drives the east-west deflection plates. A rotating sweep is obtained by the vector combination of the amplitudes of the sawtooth sweep voltages on the four deflection plates. Since the amplitudes of the individual sawtooth sweep voltages vary as the acquisition azimuth resolver outputs vary in amplitude and phase, a change in the angular position of the acquisition antenna produces an equal change in the resultant direction of the electrostatic deflection field. This resultant field produces the radial deflection of the sweep trace.

(5) The inputs to the PPI video amplifier are the sync pulse, the symbols unblanking pulse, and the low level acquisition video and marks. The PPI video amplifier amplifies the acquisition video and marks to a voltage level sufficient to intensity-modulate the electron beam of the CRT. It also supplies the sweep gate pulses to the sweep generator and the end of sweep pulse to the PPI marker generator.

(6) The inputs to the PPI marker generator are the end of sweep pulse, from the PPI video amplifier, the all data present (ADP) pulse from the FUIF equipment, and the symbol designations from the FUIF equipment (foe, friend, or battery signals). The outputs of the PPI marker generator are the gate control pulses which control electronic gates Z1 through Z6, the X symbol signal, the Y symbol signal, the symbols unblanking pulse, and the defocus pulse. The X symbol signal is fed to the east-west (E-W) PPI dc amplifier where it provides the necessary east-west deflection voltages to generate the foe or friend signals. The Y symbol signal is fed to the north-south (N-S) PPI dc amplifier where it provides the necessary north-south deflection voltages to generate the foe or friend signals. The defocus pulse is generated by the PPI marker generator when it receives the battery signal. The defocus pulse is then applied to the focus grid of the CRT.

Note. The key letter-number combinations shown in parentheses in c below refer to figure 4. TM 9-1430-257-20 unless otherwise indicated.

c. Detailed Theory. In addition to the subassemblies listed in a(3) above, the PPI contains cathode-ray tube V1 (C12) and associated circuitry. Associated controls are LIGHTS variable resistor R15 (D8), which controls the brightness of the panel lights; GAIN variable resistor R5 (B2), which controls the brightness of the acquisition video and marks; RANGE switch S2 (A7), which selects the range represented on the PPI; INTENSITY variable resistor R27 (D9), which controls the dc level of the unblanking pulses and therefore controls the brightness of the azimuth sweep; EXPANSION switch S3 (B8), EXPANSION POSITION variable resistor R19 (B9), and EXP-ADJ variable resistors R21 and R22 (B9), which control the expanded presentation on the PPI; SYMBOLS switch S1 (D2), which controls the symbols which appear on the PPI; SYMBOL INTENSITY variable resistor R39 which controls the brightness of the symbols; and FOCUS variable resistor R24 (C9), which controls the focus voltage applied to the CRT. Steerable azimuth line relay K1 (B2) removes the acquisition video and marks and replaces them with a steerable azimuth line and an intensified acquisition range mark. ACQ RANGE MARK variable resistor R4 (C2) is provided to adjust the intensity of the intensified acquisition range mark.

(1) Acquisition video and marks controls. Acquisition video and and marks from the video and mark mixer are applied through ACQ VIDEO connector J8 (B1), GAIN variable resistor R5, and contacts 5 and 11 of steerable azimuth line relay K1 to the PPI video amplifier. The setting of R5 determines the amplitude of the acquisition video and marks applied to the PPI video amplifier. This in turn determines the brightness of acquisition video and marks on the CRT screen. When K1 is operated, the acquisition video and marks are removed, and the acquisition range mark is the input signal to the PPI video amplifier. The acquisition range mark from the acquisition range generator is applied through ACQ MARK connector J7, ACQ RANGE MARK variable resistor R4, and contacts 6 and 11 of K1 to the PPI video amplifier. This input is an intensified acquisition range mark. Variable resistor R4 controls the brightness of the intensified acquisition range mark on the CRT in the same manner that R5 controls the acquisition video and marks. Resistor R6, capacitors C3 and C4, crystal diode CR6, and associated contacts of K1 are components of a blanking circuit in the PPI video amplifier. When K1 is operated, these components, in conjunction with the PPI video amplifier, blank the CRT. Blanking occurs when K1 switches from acquisition video and marks to the steerable azimuth line presentation on the CRT screen. This circuit is discussed in detail in paragraph 38b(2)(e).

(2) Symbols control. The position of SYMBOLS switch S1 (D2) determines the symbol signal input to the PPI marker generator. Switch S1 may be in the OFF, NORMAL, or BATTS position. In the NORMAL or BATTS position, the ADP pulse

from the FUIF equipment is applied through ADP connector J10, contacts 2 and 3 (in BATTS position) and contact 4 of S1 to the PPI marker generator. In the OFF position, symbol input signals from the electrical test panel are applied through connector J2-L and contacts 1 and 4 of S1 to the PPI marker generator. Switch S1 is placed in the OFF position during check and adjustment procedures.

(2.1) Symbol intensity. The setting of SYMBOL INTENSITY variable resistor R39 determines the amplitude of symbols unblanking pulse and therefore the brightness of the symbols.

(3) Range control. The position of RANGE switch S2 (A7) determines the range represented by the sweep on the CRT screen. Switch S2A connects -28 volts to contact 1, 11, or 12 of switch S1A in the PPI video amplifier and thus controls the sweep-length time of the PPI. Switch S2B and input resistors R9 through R14 control the gain of the PPI dc amplifiers. The gain of these amplifiers must be inversely proportional to the operating range so that the sweep length on the CRT will be constant for all settings of S2. The range represented by the sweep on the CRT is 60,000, 120,000, or 250,000 yards.

(4) Expansion controls. EXPANSION switch S3 (B8), EXPANSION POSITION variable resistor R19, and expansion-adjust resistor R21 control the expanded sweep on the CRT screen. The expanded sweep presentation is a portion of the radial sweep expanded to sweep the diameter of the CRT. The starting point of the expanded sweep is 1/2 inch from the periphery of the CRT. Variable resistor R19 controls the azimuth point on the periphery of the CRT where the expanded sweep starts. When S3 is in the ON position, -28 volts dc is applied through contacts 2 and 3 of S3A and contacts 8 and 9 of S3B to the PPI dc amplifiers. This voltage operates expansion relay K1 which doubles the overall gain of the PPI dc amplifier. Contacts 8 and 9 of S3A and contacts 2 and 3 of S3B apply offset voltages from R19 to the PPI dc amplifiers for the expanded sweep presentation. EXP ADJ-DIAMETER variable resistor R21 and EXP ADJ-CENTER variable resistor R22 are provided for sweep centering adjustment. Resistors R18 and R20 are voltage dropping resistors. Resistors R16 and R17 serve as input resistors for the offset voltage applied to the PPI dc amplifiers.

(5) Cathode-ray tube V1. Cathode-ray tube V1 (C12) is the electrostatic type. A heated cathode provides a source of electrons, a control grid determines the number of electrons flowing through CRT, and an accelerating grid speeds the electrons in their flight to a fluorescent screen. The cathode, control grid, and accelerating grid are cylindrical in shape and are placed so that their axes are coincident with the axis of the CRT. Focusing is accomplished by varying the voltage on the focus grid. Deflection is accomplished by applying a voltage of the desired waveshape to the deflection plates.

(a) When the CRT is unblanked by the unblanking pulse, electrons that are emitted from the cathode can pass through the control grid to reach the fluorescent screen. The unblanking pulse applied to the control grid is produced in the PPI video amplifier. It consists of a positive-going square wave with a duration depending on the selected range. Atop the unblanking pulse are the acquisition video and marks. The unblanking pulse is applied to the control grid in synchronism with the sawtooth sweep voltage and results in unblanking of the CRT during the sweep. The dc level of the voltage applied to the control grid is set by INTENSITY variable resistor R27 (D9) controlled by the INTENSITY knob on the front panel of the PPI. Resistors R27, R26, R25, R24, and R23 form a voltage divider between the -8,000-volt supply and ground. Voltage for the control grid, cathode, and focus grid are tapped off the voltage divider. Clamper tube V3 clamps the cathode of V1 at a fixed potential by regulating the voltage drop across resistor R26. Crystal diodes CR1, CR2, and CR3, indicators I5, I6, and I7, and resistors R28 and R29 form a clamping circuit to insure that input signals at the control grid start from the same reference level. Positive-going signals are developed across R28 and R29. Negative-going signals drive CR1, CR2, CR3, I5, I6, and I7 into conduction, and signals are

bypassed to ground through capacitor C1 in the PPI HV power supply (par. 50). Capacitor C1 is connected between the brush arm of R27 (D9) (through connector J3 (B1) of the PPI and connector J2 of the PPI HV power supply) and ground.

(b) The acquisition video and marks that appear on the screen of the CRT are applied to the control grid. These signals effectively reduce the bias on the control grid, resulting in intensity modulation of the electron beam. The adjustment of GAIN variable resistor R5 on the front panel of the PPI determines the level of the signal applied to the control grid, thereby controlling the degree of modulation.

(c) After passing the control grid, the electron beam passes through the accelerating grid which accelerates the beam. Resistors R30 through R33 and R35 through R38 are accelerating grid dropping resistors, developing the accelerating grid voltage. Capacitor C6 is the accelerating grid bypass capacitor.

(d) After passing through the accelerating grid, the electron beam is focused by varying the intensity of the electrostatic field which is set up along the axis of the CRT by the focus grid. Electrons which are moving exactly along the electrostatic field set up by the focus grid are not deflected since they are moving parallel to the electrostatic field. All divergent electrons are acted on by

the electrostatic field, which produces inward radial accelerations and brings the electrons together at a common point. This common point is known as a focus point and is a function of the intensity of the electrostatic field. When the field is adjusted so that the focus point is at the screen of the CRT, the electron beam is properly focused. The voltage on the focus grid is controlled by FOCUS variable resistor R24. When a positive defocus pulse from the PPI marker generator is applied to transformer T1, a positive pulse at T1-4 (with respect to T1-3) is developed. This pulse is applied directly to the focus grid, resulting in a change in the focusing voltage. Therefore the electron beam focus point is changed, resulting in a defocused spot on the CRT screen. Capacitor C7 is a decoupling capacitor for the dc voltage at the brush arm of R24.

(e) Electrostatic deflection is accomplished by applying a linear sweep voltage to the deflection plates. With no signals applied to the deflection plates, each deflection plate maintains a +1,550-volt dc potential. The sweep voltages applied to the deflection plates are positive-going and negative-going sawtooth voltages varying in amplitude about the +1,550-volt dc level. The beam deflection is proportional to the amplitude of the sawtooth sweep voltage applied to each plate, and the individual deflections add

vectorially. When the acquisition antenna is pointing west, the north and south fields are equal in amplitude and cancel each other. The west field is maximum and the east field is minimum, so the result is a west field and the sweep on the PPI is to the left (west). One quarter of a revolution later the east and west fields cancel; the north field is maximum and the south field minimum. The antenna is pointing north and the sweep on the PPI is pointing up.

(6) <u>Power supply decoupling and voltage regulator.</u> Resistors R1 (C1), R2 and R3 and capacitors C1A, C1B, C2, C8, C9, and C10 provide decoupling from the +250-, +150-, and -250-volt supplies. Resistor R34 and voltage regulator V2 provide a regulated -87 volts dc to the two PPI dc amplifiers.

34. (U) Modulation Eliminator 8517883, 9007951

a. <u>General.</u> The modulation eliminator generates sweep voltages for use by the sweep generator to produce the rotating sweep on the PPI screen. The modulation eliminator receives three input signals; a 4-kc reference carrier and two amplitude-modulated 4-kc signals from the resolver amplifier (par. 56). The output from the modulation eliminator is two sine waves, 90° out of phase with respect to each other. The two sine waves represent the north-south and east-west azimuth position of the acquisition antenna. The sine waves are applied to the sweep generator, which generates sawtooth sweep voltages that produce the rotating sweep.

b. <u>Detailed Theory.</u> The modulation eliminator (fig. 5, TM 9-1430-257-20)

consists of two crystal bridge demodulators; one in the north-south (Y) channel and the other in the east-west (X) channel. Both demodulators receive a constant-amplitude 4-kc reference carrier (fig. 21). This signal enters the modulation eliminator at connectors P1-1 and 2 (fig. 5, TM 9-1430-257-20). In addition to the 4-kc reference carrier, both demodulators receive a modulated 4-kc signal (fig. 21). The Y input is at connectors P1-3 and 4 (fig. 5, TM 9-1430-257-20) and the X input is at P1-5 and 6. The modulated 4-kc signal is a 4-kc carrier modulated by sine-wave voltages. The frequency of the sine wave corresponds to the rate of rotation of the acquisition antenna. Thus, 1 cycle of the sine wave corresponds to one revolution of the antenna. The modulated 4-kc signals and the 4-kc reference carrier are in phase for one-half revolution of the acquisition antenna and 180° out of phase during the next one-half revolution. The 4-kc reference carrier applied through P1-1 and 2 to the primary of transformer T1 causes a switching action in the demodulators. Since both demodulator channels are identical, only the Y channel will be explained in (1) through (6) below. Consideration will first be given to the demodulator with only the 4-kc reference carrier applied. Then, operation of the demodulator will be considered with the 4-kc reference carrier and the modulated 4-kc signal applied, and the sequence of events traced through one complete revolution of the antenna.

(1) The 4-kc reference carrier is applied to the demodulator through T1. Assume that during the first half-cycle of the 4-kc reference carrier, T1-4 is positive and T1-6 is negative. The voltage across the demodulator causes crystal diodes CR3 and CR4 to conduct equally. Current flows from T1-5 and

T1-6 through resistor R3, CR3, resistor R4, and CR4 to T1-4 and T1-5. During this half-cycle, crystal diodes CR1 and CR2 are not conducting because of the negative voltage at the plate of CR1 from T1-6 and the positive voltage applied through resistor R2 to the cathode of CR2 from T1-4.

(2) During the next half-cycle, T1-6 is positive and T1-4 is negative. Crystal diodes CR1 and CR2 conduct equally and CR3 and CR4 are cut off. Current flows from T1-5 and T1-4 through resistor R2, CR2, resistor R1, and CR1 to T1-6 and T1-5. It can be seen from this that the 4-kc reference carrier acts as a switching voltage. However, the bridge is balanced and there is no output across load resistor R13.

(3) Operation of the demodulator with both inputs applied is now considered. Assume that the acquisition antenna is rotating between 4,800 and 1,600 mils. (It should be remembered that the acquisition azimuth resolver rotates counterclockwise as the antenna rotates clockwise. However, the modulated 4-kc output signals of the acquisition azimuth resolver represent the clockwise rotation of the acquisition antenna.) The 4-kc reference carrier and the modulated 4-kc signal are in phase. Also, assume that T1-4 and T2-4 are positive and T1-6 and T2-6 are negative during the first half-cycle of the 4-kc signals. As a result of these voltages, the bridge is unbalanced and CR4 conducts more than CR3. The net current path is from ground through R13, T2-
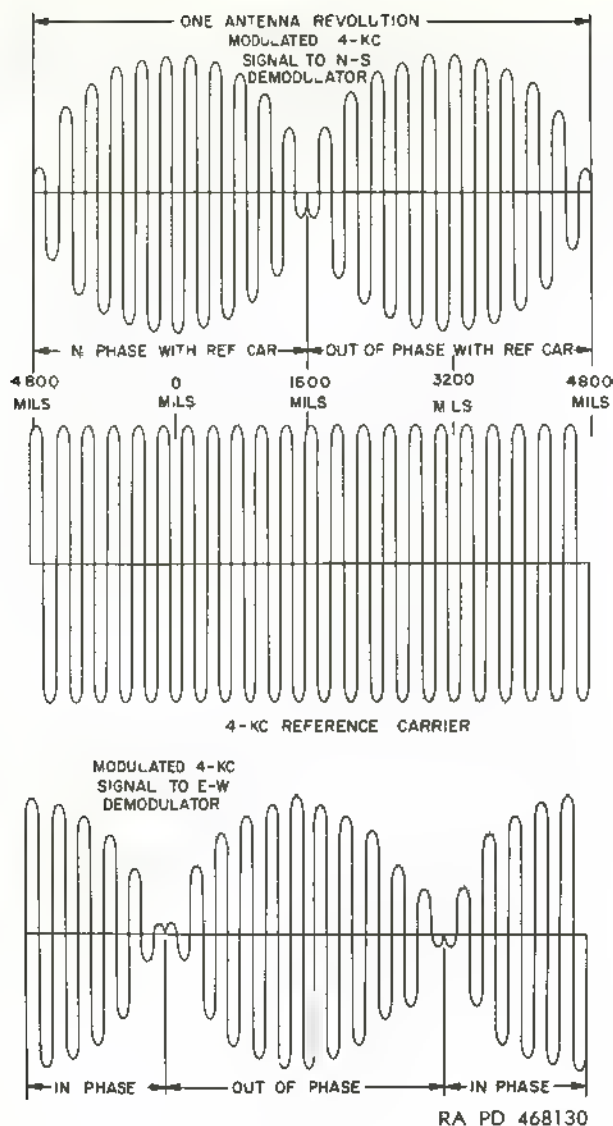
Figure 21. (U) Modulation eliminator - input waveforms.

5 and T2-6, R4, CR4, and T1-4 and T1-5 back to ground.

(4) During the second half-cycle (inputs still in phase) T1-6 and T2-6 are positive and T1-4 and T2-4 are negative. As a result of these voltages, the bridge is unbalanced and CR1 conducts more than CR2. The net current path is from ground through R13, T2-5 and T2-4, R1, CR1, and T1-6 and T1-5 back to ground. Current flow through resistor R13 is the same for both half-cycles, resulting in a positive output signal to resistor R5. Current flow continues in this direction until the next 3,200 mils (1,600 to 4,800) of acquisition antenna rotation.

(5) When the acquisition antenna is rotating between 1,600 and 4,800 mils, the 4-kc reference carrier and modulated 4-kc signal are 180° out of phase. Assume that during the first half-cycle of the 4-kc signals, T1-4 and T2-6 are positive and T1-6 and T2-4 are negative. The bridge is unbalanced and CR3 conducts more than CR4. The net current path is from ground through T1-5 and T1-6, R3, CR3, T2-6 and T2-5, and R13 back to ground. During the second half-cycle of the 4-kc signals (inputs still out of phase), T1-6 and T2-4 are positive and T1-4 and T2-6 are negative. Again the bridge is unbalanced and CR2 conducts more than CR1. The net current path is from ground through T1-5 and T1-4, R2, CR2, T2-4 and T2-5, and R13 back to ground. Current flow through R13 is in the same direction for both half-cycles of the 4-kc signals. However, current flows in the opposite direction to that which flows when the inputs are in phase. This results in a negative output signal to R5.

(6) The sine-wave output of the demodulator, developed across R13, is applied to the RC filter network consisting of resistor R5, capacitor C1, resistor R6, and capacitor C2. The purpose

of the filter network is to re-
move the 4-kc component of
the output signal. After filter-
ing, the sine-wave output sig-
nal is applied to connector P1-9.

(7) ZERO SET-Y switch S1 and
ZERO SET-X switch S2 ground
the inputs to transformers T2
and T3 when placed in the OFF
position. Connects P1-3 and 5
are externally grounded in the
target designate control-indi-
cator. When S1 and S2 are in
the OFF position, both sides of
the primaries of T1 and T2 are
grounded. This results in zero
output from the modulation
eliminator. Switches S1 and S2
are placed in the OFF position
during check and adjustment
procedures of the sweep gen-
erator.

(8) In summary, the modulation
eliminator receives two mod-
ulated 4-kc signals 90° out of
phase. The modulated 4-kc sig-
nals and the 4-kc reference
carrier are in phase for 3,200
mils (180°) of the acquisition
antenna revolution and out of
phase for the other 3,200 mils
(180°). In the modulation elim-
inator, the 4-kc signals develop
two sine-wave outputs. The fre-
quency is such that 1 cycle of
the sine-wave output represents
one revolution of the acquisition
antenna. Figure 22 shows the
outputs of both channels of the
modulation eliminator.

c. Modulation eliminator - 9007951.
Beginning with system 1181 modulation
eliminator - 9007951 replaces modula-
tion eliminator - 8517883. ZERO SET
-Y OFF switch S1 and ZERO SET -X
OFF switch S2 are replaced by a 3
position rotary switch (S1). The three
positions are stamped X OFF, NORM,
and Y OFF providing the same func-
tions as S1 and S2 in modulation elim-
inator - 8517883.

35. (U) Sweep Generator 8518032
a. General. The sweep generator
provides two variable amplitude saw-
tooth sweep voltages, 90° out of
phase with each other. These saw-
tooth sweep voltages are developed
from two idependent sine-wave in-
put signals 90° out of phase with
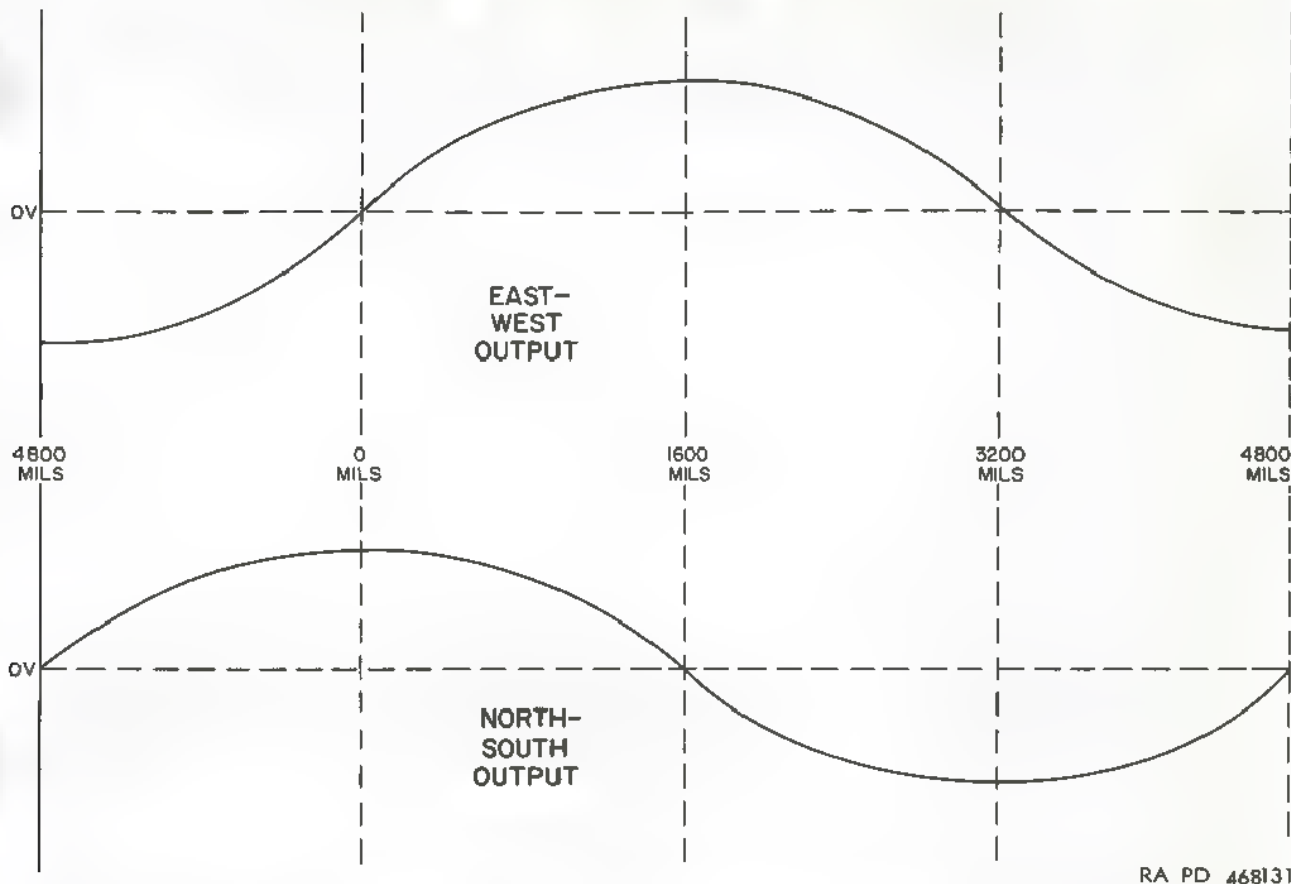
RA PD 468131

Figure 22 (U) Modulation eliminator—output waveforms.

each other, representing the N–S and E–W coordinates of the acquisition antenna position. The sawtooth sweep voltages are used to drive the deflection plates of the PPI located in the battery control console. Since the N–S and E–W channels of the sweep generator are identical except for component designation, only the N–S channel is discussed in *b* below.

   b. Detailed Theory.

      (1) *YDC amplifier V1.*

         (*a*) The N–S input signal to YDC amplifier V1A (fig. 6, TM 9-1430-257-20) is a sine-wave voltage (A, fig. 23). The frequency of this sine-wave voltage corresponds to the rate of rotation of the acquisition antenna. Maximum frequency is 0.25 cps, occurring at the maximum antenna rotation rate of 15 rpm.

The N–S output signal (C, fig. 23) of the sweep generator consists of positive and negative sawtooth sweep voltages, depending upon whether the N–S input signal is in the positive or negative half of its cycle, respectively. Sweep gate pulses (B, fig. 23), applied from the PPI video amplifier to electronic gate Z1 (fig. 6, TM 9-1430-257-20), determine the sweep time of each sawtooth voltage by effectively turning the sweep generator on and off. The repetition rate of these sweep gate pulses is 500 pps. Electronic gate Z1 is discussed in (4) below. The amplitude of the N–S output sawtooth sweep voltage at a given instant depends on the amplitude of the N–S input sine-wave voltage at

CONFIDENTIAL

that instant; therefore, the amplitude of the sawtooth sweep voltage will vary accordingly. The locus of points representing the peaks of successive

N–S output sawtooth sweep voltages will be a replica of the N S input sine wave. The frequency of the N S input signal is small compared to the fre-

INPUT SIGNAL AT PI–1

O VOLTS

A

ELECTRONIC GATE ZI OPEN

ELECTRONIC GATE ZI CLOSED

SWEEP GATE PULSES AT PI–6

O VOLTS

ELECTRONIC GATE ZI OPEN

ELECTRONIC GATE ZI CLOSED

SWEEP GATE PULSES AT PI–5

O VOLTS

B

SAWTOOTH SWEEP VOLTAGE OUTPUT AT PI–9

O VOLTS

C
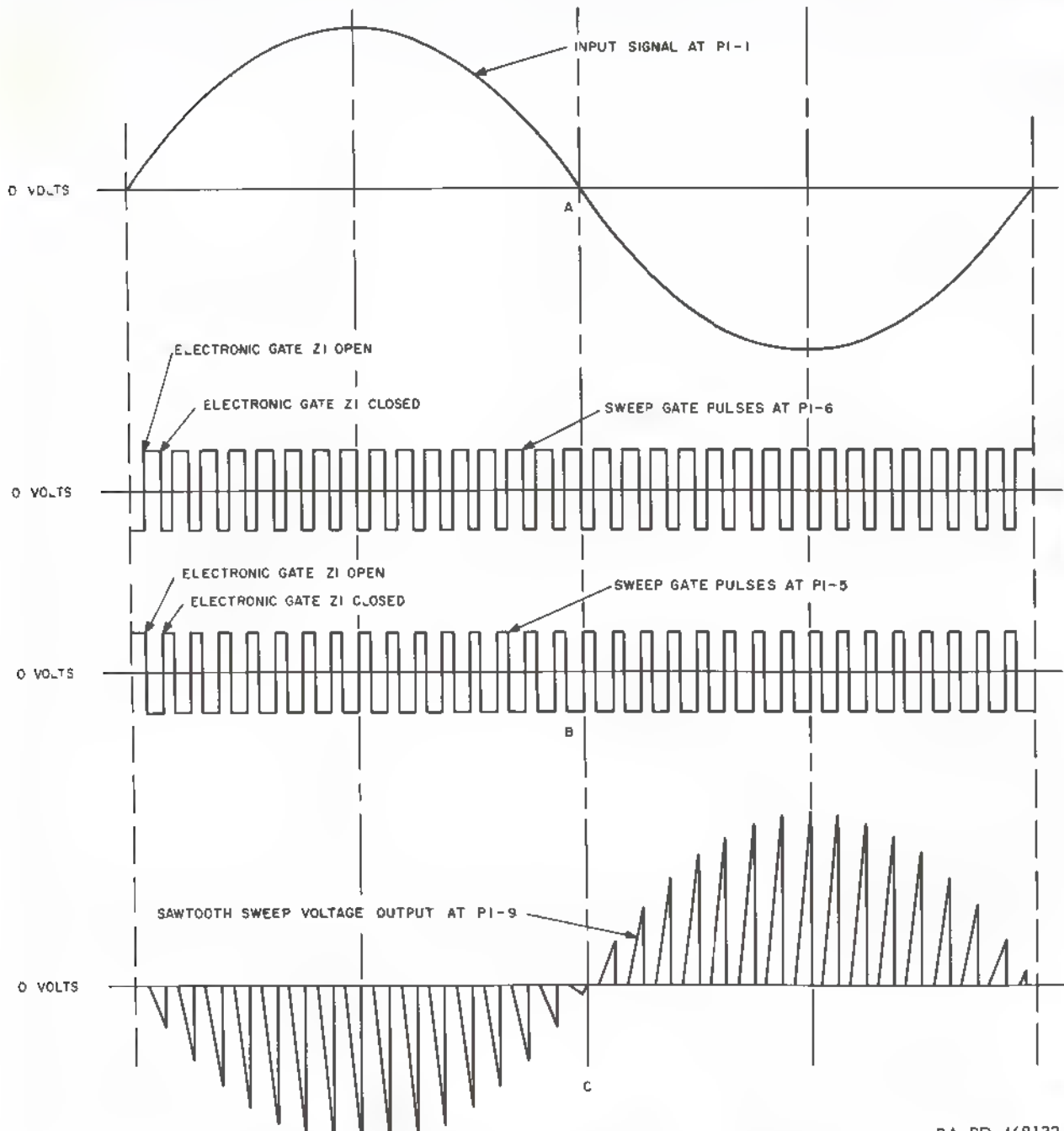
RA PD 468132

Figure 23   (U) Sweep generator—N–S channel input and output waveforms.

CONFIDENTIAL

quency of operation of the sweep generator as determined by the sweep gate pulses. Therefore, the N–S input signal for any 1 cycle of sweep generator operation can be considered as a dc voltage for that cycle. In the discussion below, only 1 cycle of sweep generator operation will be discussed; therefore, the N–S input signal applied to the grid of V1A will be considered as a dc voltage.

(*b*) The N–S input signal is applied at connector P1 1 and coupled through Y slope variable resistor R1 and resistor R2 to the grid of V1A. The Y slope variable resistor R1 controls the amplitude of the N–S input signal to the grid of V1A and is adjusted for required output sweep amplitude. With the N–S input signal in its positive half-cycle and for 1 cycle of sweep generator operation, a positive dc voltage is applied to the grid of V1A. Conduction of V1A increases, causing an increase in current through common cathode resistor R4. The voltage rise on R4 increases bias voltage on the grid of Y dc amplifier V1B, resulting in a voltage rise at the plate of V1B. Therefore, the positive dc voltage at the grid V1A produces a positive dc voltage output at the plate of V1B. The opposite effect on V1A and V1B occurs for a negative dc voltage applied to the grid of V1A. Fixed negative bias voltage for V1B is furnished through the voltage divider consisting of resistor R6, Y zero set variable resistor R7, and resistor R8 connected between the +250-volt and –250-volt supplies. The Y zero set variable resistor R7 is adjusted to provide a zero output at the cathode of Y cathode follower V5A under no signal conditions. The output of V1B is developed across plate load resistor R3. The RC network, composesd of capacitor C2

and resistor R9, stabilizes the plate voltage of V1B assuring that the plate signal will always start at the same potential.

(2) *YDC amplifier V2.* The output from the plate of V1B is coupled through resistor R10 and capacitor C11 to the grid of YDC amplifier V2. Capacitor C11 shunts R10, and its purpose is to increase high frequency response. The bias voltage for V2 is developed across the voltage divider consisting of resistors R11, R10, and R3 connected between the +250-volt and –250-volt supplies. Screen grid voltage for V2 is furnished through the voltage divider consisting of resistors R14 and R15 connected between the +150-volt supply and ground. The positive dc voltage from V1B applied to the grid of V2 increases conduction through V2, which raises the voltage drop across plate load resistor R12 and lowers plate voltage. Therefore, the positive dc voltage at the grid of V2 produces a negative dc voltage output at the plate of V2. The opposite effect on V2 occurs for a negative dc voltage applied to the grid of V1A.

(3) *Y cathode follower V5A.* The output from the plate of V2 is coupled through resistor R13 and capacitor C3 to the grid of Y cathode follower V5A. Capacitor C3 shunts R13, and its purpose is to increase high frequency response. Signal voltage on the grid of V5A is developed across resistor R16. In absence of a signal on the grid, the cathode of V5A is at zero potential due to current flow through resistor R17 and V5A. A negative dc voltage at the grid of V5A decreases cathode current and results in a negative dc output. A positive dc voltage at the grid of V5A has the opposite effect on V5A. The output of V5A is applied to connector P1 9, to feedback capacitor C1, and to Z1 for development of the sawtooth sweep voltages (C, fig. 23).

CONFIDENTIAL

(4) *Electronic gate Z1.*

> *Note* Refer to paragraph 36 for a detailed analysis of the electronic gate.

(a) Two sweep gate pulses are applied from the PPI video amplifier to Z1 through P1-6 and 5. These two sweep gate pulses (B, fig. 23) are 180° out of phase with each other. With no sweep gate pulses applied, the grid of V1A (fig. 6, TM 9-1430-257 20) is held to ground potential through the −250-volt supply, resistor R1 at terminal 4 in Z1, crystal diode CR1 at terminal 1 in Z1, Y bal variable resistor R5, crystal diode CR2 at terminal 2 in Z1, resistor R2 at terminal 6 in Z1, and the +250-volt supply. The Y bal variable resistor R5 is adjusted to provide a zero voltage at the grid of V1A under no signal conditions. The output from the cathode of V5A is held to ground potential through the −250-volt supply, resistor R1 at terminal 4 in Z1, two crystal diodes CR5 and CR6 in Z1, resistor R2 at terminal 6 in Z1, and the +250-volt supply. Therefore, with no sweep gate pulses applied to Z1, the output of V5A is at ground, and feedback capacitor C1 has no effect on the input of V1A.

(b) Application of the positive-going leading edge and negative-going leading edge of the sweep gate pulses at P1-6 and 5, respectively, switches Z1 to an open position and lifts the output of V5A from ground; this couples the output of V5A through C1 to the input of V1A. With a positive dc voltage applied to the grid of V1A, the negative dc voltage from the cathode of V5A charges C1 slowly at a linear rate for the duration of the single sweep gate pulses applied at P1 6 and 5. When the two sweep gate pulses applied at P1-6 and 5 reverse polarity, Z1 returns to the normally closed condition and capacitor C1 discharges rapidly through CR6 in Z1, R2 in Z1, and the +250-volt supply; this action results in returning the cathode of V5A to ground potential. The linear charge and rapid discharge of C1 provides a sawtooth sweep voltage output (C, fig. 23) at P1 9 (fig. 6, TM 9-1430-257-20), with an amplitude dependent upon the instantaneous amplitude of the input signal at the grid of V1A.

(c) Capacitor C4 and Y zero variable capacitor C5 balance the gate pulses applied to Z1 so that no sweep gate pulse appears at any time at the grid of V1A. With the sweep gate pulses applied to Z1 and no input signal applied to the grid of V1A, Y zero variable capacitor C5 is adjusted to provide a zero output from Z1 by cancelling the sweep gate pulses across R5. The repetition rate of the sweep gate pulse is 500 pps. Therefore, the number of sawtooth sweeps developed by C1 during 1 cycle of input signal to V1A is a function of the acquisition antenna rotation rate. With an antenna rotation rate of 0.25 cps (15 rpm), C1 provides 2,000 variable amplitude output sawtooth sweeps per cycle of antenna rotation. With an antenna rotation rate of 0.166 cps (10 rpm), C1 provides 3,000 variable amplitude output sawtooth sweeps per cycle of antenna rotation. With an antenna rotation rate of 0.0833 cps (5 rpm), C1 provides 6,000 variable amplitude output sawtooth sweeps per cycle of antenna rotation.

36. Electronic Gate 8517934

a. *General.* Eight electronic gates are used in the PPI of the battery control console. Two gates are used for determining the sweep time of the sawtooth sweep voltage from the sweep generator by starting and stopping each sweep voltage. For an understanding of the application of the two electronic gates as used in conjunction with the sweep generator, refer to paragraph 35. The re-

CONFIDENTIAL

maining six electronic gates allow the inputs to the PPI dc amplifiers to be switched between the sweep generator sawtooth sweep voltage output and the FUIF output position voltage. For an understanding of the application of the six electronic gates as used in the PPI, refer to paragraph 33. Only the basic theory of the electronic gate is discussed in *b* below.

b. Detailed Theory. The electronic gate (fig. 6, TM 9–1430–257 20) consists of crystal diode gates one and two. Crystal diode gate one (fig. 24) consists of crystal diodes CR1, CR3, CR5, and resistor R1. Crystal diode gate two consists of crystal diodes CR2, CR4, CR6, and resistor R2. Crystal diode gate one is capable of passing only positive input signals, and crystal diode gate two is capable of passing only negative input signals. The electronic gate is a combination of crystal diode gates one and two and is considered equivalent to a single-pole, single-throw switch capable of passing both positive and negative input signals. Two gate control pulses are applied simultaneously but 180° out of phase with each other, and together open or close the electronic gate. The electronic gates are on-off switching devices and do not switch from one input signal to another.

(1) In the quiescent state of the electronic gate with neither input signals nor gate control pulses applied, terminals 1, 2, and 3 are at ground potential. Current flows from the −250-volt supply through terminal 4 and resistor R1 where it divides equally at point A and follows two paths: one path is through CR1, terminals 1 and 2, CR2, and point B; the other path is through CR5, CR6, and point B. The two currents combine at point B and flow through resistor R2, terminal 6, and to the +250-volt supply. The condition stated above occurs because the voltage supplies are equal and opposite, resistors R1 and R2 are equal, and the forward resistance of the crystal diodes is essentially equal. The input and output points at terminals 1, 2, and 3 are at the center of the bridge network. Thus, terminals 1, 2, and 3 are at ground potential.

(2) The two gate control pulses are applied to the electronic gate at terminals 5 and 7. Consider the electronic gate at one instant of time as having a positive voltage applied at terminal 7 and a negative voltage applied at terminal 5. Under these conditions, current flow is from the −250-volt supply through terminal 4, R1, CR3, terminal 7, an external circuit, terminal 5, CR4, R2, terminal 6, and to the +250-volt supply. Thus, the voltage at point A becomes more positive than when at quiescence because of the larger voltage
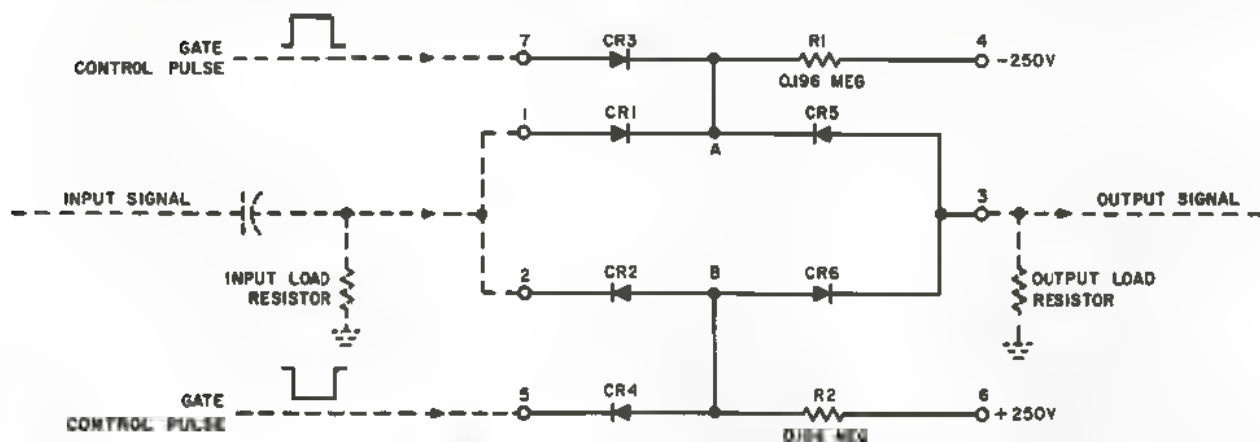
Figure 24. (U) Electronic gate—schematic diagram.

RA PD 468133

drop across R1. This positive voltage cuts off CR1 and CR5. The voltage at point B becomes more negative than when at quiescence because of the larger voltage drop across R2. This negative voltage cuts off CR2 and CR6. With CR1, CR2, CR5, and CR6 biased below cutoff, there can be no output signal through terminal 3 with either positive or negative input signals applied at terminals 1 and 2.

(3) If the polarity of the gate control pulses applied at terminals 7 and 5 is reversed, there is a negative voltage applied at terminal 7 and a positive voltage applied at terminal 5. This voltage cuts off current flow through CR3 and CR4, returning the electronic gate to its quiescent condition. At quiescence, CR1, CR2, CR5, and CR6 are biased to conduct as explained in (1) above.

(4) With the electronic gate in its quiescent state and a positive input signal applied at terminals 1 and 2, current flows from ground through the input load resistor to the external input signal source. At the same instant, current flows from the −250-volt supply through terminal 4, R1, CR1, terminal 1, and to the external input signal source. The positive input signal at terminals 1 and 2 biases CR2 below cutoff. Assuming the positive input signal does not exceed +50 volts amplitude, the voltage at point A and across the output load resistor simultaneously follows the polarity of this positive input signal. Therefore, as point A becomes more positive, less current flows from the −250-volt supply through R1, CR5, CR6, R2, terminal 6, and to the +250-volt supply. At the same instant, current increases from ground through the output load resistor, terminal 3, CR6, R2, terminal 6, and to the +250-volt supply. Thus, the voltage drop across the output load resistor simultaneously develops the output signal of the same polarity as the positive input signal.

(5) For a negative input signal applied at terminals 1 and 2 current flows from the external input signal source through the input load resistor to ground. At the same instant, current flows from the external input signal source through terminal 2, CR2, R2, terminal 6, and to the +250-volt supply. The negative input signal at terminals 1 and 2 biases CR1 below cutoff. Assuming the negative input signal does not exceed 50 volts amplitude, the voltage at point B and across the output load resistor simultaneously follows the polarity of this negative input signal. Therefore, as point B becomes more negative, less current flows from the −250-volt supply through R1, CR5, CR6, R2, terminal 6, and to the +250-volt supply. At the same instant, current increases from the −250 volt supply through terminal 4, R1, CR5, terminal 3, the output load resistor, and to ground. Thus, the voltage drop across the output load resistor simultaneously develops the output signal of the same polarity as the negative input signal.

(6) The following circuit description is based on the assumption that the input signals exceed ±50 volts amplitude.

(a) Should positive input signals in excess of +50 volts amplitude be applied at terminals 1 and 2, CR2 would remain cut off and CR5 would be cut off. This would result in positive peak clipping for input signals above +50 volts amplitude. Crystal diode CR5 would be cut off with positive input signals in excess of +50 volts amplitude because more current would flow through R1, causing a higher voltage drop across R1. This higher voltage drop across R1 would make point A and the cathode of CR5 more positive than the plate of CR5. The voltage drop across the output load resistor cannot be made large enough to cause CR5 to conduct. Therefore, any positive input signals in excess of +50 volts amplitude would

bias CR5 below cutoff. As a result, positive voltage limiting takes place across the output load resistor because the current path is from ground through the output load resistor, terminal 3, CR6, R2, terminal 6, and to the +250-volt supply.

(*b*) Should negative input signals in excess of −50 volts amplitude be applied at terminals 1 and 2, CR1 would remain cut off and CR6 would be cut off. This would result in negative peak clipping below −50 volts amplitude. Crystal diode CR6 would be cut off with negative input signals in excess of −50 volts amplitude because more current would flow through R2 causing a higher voltage drop across R2. This higher voltage drop across R2 makes point B and the plate of CR6 more negative than the cathode of CR6. The voltage drop across the output load resistor cannot be made large enough to cause CR6 to conduct. Therefore, negative input signals in excess of −50 volts amplitude would bias CR6 below cutoff. As a result, negative voltage limiting takes place across the output load resistor because the current path is from the −250-volt plate supply through terminal 4, R1, CR5, terminal 3, the output load resistor, and to ground. The output signals through terminal 3 are thus limited to a maximum positive and negative voltage of ±50 volts amplitude. Input signals in excess of ±50 volts amplitude result in positive and negative peak clipping at ±50 volts of the input waveform.

(7) In summary, the electronic gate is a switching device controlled by gate control pulses applied at terminals 5 and 7. When the gate control pulse is positive at terminal 7 and negative at terminal 5, the electronic gate acts as an open switch preventing any input signal applied at terminals 1 and 2 from passing through the gate to terminal 3. When the gate control pulse is negative at terminal 7 and positive at terminal 5, the electronic gate acts as a closed switch permitting input signals no greater than ±50 volts amplitude to pass through the gate.

37. PPI DC Amplifier 9005503

a. General. Two PPI dc amplifiers are used in the PPI to amplify the relatively low level positioning voltages to the level necessary for driving the deflection plates of the cathode-ray tube in the PPI. Since both PPI dc amplifiers are identical, only the north-south amplifier with north-south (Y) signals applied is discussed in *b* (1) through (3) below.

b. Detailed Theory. The PPI dc amplifier (fig. 7, TM 9–1430–257–20) is a 3-stage feedback amplifier. It consists of two conventional voltage amplifiers V1A and V1B, and high-voltage phase splitting amplifier V2. Degenerative feedback is utilized to develop a high degree of linearity. Inputs to the PPI dc amplifier are the sawtooth sweep pulses from the sweep generator during one period of time or the Y analog dc voltage at connector P1 1 and the Y symbol signal from the PPI marker generator at connector P1–10. The inputs are switched 500 times per second by electronic gates Z1 through Z4. Outputs from the dc amplifier are amplified sawtooth sweep pulses or the Y symbol signal alternating about the Y analog dc voltage. Since the dc amplifier operates in the same manner for both inputs, only the sawtooth sweep pulse input is discussed in (1) through (3) below.

(1) *Voltage amplifiers V1A and V1B.* The sawtooth sweep pulse at P1–1 is applied through gain adjust variable resistor R1 and resistor R30 to the grid of voltage amplifier V1A. The setting of R1 determines the amplitude of the sawtooth sweep pulse input. Bias voltage for V1A is determined by the voltage divider consisting of dc balance variable resistor R4 and resistors R3, R30, and R1 connected between the −87-volt supply at connector P1–4 and ground. The setting

CONFIDENTIAL

of R4 determines the starting or reference level of the sawtooth sweep pulse input. Since the starting level is the point from which each sweep on the CRT begins, R4 is adjusted to position the starting point of the sweep trace at the center of the CRT screen. Cathode bypass capacitor C2 increases the response above 800 kc by shunting cathode resistor R6. This counteracts the tendency to decrease in response above 800 kc due to stray capacitance in the plate circuit of V1A. Resistor R5 is the plate load resistor for V1A. Voltage amplifier V1A has midband gain of approximately 20 db. The output from the plate of V1A is coupled through resistor R7, zero-set variable resistor R29, and capacitor C3 to the grid of voltage amplifier V1B. Zero-set variable resistor R29 varies dc voltages throughout the PPI dc amplifier in order to set the control grid of V1A to zero and thus maintain a low-impedance summing point. For example, when R29 is turned clockwise, the control grid voltage of V1B is biased more positive. This more positive grid voltage causes the plate voltage of V1B to decrease and the plate voltage of V2 (PU1) to increase. The increase in plate voltage of V2 is fed back to the grid of V1A through R14, R13, R12, and R2, causing the grid voltage of V1A to increase. Thus, R29 can be used to adjust the grid voltage of V1A. Proper adjustment of R29 produces zero output of the dc amplifier for zero input. Capacitor C3 increases the response above 16 kc by shunting R7 and part of R29. This counteracts the tendency to decrease in response above 16 kc due to the input capacitance of V1B. Resistor R8 and part of R29 serve as the grid load resistor. Resistor R9 is the plate load resistor for V1B. Cathode bypass capacitor C4 increases the response above 1,600 kc by shunting cathode resistor R10. This counteracts the tendency to decrease in response

above 1,600 kc due to stray capacitance in the plate circuit of V1B. Voltage amplifier V1B has a midband gain of approximately 20 db.

(2) *Phase splitting amplifier V2.* Phase splitting amplifier V2 provides a push-pull output from a single input. The push-pull outputs are equal in amplitude and opposite in polarity. The output from the plate of V1B is coupled through resistor R15 in parallel with capacitor C8 and resistor R20 to the control grid of V2 (PU1). Capacitor C8 increases the response above 16 kc by shunting R15. This counteracts the tendency to decrease in response above 16 kc due to the input capacitance of V2 (PU1). Resistors R16 and R27 are the grid and the plate resistors of V2 (PU1), respectively. The output from the plate of V2 (PU1) is coupled through resistors R17, R18, R19, R32, R33, and R21 to the control grid of V2 (PU2). Capacitors C9, C10, and C11 increase the response above 50 kc by shunting R17, R18, and R19. This counteracts the tendency to decrease in response due to stray capacitance in the plate circuit of V2 (PU1) and the input capacitance of V2 (PU2). Resistors R22 and R26 are the control grid and plate resistors of V2 (PU2), respectively. Resistor R28 is the screen grid resistor for V2; capacitor C15 is the screen grid bypass capacitor. The output from the plate of V2 (PU2) is fed back to the control grid of V2 (PU2) through resistors R25, R24, R23, R32, R33, and R21. This degenerative feedback reduces the gain of V2 (PU2) to approximately unity. Capacitors C12, C13, and C14 increase the degenerative feedback above 50 kc by shunting R23, R24, and R25. This counteracts the tendency to decrease in feedback due to stray capacitance in the plate circuit and the input capacitance of V2 (PU2). Thus, V2 serves as a phase splitting amplifier, since the output at the plate of V2 (PU2) is equal in amplitude

CONFIDENTIAL

and opposite in phase to the output at the plate of V2 (PU1). The sawtooth sweep voltages at the plates of V2 are applied to connectors P2 and P3. These sawtooth sweep voltages drive a pair of deflection plates in the CRT of the PPI. The +1,550-volt plate supply for V2 is received at connector J1.

(3) Feedback. Resistors R14, R13, R12, and R2 provide a degenerative feedback path between the output of V2 (PU1) and the grid of V1A. Capacitors C5, C6, and C7 increase the degenerative feedback above 80 kc by shunting R14, R13, and R12, thus avoiding parasitic oscillators in the PPI dc amplifier. Resistors R11, R12, R13, and R14 form a voltage divider in the feedback path. An additional degenerative feedback path is provided from the plate circuits of V2 through crystal diodes CR2 and CR3 to the grid of V1A.

(4) Symbol positioning. The X and Y symbol signals from the PPI marker generator are applied to P1-10 on the E-W and N-S PPI dc amplifiers, respectively. The X and Y analog dc voltages are applied to P1-1 on the E-W and N-S PPI dc amplifiers, respectively. Electronic gates Z1 through Z4 gate these inputs so that first the sawtooth sweep pulse is applied to the PPI dc amplifiers, then the X and Y symbol signals and X and Y analog dc voltages are applied to the PPI dc amplifiers. The symbol signal is either 3 cycles of a 12.5-kc sine wave or 3 cycles of a full-wave rectified 12.5-kc sine wave. The X or Y symbol signal at P1-10 is coupled through resistor R31

and capacitor C16 in parallel to the grid of V1A. Capacitor C16 increases the response above 50 kc by shunting R31. This counteracts the tendency to decrease in response above 50 kc due to the input capacitance of V1A. The X or Y symbol signal at the grid of V1A alternates about the X or Y analog dc voltage at the grid of V1A. The output of the E-W PPI dc amplifier is 3 cycles of a 12.5-kc sine wave alternating about the X analog dc voltage. The output of the N-S PPI dc amplifier is either 3 cycles of a 12.5-kc sine wave or 3 cycles of a 12.5-kc full-wave rectified sine wave alternating about the Y analog dc voltage. The X and Y analog dc voltages determine the position at which the symbols are painted on the CRT screen.

(5) Expansion circuit. When EXPANSION switch S3 (fig. 25) on the PPI is set to ON, expansion relay K1 on the PPI dc amplifier is energized. This closes contacts 1 and 6 of K1, shorting resistor R30 and doubling the amplitude of the input signal to the grid of V1A. That is, when R30 is shorted, the portion of the input signal formerly dropped across R30 now appears as an added portion of the grid signal. Doubling the amplitude of the input signal to V1A doubles the amplitude of the output voltages of the PPI dc amplifier and therefore doubles the sweep length on the PPI. An offset voltage is developed by the voltage divider consisting of resistor R18, EXPANSION POSITION variable resistor R19 in parallel with expansion adjust vari-
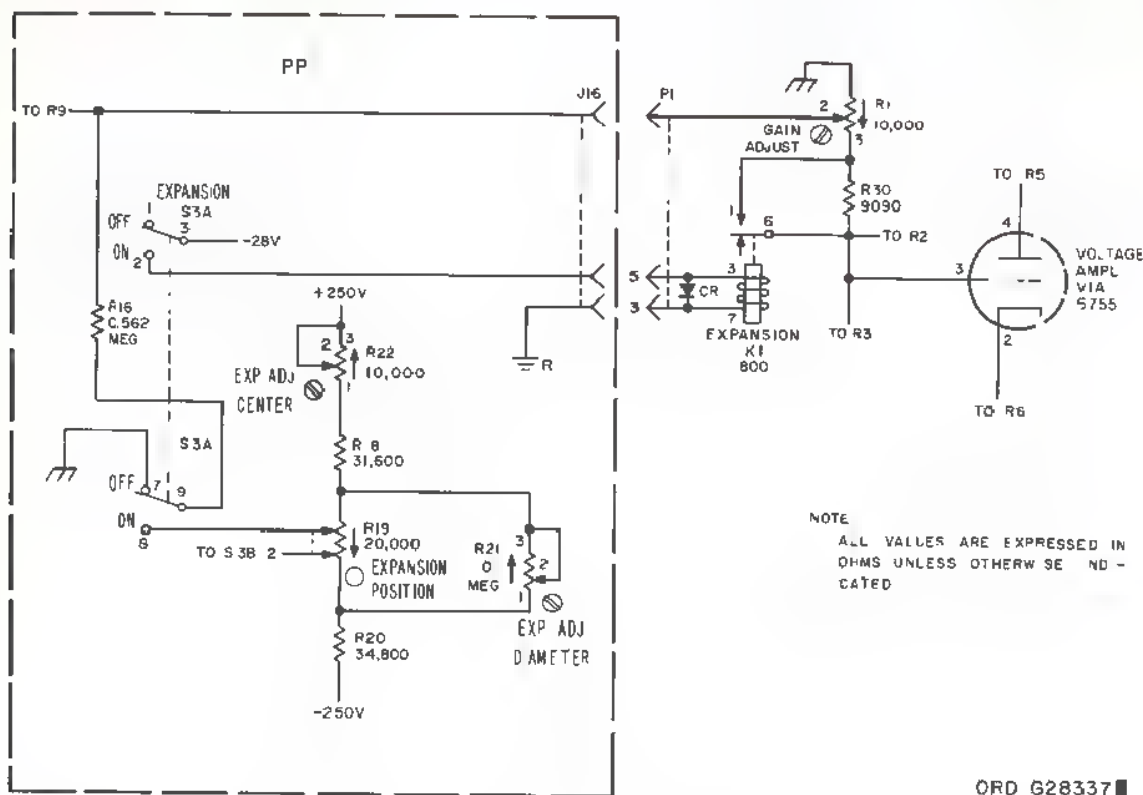
Figure 25. (U) PPI dc amplifier – expansion circuit – partial schematic diagram.

able resistor R21, and resistor R20 connected between the +250- and –250-volt supplies. The offset voltage is applied from the brush arm of R19 through EXPANSION switch S3A and resistor R16 and R1 to the grid of V1A. This offset voltage establishes a new reference level for input signals, resulting in a new starting point for sweep traces on the CRT. The expanded presentation on the PPI is discussed in greater detail in paragraph 33. Crystal diode CR1 provides protection from arcing for the contacts of S3 on the PPI.

38. (CMHA) PPI Video Amplifier 9142869

a. General. The PPI video amplifier produces pulses, and amplifies the acquisition video and marks. The sweep gate pulses generated in the end of sweep pulses, sweep gate pulses, unblanking control channel determine the time of sweep on the cathode-ray tube screen of the PPI. Therefore, the sweep gate pulses determine the range represented by the sweep on the CRT screen. Two unblanking pulses are provided for unblanking the CRT. One unblanking pulse is generated from a gate produced in the control channel and is also a pedestal for the acquisition video and marks applied to the CRT. The other is a sym-

bols unblanking pulse input from the PPI marker generator.

b. Detailed Theory. The PPI video amplifier (fig. 8, TM 9-1430-257-20) contains two channels; the control channel and the video channel. The control channel consists of monostable multivibrator V1A and V1B, cathode follower V2A, and monostable multivibrator V3A and V3B. The video channel consists of video gate V4B, video amplifier V4A, symbol cathode follower V2B, and video mixer V5. The control channel generates sweep gate pulses and end of sweep pulses, and the video channel amplifies the symbols unblanking pulse and acquisition video and marks applied to the CRT.

(1) Control channel. The input to the control channel is the sync pulse from the acquisition-track synchronizer. Outputs of the control channel are sweep gate pulses to the sweep generator, end of sweep pulses to the PPI marker generator, and end of sweep pulses to the video channel, as described in (2) below.

(a) Monostable multivibrator V1A and V1B.

1. Monostable multivibrator V1A and V1B generates sweep gate pulses. Prior to application of signals, V1A is cut off and V1B is conducting. Because of the +250 volts applied through resistor R17 and range adjust variable resistor R18 to the grid of V1B, grid current flows, biasing V1B at a positive dc potential. Cathode follower V2A is conducting heavily at this time. Since V2A has only a small resistance when conducting, the cathode is approximately +250 volts.

Thus, capacitor C9 (or C9 and C10 or C9 and C11, depending on the position of switch S1) maintains only a small charge. With V1B conducting, a positive voltage developed across common cathode resistor R14 keeps V1A cut off. This is the quiescent state of the multivibrator.

2. Positive sync pulses trigger the multivibrator into operation. A positive sync pulse at connector J3, coupled through crystal diode CR7 to the grid of V1A, drives V1A into conduction. This results in a negative-going pulse at the plate of V1A. Crystal CR7 acts as a clipper for the sync pulse. Positive signals allow CR7 to conduct and are therefore passed through CR7 and developed across grid load resistor R3. Negative signals drive CR7 into cutoff, resulting in no signal at the grid of V1A. When V1A conducts, the voltage across R14 increases. At the same time, the negative pulse at the plate of V1A is coupled through V2A and capacitor C9 (or C9 and C10 or C9 and C11) to the grid of V1B. This negative-going pulse at the grid and the positive voltage at the cathode causes a sharp cutoff of V1B, resulting in a positive-going pulse at the plate. The time duration of the pulses of V1A and V1B depends on which capacitors (C9, C9 and C10, or C9 and C11) are in the circuit. The position of S1 determines

which capacitor is in the circuit. When C9 is in the circuit, a 384±18-microsecond pulse is developed. Capacitor C9 and C10 in the circuit increases the time to 768±36 microseconds, and C9 and C11 to 1,600±78 microseconds. The length of the pulses represents 60,000, 120,000, and 250,000 yards in range. Variable resistor R18 is a fine adjustment for the pulse length. The remainder of the detailed theory is discussed with S1 in the 60,000-yard position, which places C9 in the circuit.

(b) Cathode follower V2A. Cathode follower V2A develops a sweep gate pulse for gating the video channel and the PPI marker generator. The negative 395±10 - microsecond pulse at the plate of V1A is applied directly to the grid of V2A. This results in a negative 395±10-microsecond pulse at the cathode of V2A which is applied directly to connector J4. This pulse output is the end of sweep pulse for triggering the PPI marker generator to mark the end of the sweep period. Resistors R9 and R8 form a voltage divider in the cathode circuit of V2A. Because of the voltage divider, the negative end of sweep pulse is reduced in amplitude for coupling to video gate V4B in the video channel. The amplitude of the end of sweep pulse coupled to V4B is approximately 25 percent of the end of sweep pulse developed at the cathode of V2A. This pulse is developed across R9 and coupled through capacitor C6 and resistors R11 and R15 to the grid of V4B. This circuit is discussed further in (2)(a) below. Resistor R8, bypassed by capacitor C7, and resistor R9 are also in the charge path for C9. Capacitor C7 presents a low impedance path as compared to R8 for the sharp rise time of the end of sweep pulse across R8. The charge path for C9 is from one plate of C9 through R18, R17, the +250-volt supply, ground, R9, and R8 to the other plate of C9. This occurs when V1B is cut off. At the end of 395±10 microseconds, the charging action of C9 raises the bias of V1B above cutoff and V1B conducts. This drives V1A to cutoff, and the multivibrator is at quiescence. Capacitor C9 discharges quickly through V2A.

(c) Monostable multivibrator V3A. Monostable multivibrator V3A provides one of the sweep gate pulse outputs of the PPI video amplifier. The positive pulse at the plate of V1B is coupled through series dropping resistor R19 in parallel with capacitor C13 to the grid of V3A. Capacitor C13 presents a low impedance path as compared to R19 for the sharp rise and fall time of the pulse to the grid of V3A. This prevents degeneration of the pulse shape. Grid bias for V3A is determined by the voltage divider consisting of resistors R20, R19, and R13 connected between the -250- and +250-volt supplies.

The positive pulse at the grid of V3A is amplified and inverted by V3A, resulting in a negative pulse at the plate. This negative sweep gate pulse is applied directly to connector J2-1. The negative sweep gate pulse is also coupled through resistor R23 to the grid of monostable multivibrator V3B.

(d) Monostable multivibrator V3B. Monostable multivibrator V3B provides the other sweep gate pulse output of the PPI video amplifier. Bias voltage for V3B is determined by the voltage divider consisting of resistor R26, the series-parallel combination of resistors R23 and R22 with R25 and R28, resistors R21 and R10 connected between the -250- and filtered +150-volt supplies. The +150-volt supply at connector J2-6 is filtered by resistor R1 and capacitor C1. The parallel combination of capacitor C8 and R10 prevents fluctuations in voltage in the plate circuits of V3 and V4 from affecting the +150-volt supply. Rapid changes are coupled through C8 and bypassed to ground through C1. Slow changes are effectively dampened by R10. Resistor R2 provides positive bias for filaments of V2, preventing arcing between the cathode and filaments. The negative sweep gate pulse at the grid of V3B is amplified and inverted by V3B, resulting in a positive pulse at the plate of V3B. The positive sweep gate pulse is applied directly to connector J2-3. Because of equal

plate load resistors R22 and R28, the common cathode resistor R29, and the plate connecting resistors R23 and R25 between V3A and V3B, the gain of V3B is such that the output pulse is equal and opposite to the output of V3A. Therefore, the sweep gate pulses at J2-1 and 3 are of equal amplitude and opposite polarity. The sweep gate pulses determine the time of the sweep on the PPI.

(e) Switch S1. Switch S1 (fig. 26) provides electromechanical action for the selection of C9, C10, or C11 in the multivibrator V1A and V1B circuit. Switch S1 is operated by a step solenoid connected electrically through S1A to RANGE switch S2 on the front of the PPI.

1. Assume that the RANGE knob is operated to the 120,000 - yard position. Switch S2A, by mechanical connection to the knob, is moved so that -28 volt is applied between contacts 4 and 2. The -28 volts is applied through connector P1-7, J2-7, S1A-12, S1A-5, and contact 2 of the step solenoid to the step solenoid coil. Capacitor C16 charges quickly to -28 volts and the solenoid is operated. When the solenoid operates, contacts 2 and S1A-5 break, removing the -28 volts from the solenoid coil and C16. Switch S1A rotates in a counterclockwise motion and contact 12 is now at a detent on S1A. Switch S1B rotates and places capacitor C10 in the circuit. While

ORD G27561

NOTE:
ALL CAPACITOR VALUES
ARE EXPRESSED IN
MICROMICROFARADS
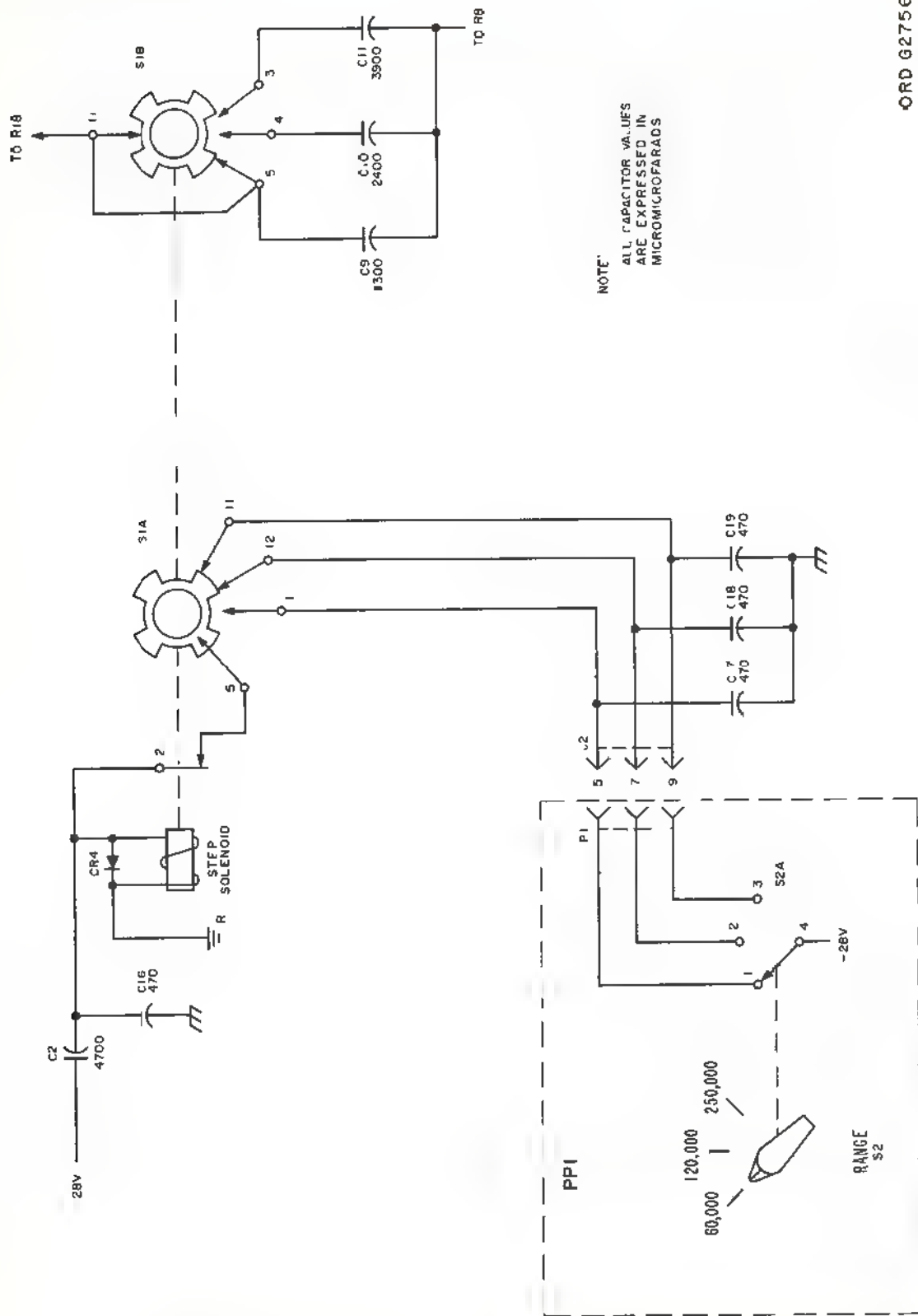
Figure 26. (CMHA) PPI video amplifier – switch S1 – partial schematic diagram.

the solenoid is operated, C16 discharges through the solenoid coil holding contacts 2 and S1A-5 open. The solenoid will release at the end of the discharge of C16. Since contact 12 is at a detent, the -28 volts is not applied again to the solenoid coil. The solenoid and switch remain in this position until the solenoid is operated once again.

2. When S2 is operated to the 250,000-yard position, a similar action takes place and S1A-11 is at a detent on S1A. Similarly, S1B rotates, placing C11 in the multivibrator V1A and V1B circuit. The mechanical connection between the solenoid and switch is a spring and ratchet connection. When the solenoid is operated, the spring and ratchet rotate the switch. A single ball bearing, seated in a hole, locks the switch in each position. When the solenoid is deenergized, the spring is released, preparing the ratchet for the next cycle. The solenoid will cycle until no voltage is applied through S1A-5 and contact 2. In this manner, the selection of C9, C9 and C10, or C9 and C11 is accomplished. Crystal diode CR4 prevents arcing in the solenoid coil. Capacitor C2 prevents transient voltages from causing surges of current through the solenoid coil. Surges of current could cause failure of the solenoid. The solenoid is an integral part of S1. Capacitors C17, C18, and C19 are decoupling capacitors for the -28 volt supply.

(2) Video channel. The video channel (fig. 8, TM 9-1430-257-20) receives three inputs: an end of sweep pulse from the control channel, described in (1) above; acquisition video and marks from the video and mark mixer; and a symbols unblanking pulse from the PPI marker generator. The outputs of the video channel, which are unblanking pulses and amplified acquisition video and marks, are applied to the CRT. Two circuits are provided in the video channel for blanking the CRT. One circuit operates when the acquisition antenna is not rotating and the other when switching from the rotating sweep to the steerable azimuth line on the CRT screen. Blanking the CRT during the switching time prevents blossoming on the screen, which would obscure video presentations.

(a) Video gate V4B. Video gate V4B provides gating action for the video channel. The negative 395±10-microsecond end of sweep pulse from V2A is developed across R9 and coupled through C6 and series dropping resistors R11 and R15 to the grid of V4B. Crystal diode CR2 in parallel with R11 provides a quick discharge path for C6. When the positive-going trailing edge of the negative end of sweep pulse occurs, CR2 conducts. This results in a sharp trailing edge to the pulse. Because the cathode signal follows the grid signal, a negative end of sweep pulse is developed at

the cathode of V4B. The negative pulse is developed across resistor R7 and pedestal adjust variable resistor R33. Both R7 and R33 are common cathode resistors of V4B and video amplifier V4A. The negative end of sweep pulse from V4B increases conduction of V4A.

(b) <u>Video amplifier V4A.</u> Video amplifier V4A amplifies and combines the acquisition video and marks and the sweep gate pulse. The negative end of sweep pulse from V4B is amplified by V4A. The signal at the plate of V4A is a negative pulse. This pulse is a pedestal for the acquisition video and marks signals and an unblanking pulse for the CRT. The setting of R33 determines the amplitude of the pedestal. High level positive acquisition video and marks signals at connector J5 are coupled through capacitor C3 to the grid of V4A. Crystal diode CR3 clips the negative portion of the input acquisition video and marks signals. Negative signals coupled through C3 drive CR3 into conduction, bypassing the signals to ground. This high-level clipping permits almost complete elimination of the negative portion of the signals without loss of weak positive video. Positive signals cut off CR3 and are developed across a voltage divider made up of resistor R37 and R4. The voltage divider reduces the positive signals to a valve suitable for the grid of V4A. The positive acquisition video

and marks signals are amplified and inverted by V4A, resulting in negative signals at the plate. These signals are more negative than the negative unblanking pulse. Inductor L1 in the plate circuit of V4A prevents the high frequency acquisition video and marks signals from entering the +150-volt supply. The negative pedestal and acquisition video and marks signals at the plate of V4A are coupled through capacitor C4 to the control grid of video mixer V5. These signals are developed across resistor R36. Crystal diode CR1 clips the positive portion of the signals. Positive signals drive CR1 into conduction, bypassing the signals to ground. Negative signals cut off CR1 and the signals are developed across R36.

(c) <u>Symbol cathode follower V2B.</u> Symbol cathode follower V2B provides the symbols unblanking pulse for unblanking the CRT. The input signal to V2B is a negative 80-microsecond pulse. This pulse occurs when symbols are to be painted on the PPI. The negative symbols unblanking pulse from the PPI marker generator at connector J6 is coupled to the grid of V2B. Resistor R24 forms part of a voltage divider which determines the amplitude of the unblanking pulse. Since the cathode follows the grid, a negative pulse is developed across resistor R27. This negative symbols unblanking pulse is applied directly to the screen grid of V5.

(d) *Video mixer V5.* Video mixer V5 amplifies and mixes the acquisition video and marks that are applied to the CRT. The negative acquisition video and marks signals combined with the negative pedestal from V4A at the control grid of V5 are amplified and inverted by V5. Positive acquisition video and marks signals atop the positive pedestal at the plate are coupled through capacitor C15 to connector P1. The pedestal unblanks the CRT, allowing the acquisition video and marks to be presented on the CRT. Negative symbols unblanking pulses from V2B applied to the screen grid of V5 result in positive pulses at the plate. These positive pulses unblank the CRT during the symbol painting period. Inductor L2 in the plate circuit of V5 improves the high frequency response of V5 and prevents high frequency acquisition video and marks signals from entering the +250-volt supply.

(e) *Blanking circuits.* When ANTENNA AZIMUTH RPM switch S7 (fig. 27) on the acquisition control-indicator is placed in the OFF position, connector J2–11 of the PPI video amplifier is grounded. This places the plate of crystal diode CR6 at ground potential, which in turn essentially places the grid of V4B at ground. Thus, signals from V2A are essentially grounded, and this in turn keeps the CRT blanked. This blanking action takes place when the acquisition antenna is not rotating. Crystal diode CR8 clips any positive signals at the grid of V4B. Positive signals are bypassed to ground by CR8. Negative signals cut off CR8 and are developed across R12. When switching from the radial sweep to the steerable azimuth line on the CRT, AZIMUTH switch S1 on the target designate control-indicator is operated. This activates steerable-azimuth line relay K1 in the PPI, closing K1 contacts 10 and 4. A sharp positive pulse is coupled through capacitor C3 in the PPI and resistors R32 and R15 in the PPI video amplifier. The charge path is from one plate of C3, the +250-volt supply, ground, resistor R12, and R32 to the other plate of C3. At the same time, capacitor C4 discharges through K1 contacts 2 and 9 and R6. The positive pulse at the grid of V4B, caused by the charging time of C3, results in blanking the CRT for the duration of the charging time of C3. A similar action occurs when K1 is deenergized. Capacitor C4 charges at this time in the same path as C3. Thus, two positive pulses developed across R12 blank the CRT during the switching action. Blanking the CRT prevents blossoming that would obscure the video presentations on the CRT screen.

(f) *Voltage divider.* Resistors R35, R34, R10, and capacitor C8 form a voltage divider between −250 volts and +150 volts.

90.1

38.1 (U). PPI Video Amplifier 9985598

a. General. The theory of PPI video amplifier 9985598 (fig. 8.1, TM 9–1430–257–20) is the same as PPI video amplifier 9142869, discussed in paragraph 38, except for the modifications described in *b* below.

b. Detailed Theory. Resistor R4 is increased in value from 9100 ohms to 1 megohm and resistor R37 is removed completely. The video and marks signals applied at connector J5 are coupled through capacitor C3 to the grid of V4A. Crystal diode CR3 clips the negative portion of the input signals. Positive signals cut off CR3 and are developed across grid resistor R4. The positive signals are amplified and inverted by V4A.

39 (U). PPI Marker Generator 8157989, 9007680

a. General. The function of the PPI marker generator is to produce one of the three possible symbols, designated by the fire unit integration facility (FUIF) equipment, for presentation on the PPI cathode-ray tube screen. The symbol produced, designating the status of the target, will be: a circle around the target video designating a foe; a semicircle around the target video, concave down, designating a friend; or, a defocused spot over the target video designating that another battery is tracking the target. Another function of the PPI marker generator is to produce a symbols unblanking pulse for unblanking the PPI, and two gate control pulses for switching the electronic gates.

b. Detailed Theory. The PPI marker generator (fig. 9, TM 9–1430–257–20) consists of pulse amplifier V1A for reducing noise and amplifying the ADP pulse; bistable multivibrator V2A and V2B for generating a timing pulse pedestal; monostable multivibrator V3A and V3B for generating the timing pulses; start-stop oscillator V4A and V4B for generating 3 cycles of a 12.5-kc sine wave; squaring amplifier V5A and cathode follower V5B for squaring the sine-wave cycles in steps; switching multivibrator V6A and V6B for producing gate control pulses; unblanking amplifier V1B for producing the symbols unblanking pulse; and defocus amplifier V8A and cathode follower V8B for developing the defocusing pulse.

Note. The key letters shown in parentheses in (1) through (8) below refer to figure 28.

    (1) *Pulse amplifier V1A.* The negative ADP pulse (A) at connector J5 (fig. 9, TM 9–1430–257–20) is coupled through capacitor C1 to the cathode of pulse ampli-

Figure 27. (U) PPI video amplifier – blanking circuits – simplified schematic diagram.
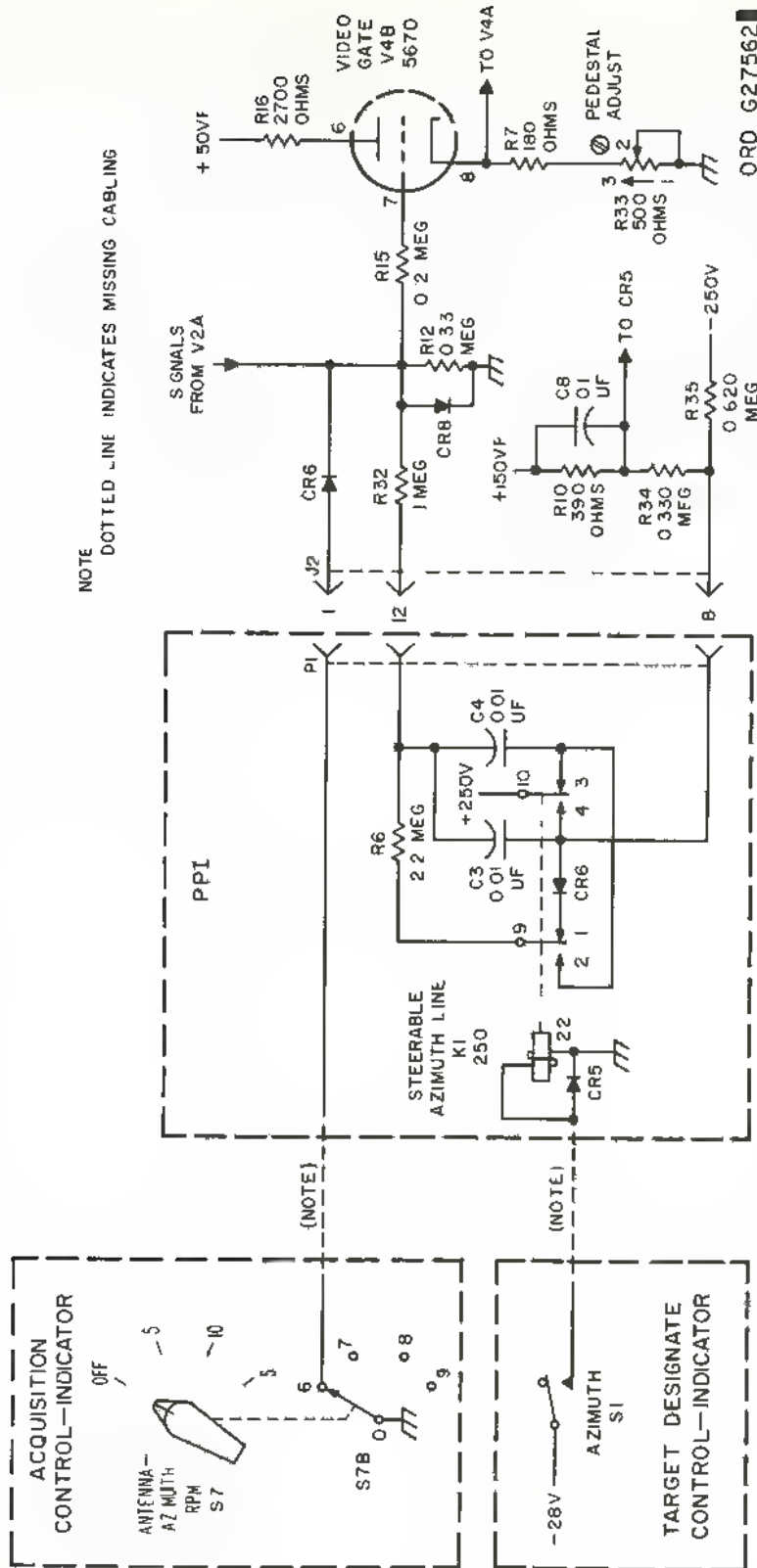
fier V1A. Cathode resistor R2 is unbypassed, reducing the voltage gain of V1A. Grounding the grid of V1A reduces noise and prevents regenerative feedback from being coupled from the plate to the grid by interelectrode capacitance. This feedback could cause oscillations in V1A. The overall result of an unbypassed cathode resistor and of grounding the grid in V1A is faithful reproduction of the ADP pulse and a high signal-to-noise ratio. Since the input to V1A is a negative pulse at the cathode, the output at the plate is an amplified negative pulse. The negative pulse is coupled through capacitor C2 and crystal diode CR1 to the grid of bistable multivibrator V2A. Crystal CR1 clips the input signals to the bias voltage of V2A. Therefore, signals more positive than the grid bias of V2A are blocked. Signals more negative than the bias of V2A are passed. These negative signals are developed across resistor R4.

(2) *Bistable multivibrator V2A and V2B.*

(a) Bistable multivibrator V2A and V2B has two stable conditions; V2A conducting and V2B cut off, and V2A cut off and V2B conducting. Two triggers are required to complete 1 cycle of operation. When power is initially applied to the marker generator, either condition (conduction or cutoff) of V2A and V2B may exist. After the monostable multivibrator, described in (3) below, has completed the first cycle of operation, normal operation of V2A and V2B is effected. During normal operation, prior to application of the negative pulse from V1A, V2A is conducting and V2B is cut off. Bias for V2A is developed by the voltage divider consisting of resistors R7, R10, and R11 connected between the −250- and +150-volt supplies. Bias for V2B is developed by the voltage divider consisting of resistors R8, R6, and R5 connected between the −250-

and +150-volt supplies. Resistors R4 and R16 in the grid circuit of V2A and V2B develop grid signals.

(b) When the negative pulse at the plate of V1A is coupled through C2 and CR1, V2A cuts off, producing a positive pulse at the plate. This positive pulse is coupled through capacitor C3 in parallel with R6 to the grid of V2B. The positive pulse drives V2B into conduction. Capacitor C3 presents a low impedance path as compared to R6 for the sharp rise time of the pulse. This causes rapid switching of V2B from cutoff to conduction. The multivibrator will remain in this state, V2A cut off and V2B conducting, until a negative pulse from monostable multivibrator V3B, described in (3) below, appears at the grid of V2B.

(c) The positive pulse at the plate of V2A is also coupled through resistor R9, pedestal adjust variable resistor R12, and capacitor C5 in parallel with resistor R17 to the grid of monostable multivibrator V3A. Capacitor C5 presents a low impedance path as compared to R16 for the sharp rise time of the pulse. Thus, the sharp rise time of the pulse is maintained at the grid of V3A. The positive pulse forms a pedestal (B) for a second input to the grid of V3A. Variable resistor R12 is adjusted to raise the grid voltage of V3A just below the cutoff voltage when the pedestal is applied to the grid of V3A.

(3) *Monostable multivibrator V3A and V3B.*

(a) At quiescence, prior to the application of the positive pulse from V2A (fig. 9, TM 9-1430-257-20), V3A is cut off and V3B is conducting. However, two inputs are required to trigger V3A into conduction. The pulse from V2A alone is not sufficient amplitude to drive V3A into conduction. Bias for V3A is developed by the voltage divider consisting of resistors R18, R12, R9, and R5 connected between the −250- and
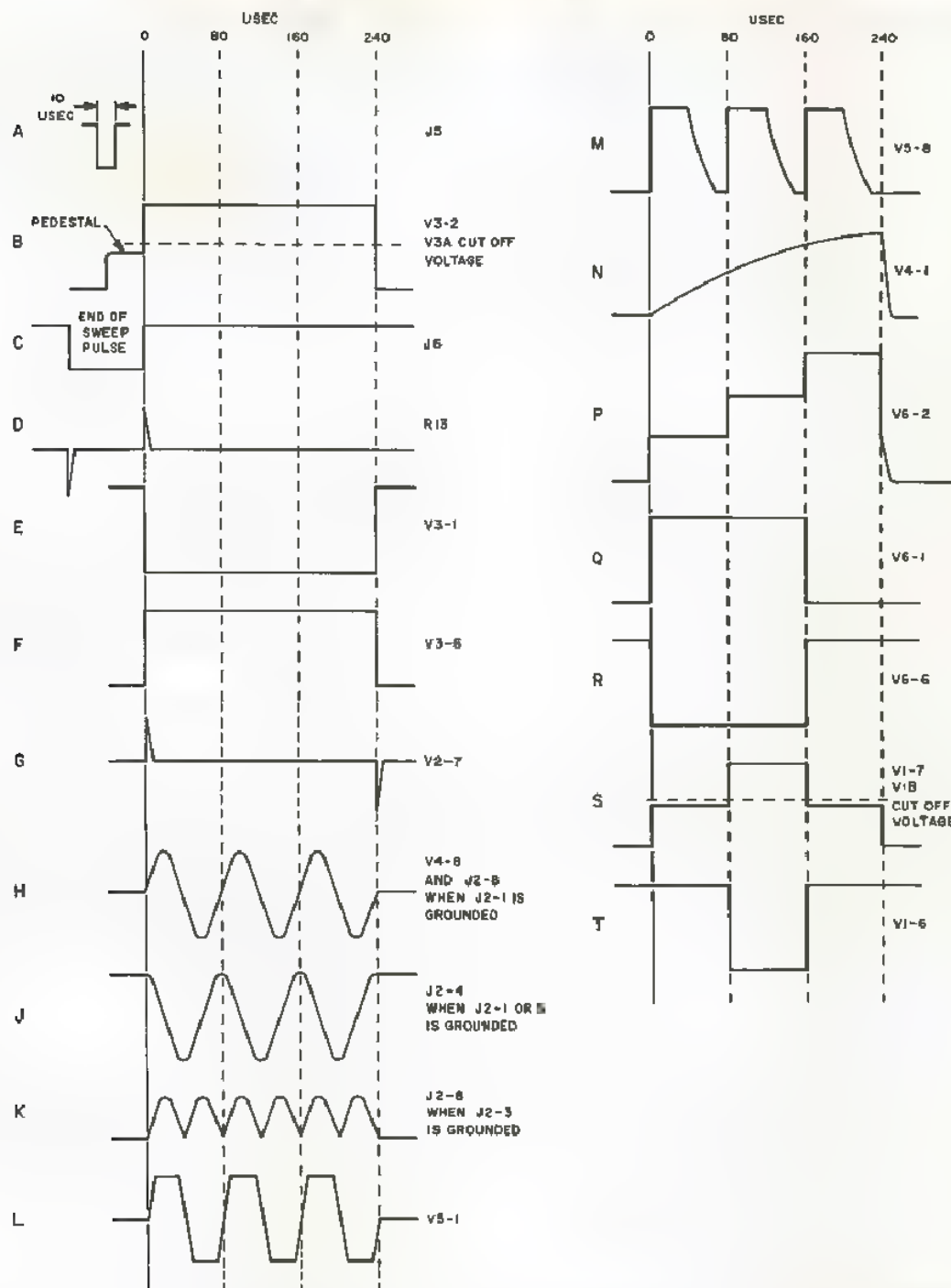
Figure 28 (U) PPI marker generator—waveforms.

RA PD 468137

CONFIDENTIAL

+150-volt supplies. Since the cathode of V3B is connected through resistor R20 to the −250-volt supply and the plate through resistor R22 to the +250-volt supply, V3B will conduct with no signal applied. The positive pulse from V2A forms a pedestal for the input signal to V3A.

(*b*) When a negative end of sweep pulse (C) is applied at connector J6 (fig. 9, TM 9–1430–257 20), the leading and trailing edges of the end of the sweep pulse are differentiated by capacitor C6 and resistor R13. The negative-going leading edge is differentiated into a negative pip (D), and the positive-going trailing edge into a positive pip. The negative pip is coupled through capacitor C7 (fig. 9, TM 9–1430–257–20) and resistor R14 to the grid of V3A. Since V3A is cut off, the negative pip has no effect on the circuit. The positive pip is coupled through C7 and R14 to the grid of V3A. This positive pip atop the pedestal from V2A causes V3A to conduct, resulting in a negative pulse (E) at the plate of V3A (fig. 9, TM 9–1430–257–20). The negative pulse is coupled through capacitor C10 to the grid of V3B, driving V3B to cutoff. At the end of 240 microseconds, V3B returns to conduction because of the discharging of C10 through resistor R21. The discharge path is from one plate of C10 through R21, ground, the −250-volt supply, R20, and V3A to the other plate of C10. The resultant negative-going trailing edge of the positive 240-microsecond pulse (F) at the plate of V3B is coupled through capacitor C9 (fig. 9, TM 9–1430–257–20) to the grid of V3A. This drives V3A to cutoff, returning V3A and V3B to quiescence.

(*c*) The positive 240-microsecond pulse at the plate of V3B is differentiated by capacitor C8 and resistor R15 and R16 at the grid of V2B. Since V2B is con-

ducting, the positive pip (G) (leading edge of pulse) has no effect on the circuit. The negative pip (trailing edge of pulse) drives V2B to cutoff, which in turn drives V2A into conduction. Thus, V2A and V2B are returned to quiescence. The negative 240-microsecond pulse at the plate of V3A is coupled through crystal diode CR2 and capacitor C11 to the grid of V4A. Crystal diode CR2 conducts when the plate voltage of V3A drops below +150 volts. Therefore, the amplitude of the negative pulse coupled to the grid of V4A is clamped at +150 volts by CR2.

(4) *Start-stop oscillator V4A and V4B.*

(*a*) Prior to the application of the negative pulse from V3A, V4A is conducting. Current flows through the tank circuit composed of inductor L1 and capacitors C12 through C15. The capacitors charge to the potential developed across L1 and retain the charge. Thus, conduction of V4A prevents the tank circuit from oscillating. At this same time, V4B is conducting because of the negative voltage at the cathode. The negative voltage is developed across the voltage divider consisting of resistors R28, R73, oscillator level variable resistor R27, and L1–3 and 2 connected between the −250-volt supply and ground.

(*b*) The negative pulse from V3A drives V4A to cutoff for 240 microseconds, cutting off current flow through L1. Capacitors C12 through C15 discharge through L1, starting oscillations in the tank circuit. The output signal of the tank circuit is coupled through capacitor C17 to the grid of V4B. This signal is developed across resistor R26. When the output of the tank circuit is positive, the grid of V4B is positive, causing increased conduction through L1–2 and 3, R27, and V4B. In this manner, V4B produces regenerative

94

feedback to the tank circuit to maintain oscillations. The strapping connection of C12, C13, and C14 in parallel with C15 is connected to make the tank circuit oscillate at exactly 12.5 kilocycles. This is a factory adjustment and will not be changed in the field. Since the tank circuit oscillates for 240 microseconds, three complete sine waves (H) are produced at the cathode of V4B. The setting of R27 (fig. 9, TM 9–1430–257 20) determines both the amplitude and the reference level of the sine waves.

(c) The sine waves at the cathode of V4B are applied through R73 to the primaries of transformers T1, T2, and T3. The operation of T1, T2, and T3 depends on the grounding of connector J2–1, 3, or 5. When J2–1 is grounded, output signals are developed by T1 and T2, producing a circle on the PPI. When J2–3 is grounded, outputs are developed by T1 and T3, producing a semicircle on the PPI. When J2–5 is grounded, no output is developed by T1, T2, or T3. This is discussed further in (9) below. The grounding of J2 1, 3, or 5 is accomplished in the FUIF equipment during operation or by TEST switch S1 on the PPI test panel during checks and adjustments.

1. In the secondary of T1, capacitor C18 and resistor R29 form an RC network to shift the output signal 90° with respect to the input signal. The signal developed across T1–4 and 3 is 180° out of phase with respect to the signal developed across T1–4 and 5. Consider now the separate branches. Since the branch through resistors R29, R52, and X amplitude variable resistor R30 is resistive, the signal is in phase with the signal across T1–4 and 3. In the branch through C18, R52, and R30, there are two components of the signal; the signal developed by the reactance of C18 and the signal developed by the resistance of R52 and R30. The signal from the branch of T1–4 and 5 and the branch of T1–4 and 3 results in a signal with a phase shift of 90°. The output of T1 is coupled through R52 and R30 to connector J2 4. This X symbol signal (J) is three sine waves shifted 90° with respect to the input sine waves (H). The setting of variable resistor R30 (fig. 9, TM 9–1430–257–20) determines the amplitude of the X symbol signal at J2–4.

2. With J2–1 grounded, the output signal of T2 is developed across resistor R32 and coupled through resistors R31, R53, and Y amplitude variable resistor R74 to J2–8. The setting of R74 determines the amplitude of the Y symbol signal at J2–8. The Y symbol signal from the secondary of T2 is three sine waves (H) in phase with the input signals. In the secondary of T3 (fig. 9, TM 9–1430–257–20), crystal diodes CR5 and CR6 and resistor R32 form a full-wave rectifier. With J2–3 grounded, the Y symbol signal output (K) of T3 is developed across R32 and coupled through R31, R53, and R74 to J2–8.

(5) *Squaring amplifier V5A.* The output (H) of V4B is also applied through resistor R33 (fig. 9, TM 9–1430–257–20) to the grid of squaring amplifier V5A. Squaring amplifier V5A is driven to saturation and cutoff by the sine waves. The output of V5A (L) is three squared sine waves. These square waves are coupled through capacitor C19 (fig. 9, TM 9 1430–257–20) to the grid of cathode follower V5B. During the positive half-cycle of the squared sine wave, V5B conducts. During the negative half-cycle of the squared sine wave, V5B is cut off. The resultant waveform (M) at the cathode of V5B is three positive 80-microsecond pulses. The pulses have a steep lead-

CONFIDENTIAL

ing edge and a sloping trailing edge. The sloping trailing edge is caused by the discharge of capacitor C21 (fig. 9, TM 9–1420–257–20) through resistor R37. However, at this time the plate signal of V4A is being applied to the cathode through resistors R39 and R38. The signal (N) at the plate of V4A is a rising voltage for 240 microseconds. Although V4A (fig. 9, TM 9–1430–257–20) cuts off quickly when the negative pulse from V3A is coupled to the grid of V4A, the plate voltage will rise exponentially. The charging action of capacitor C16 in the plate circuit of V4A causes the exponential rise. The rising voltage from V4A with the three positive pulses from V5B form a three-step pulse (P). Each step is 80 microseconds wide. The three-step pulse is coupled through capacitor C23 (fig. 9, TM 9–1430–257 20) to the grid of V6A. The waveform is also coupled through resistor R38, capacitor C22, and capacitor C30 and resistor R41 in parallel to the grid of V1B. Capacitor C30 presents a low impedance path as compared to R41 for the sharp rise times of the step pulse.

(6) *Switching multivibrator V6A and V6B.*

  (a) Prior to application of the step pulse from V5B and the positive pulse from V3B, switching multivibrator V6A is conducting and switching multivibrator V6B is cut off. Bias for V6B is developed by the voltage divider consisting of resistors R46 and R54 connected between the -250-volt supply and ground. Bias is applied to the grid of V6A through resistor R40 and gate pulse adjust variable resistor R49.

  (b) Inputs to V6A and V6B are received simultaneously. The positive 240-microsecond pulse at the plate of V3B is coupled through capacitor C27 to the grid of V6B; the three-step pulse is coupled through C23 to the grid of V6A. The positive pulse at the grid of V6B drives V6B into conduction. A negative-going pulse (R) is developed at the plate. This pulse is coupled through crystal diode CR7 and resistor R42 in parallel and capacitor C24 to the grid of V6A. The negative pulse is of sufficient amplitude to cut off V6A. Multivibrator V6A remains cut off until the step pulse at the grid is of sufficient amplitude to override the negative pulse from V6B. Variable resistor R49 is adjusted to cause V6A to conduct upon application of the third step of the step pulse (P). This results in a positive pulse (Q) for 160 microseconds at the plate of V6A.

  (c) The negative going trailing edge of the positive pulse (Q) at the plate of V6A coupled through capacitor C25 (fig. 9, TM 9–1430–257–20) is of sufficient amplitude to drive V6B to cutoff. This action causes a rise in the plate voltage of V6B and terminates the negative 160-microsecond pulse (R). Crystal CR7 (fig. 9, TM 9 1430–257 20) will conduct during the negative pulse at the plate of V6B, allowing the pulse to be coupled through C24 to the grid of V6A. When the positive step pulse at the grid of V6A overrides the negative pulse from the plate of V6B, CR7 cuts off because the plate voltage of V6B is more positive than the step pulse. The large value of R42 and nonconduction of CR7 isolate the plate of V6B from the positive step pulse. This prevents V6B from conducting upon application of the third step of the step pulse.

(7) *Cathode followers V7A and V7B.* The positive 160-microsecond pulse from V6A is applied through resistor R43 to the grid of cathode follower V7B. This results in a positive 160-microsecond gate control pulse at the cathode of V7B. Grid bias for V7B is the voltage drop across resistor R51 which is part of a voltage divider consisting of resistors R51, R43, and R44 connected between

CONFIDENTIAL

the —250- and +250-volt supplies. The negative 160-microsecond pulse from V6B is applied through resistor R45 to the grid of cathode follower V7A. This results in a negative 160-microsecond gate control pulse at the cathode of V7A. Grid bias for V7A is the voltage drop across resistor R50 which is part of a voltage divider consisting of resistors R50, R45, and R47 connected between the —250- and +250-volt supplies. The negative gate control pulse is developed across cathode resistors R57 and R56 and applied directly to connector J2–11. The positive gate control pulse at the cathode of V7B is developed across resistors R58 and R56 and applied directly to J2–12. The positive pulse is also coupled through capacitor C28 and resistor R59 to the grid of V1B.

(8) *Unblanking amplifier V1B.* Prior to application of the step pulse from V5B and the positive pulse from V7B, unblanking amplifier V1B is cut off. Bias for V1B is developed across the voltage divider consisting of resistor R72, symbols unblanking pulse adjust variable resistor R71, and resistor R70 connected between the 25-volt supply and ground. The inputs to V1B are the positive 160-microsecond pulse (Q) and the three-step pulse (P). The resultant waveform (S) at the grid of V1B is two rising step voltages for 160 microseconds and a lower step voltage for 80 microseconds followed by a negative return to quiescence at the end of the 240-microsecond period. Variable resistor R71 (fig. 9, TM 9–1430–257–20) is adjusted to cause V1B to conduct upon application of the second step only. Crystal diode CR8 clamps the positive pulse from V7B to the bias voltage determined by the setting of R71. The output waveform (T) at the plate of V1B is a negative 80-microsecond symbols unblanking pulse. This pulse occurs between 80 and 160 microseconds of the 240-microsecond operating period of the marker generator. The negative 80-microsecond symbols unblanking

pulse is coupled through capacitor C29 (fig. 9, TM 9–1430–257–20) to connector J4 and through series dropping resistor R64 and resistor R65 to the grid of V8A. Resistor R65 limits the flow of grid current in V8A.

(9) *Defocus amplifier V8A and cathode follower V8B.* Bias for defocus amplifier V8A is developed by the voltage divider consisting of resistors R62, R61, and R60 connected between the —250- and +150-volt supplies The bias also depends on the grounding of J2–5. Normal operation occurs when J2–5 is not grounded and V8A is conducting heavily. At this time, a negative pulse from V1B fails to overcome the bias voltage and V8A continues conducting. When J2–5 is grounded, the bias voltage is reduced considerably, reducing conduction in V8A. A negative 80-microsecond pulse from V1B at this time drives V8A to cutoff. This results in a positive pulse at the plate of V8A. The positive pulse is applied through resistor R67 to the grid of cathode follower V8B. Grid bias for V8B is the voltage drop across resistor R68 which is part of the voltage divider consisting of resistors R68, R67, and R66 connected between the —250- and +250-volt supplies. The cathode of V8B follows the grid and a positive pulse is applied directly to connector J3. This pulse is developed across the primary of transformer T1 in the PPI to produce a defocused spot on the PPI. Transformer T1 is connected externally to J3.

c. *PPI Marker Generator 9007690.* PPI marker generator 9007680 (fig. 9, TM 9–1430–257–20) is similar to PPI marker generator 8157989, discussed in *a* and *b* above. Detailed theory of the two units remains the same as in *b* above. Differences between the two units are: V7 is changed from 5814A to 5687; R43 and R45 are removed from the circuit; resistor R75 and capacitor C31 in parallel are added in the cathode circuit of V6; the plate supply of V6 and V7 is changed from +250 to +150 volts; and component values change in the circuitry associated with V6 and V7. In the older model

PPI marker generator 8157989, V7 was operating outside the normal tube limits. This resulted in unstable operation of V7. The unstable operation of V7 caused jitter on the PPI screen. By replacing V7 with the present tube 5687, reducing the plate supply, and changing values of the components, jitter on the PPI screen is reduced.

39.1 (CMHA). PPI 9986454

PPI 9986454 (fig. 72, TM 9 1430–257–20) is the same as PPI 9142868 discussed in paragraph 33 except for the following modifications:

a. The PPI contains 12 subassemblies listed in (1) through (6) below.

    (1) Modulation eliminator 9007951.
    (2) Sweep generator 9143168.
    (3) PPI dc amplifier 9986059 (2).
    (4) PPI video amplifier 9986410.
    (5) PPI marker generator 9143202
    (6) Electronic gate 9007695 (6).

b. Three-position RANGE switch S2 is replaced by a four-position switch with increments of 50,000, 150,000, 250,000, and 350,000 yards. The 350,000-yard display can be selected only in the HIPAR mode of operation. If the 350,000-yard range presentation is selected when LOPAR is being used, an interlocking circuit causes the PPI scope to blank. A ground from connector J1-P shorts the video signal to ground when S2 is in the maximum range position. This operation presents ground to J1-P until RADAR SELECT switch S4 on the acquisition control-indicator is placed to the HIPAR position.

39.2 (U). Modulation Eliminator 9007951

See paragraph 34

39.3 (U). Sweep Generator 9143168

a. General. The sweep generator provides two variable amplitude sawtooth sweep voltages, 90° out of phase with each other. These sawtooth sweep voltages are developed from two independent sine-wave input signals 90° out of phase with each other, representing the N-S and E-W coordinates of the low-power acquisition antenna position. The sawtooth sweep voltages are used to drive the deflection plates of the PPI.

b. Detailed Theory. Sweep generator 9143168 (fig. 73, TM 9–1430–257–20) is the same as sweep generator 8518032, discussed in paragraph 35, except for the following modifications:

    (1) The repetition rate of the sweep gate pulses is 500 pps for LOPAR operation and 400 to 445 pps for HIPAR operation
    (2) Y cathode follower V5A is replaced by Y cathode follower V5B.
    (3) The number of sawtooth sweeps developed by C1 during 1 cycle of input signal to V1A, given in paragraph 35*b*(4)(*c*), applies for LOPAR operation only. The repetition of the sweep gate pulse in HIPAR operation is 400 to 445 pps. The number of sawtooth sweeps developed by C1 is a function of this repetition rate. Assume a repetition rate of 400 pps in HIPAR operation. With an antenna rotation rate of 0.166 rps (10 rpm), C1 provides 2400 variable amplitude output sawtooth sweeps per cycle of antenna rotation. With an antenna rotation rate of 0.111 rps (6.67 rpm), C1 provides 3600 variable amplitude output sawtooth sweeps per cycle of antenna rotation

39.4 (U). Electronic Gate 9007695

Electronic gate 9007695 is identical to electronic gate 8517934 discussed in paragraph 36 except that electronic gate 9007695 is a plug-in unit while electronic gate 8517934 has solder lug terminals.

39.5 (U). PPI DC Amplifier 9986059

The theory of operation of PPI DC amplifier 9986059 (fig. 72 1, TM 9–1430–257–20) is the same as the theory for PPI DC amplifier 9005503 discussed in paragraph 37

39.6 (CMHA). PPI Video Amplifier 9986410

a. General. The PPI video amplifier produces pulses, and amplifies the acquisition video and marks. The sweep pulses generated in the end of the sweep branch and the sweep gate branch of the unblanking control channel determine the time of sweep on the cathode-ray tube screen of the PPI Therefore the sweep gate pulses determine the range represented by the sweep on the CRT screen. Two unblanking pulses are provided for unblanking the CRT. One unblanking pulse is generated from a gate produced in the control channel and provides unblanking for the acquisition video and marks applied to the CRT. The other is a symbols unblanking pulse input from the PPI marker generator.

b. Detailed Theory. The PPI video amplifier (fig. 74, TM 9–1430–257–20) contains two channels: the control channel and the video channel. The control channel consists of monostable multivibrator V1A and V1B, cathode follower V2A, final amplifier V3A, and final amplifier phase inverter V3B. The video channel consists of video gate V4B, video amplifier V4A, blanking amplifier V6A, pulse amplifier V6B, symbol cathode follower V2B, and video mixer V5. The control channel generates sweep gate pulses and end of sweep pulses, and the video channel amplifies the symbols unblanking pulse and acquisition video and marks applied to the CRT.

98.1

(1) *Control channel.* The input to the control channel is the sync pulse from the acquisition-track synchronizer. Outputs of the control channel are sweep gate pulses to the sweep generator, end of sweep pulses to the PPI marker generator, and end of sweep pulses to the video channel, as described in (2) below.

(a) *Monostable multivibrator V1A and V1B*

1. Monostable multivibrator V1A and V1B generates sweep gate pulses. Prior to application of signals, V1A is cut off and V1B is conducting. Because of the +250 volts applied through resistor R17 and range adjust variable resistor R18 to the grid of V1B, grid current flows, biasing V1B at a positive dc potential. Cathode follower V2A is conducting heavily at this time. Since V2A has only a small resistance when conducting, the cathode is at approximately +250 volts. Thus, capacitor C9 (or C9 and C10, C9 and C11, or C9 and C20, depending on the position of switch S1) maintains only a small change. With V1B conducting, a positive voltage developed across common cathode resistor R14 keeps V1A cut off. This is the quiescent state of the multivibrator.

2. Positive sync pulses trigger the multivibrator into operation. A positive sync pulse at connector J3, coupled through crystal diode CR7 to the grid of V1A, drives V1A into conduction. This results in a negative-going pulse at the plate of V1A. Crystal CR7 acts as a clipper for the sync pulse. Positive signals allow CR7 to conduct and are therefore passed through CR7 and developed across grid load resistor R3. Negative signals drive CR7 into cutoff, resulting in no signal at the grid of V1A. When V1A conducts, the voltage across R14 increases. At the same time, the negative pulse at the plate of V1A is coupled through V2A and capacitor C9 (or C9 and C10, C9 and C11, or C9 and C20) to the grid of V1B. This negative-going pulse at the grid and the positive voltage at the cathode cause a sharp cutoff of V1B, resulting in a positive-going pulse at the plate. The time duration of the pulses of V1A and V1B depends on which capacitors (C9, C9 and C10, C9 and C11, or C9 and C20) switch S1 connects in the circuit. When C9 is in the circuit, a pulse of approximately 305 microseconds is developed. Capacitors C9 and C10 in the circuit increase the time to about 915 microseconds. Capacitors C9 and C11 in the circuit increase the time to about 1525 microseconds, and C9 and C20 to about 2135 microseconds. The length of the pulses represents 50,000, 150,000, 250,000 and 350,000 yards in range. Range adjust variable resistor R18 is a fine adjustment for the pulse length. The remainder of the detailed theory is discussed with S1 in the 50,000-yard position, which places C9 in the circuit.

98.2

(b) *Cathode follower V2A.* Cathode follower V2A develops a sweep gate pulse for gating the video channel and the PPI marker generator. The negative 305-microsecond pulse at the plate of V1A is applied directly to the grid of V2A. This results in a negative 305-microsecond pulse at the cathode of V2A which is applied directly to connector J4 This pulse output is the end of sweep pulse for triggering the PPI marker generator to mark the end of the sweep period. Resistors R9 and R8 form a voltage divider in the cathode circuit of V2A. Because of the voltage divider, the negative end of sweep pulse is reduced in amplitude for coupling to video gate V4B in the video channel. The amplitude of the end of sweep pulse coupled to V4B is approximately 25 percent of the end of sweep pulse developed at the cathode of V2A. This pulse is developed across R9 and coupled through capacitor C6 and resistors R11 and R15 to the grid of V4B. This circuit is discussed further in (2) (a) below. Resistor R8, bypassed by capacitor C7, and resistor R9 are also in the charge path for C9. Capacitor C7 presents a low impedance path as compared to R8 for the sharp rise time of the end of sweep pulse across R8. The charge path for C9 is from one plate of C9 through R18, R17, the +250-volt supply, ground, R9, and R8 to the other plate of C9. This occurs when V1B is cut off. At the end of 305 microseconds, the charging action of C9 raises the bias of V1B above cutoff and V1B conducts. This drives V1A to cutoff, and the multivibrator is at quiescence. Capacitor C9 discharges quickly through V2A.

(c) *Final amplifier V3A.* Final amplifier V3A provides one of the sweep gate pulse outputs of the PPI video amplifier. The positive pulse at the plate of V1B is coupled through series dropping resistor R19 in parallel with variable capacitor C13 to the grid of V3A. Capacitor C13 presents a low impedance path, as compared to R19, for the sharp rise and fall time of the pulse to the grid of V3A. This prevents degeneration on the pulse shape. Grid bias for V3A is determined by the voltage divider consisting of resistors R20, R19, and R13 connected between the 250 and +250-volt supplies. The positive pulse at the grid of V3A is amplified and inverted by V3A, resulting in a negative pulse at the plate. This negative sweep gate pulse is applied directly to connector J2 1. The negative sweep gate pulse is also coupled through resistor R23 to the grid of final amplifier phase inverter V3B.

(d) *Final amplifier phase inverter V3B.* Final amplifier phase inverter V3B provides the other sweep gate pulse output of the PPI video amplifier. Bias voltage for V3B is determined by the voltage divider consisting of resistor R26, the series-parallel combination of resistors R23 and R22 with R25 and R28, and resistors R21 and R10 connected between the 250 and filtered +150-volt supplies. The +150-volt supply at connector J2-6 is filtered by resistor R1 and capacitor C1. Capacitor C8 and resistor R10 prevent fluctuations in voltage in the plate circuits of V3 and V4 from affecting the +150-volt supply. Rapid changes are coupled through C8 and C1 to ground. Slow changes are effectively dampened by R10. Resistor R2 provides positive bias for the filaments of V2, preventing arc-

ing between the cathode and the filaments. The negative sweep gate pulse at the grid of V3B is amplified and inverted by V3B, resulting in a positive pulse at the plate of V3B The positive sweep gate pulse is applied directly to connector J2-3. Because of equal plate load resistors R22 and R28 and the common cathode resistor R29, the gain of V3B is such that the output pulse is equal and opposite to the output of V3A. Therefore, the sweep gate pulses at J2 1 and 3 are of equal amplitude and opposite polarity The sweep gate pulses determine the time of the sweep on the PPI.

(e) *Switch S1.* Switch S1 (fig 28.1) provides electromechanical action for the selection of C9, C9 and C10, C9 and C11, or C9 and C20 in the multivibrator V1A and V1B circuit. Switch S1 is operated by a step solenoid connected electrically through S1A to RANGE switch S2 on the front of the PPI.

1. Assume that the RANGE knob is operated to the 150,000-yard position. Switch S2A, by mechanical connection to the knob, is moved so that 28 volts is applied between contacts 6 and 2. The —28 volts is applied through connector P1-7, J2-7, S1A-12, S1A-5, and contact 2 of the step solenoid to the step solenoid coil Capacitor C16 charges quickly to -28 volts and the solenoid is operated. When the solenoid operates, contacts 2 and S1A-5 break, removing the —28 volts from the solenoid coil and C16. Switch S1A rotates in a counterclockwise direction and contact 12 is now at a detent on S1A. Switch S1B rotates and places capacitor C10 in the circuit in parallel with C9, While the solenoid is operated,

C16 discharges through the solenoid coil holding contacts 2 and S1A-5 open. The solenoid will release at the end of the discharge of C16. Since contact 12 is at a detent, the —28 volts is not applied again to the solenoid coil. The solenoid and switch remain in this position until the solenoid is operated again.

2. When S2 is operated to the 250,000-yard position, a similar action takes place and S1A 11 is at a detent on S1A. Similarly, S1B rotates, placing C11 in parallel with C9 in the multivibrator V1A and V1B circuit. When S2 is operated to the 350,000-yard position, S1A-10 is at a detent on S1A. Similarly, S1B rotates, placing C20 in parallel with C9 in the multivibrator circuit. The mechanical connection between the solenoid and switch is a spring and ratchet connection. When the solenoid is operated, the spring and ratchet rotate the switch. A single ball bearing, seated in a hole, locks the switch in each position. When the solenoid is deenergized, the spring is released, preparing the ratchet for the next cycle. The solenoid will cycle until no voltage is applied through S1A-5 and contact 2 In this manner, the selection of C9, C9 and C10, C9 and C11, or C9 and C20 is accomplished. Crystal diode CR4 prevents arcing in the solenoid coil. Capacitor C2 prevents transient voltages from causing surges of current through the solenoid coil. Surges of current could cause failure of the solenoid. The solenoid is an integral part of S1. Capacitors C17, C18, C19, and C23 are decoupling capacitors for the 28-volt supply.

98.4
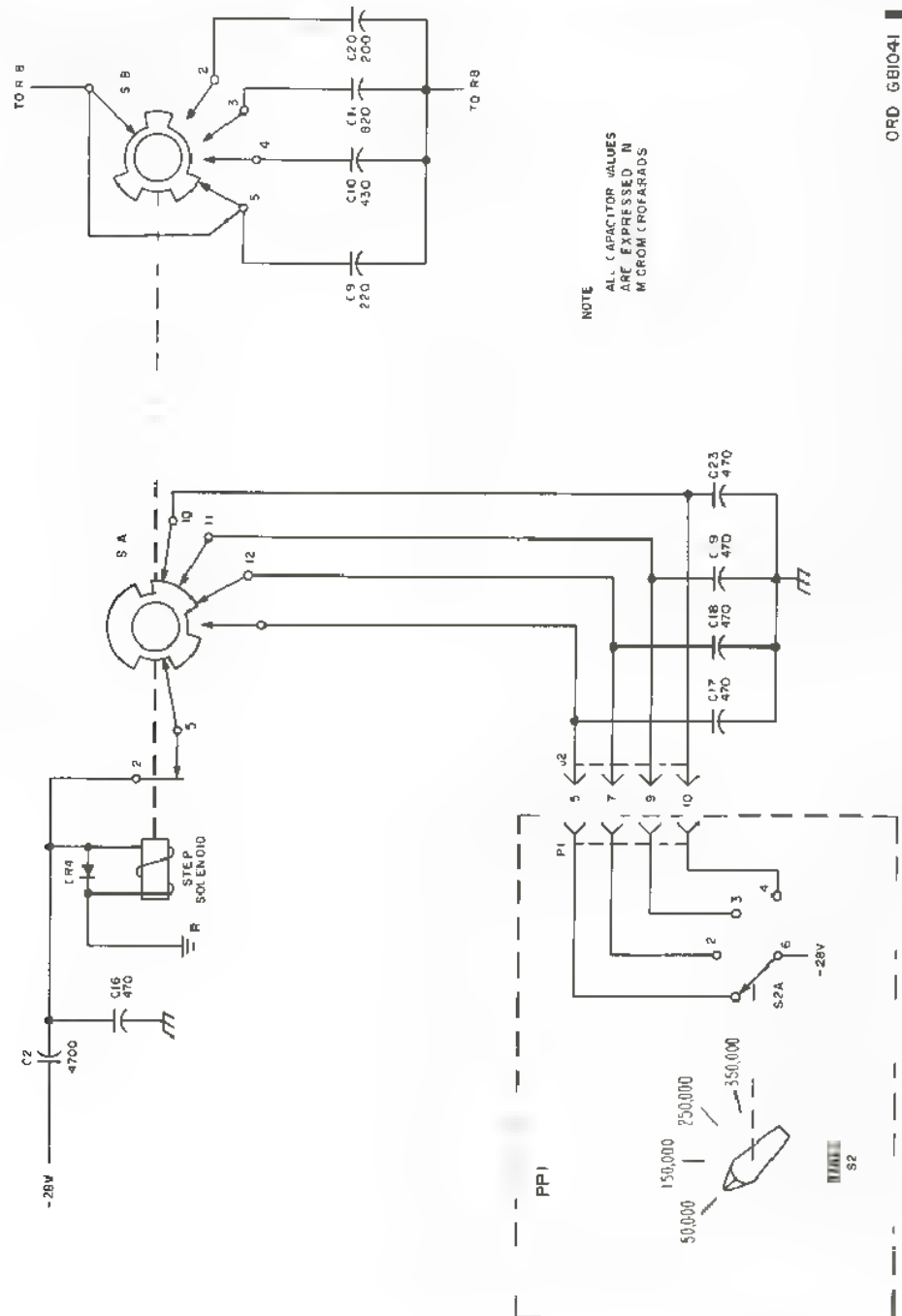
Figure 28.1 (CMHA). PPI video amplifier—switch S1—partial schematic diagram

NOTE:
ALL CAPACITOR VALUES
ARE EXPRESSED IN
MICROMICROFARADS

ORD G81041

(2) *Video channel*. The video channel (fig. 74, TM 9 1430–257 20) receives three inputs. an end of sweep pulse from the control channel, described in (1) above; acquisition video and marks from the video and mark mixer; and a symbols unblanking pulse from the PPI marker generator. The outputs of the video channel, which are unblanking pulses and amplified acquisition video and marks, are applied to the CRT. Two circuits are provided in the video channel for blanking the CRT. One circuit operates when the acquisition antenna is not rotating and the other when switching from the rotating sweep to the steerable azimuth line on the CRT screen. Blanking the CRT during the switching time prevents blossoming on the screen, which would obscure video presentations.

(a) *Video gate V4B*. Video gate V4B provides gating action for the video channel. The negative 305-microsecond end of sweep pulse from V2A is developed across R9 and coupled through C6 and series dropping resistors R11 and R15 to the grid of V4B. Crystal diode CR2 in parallel with R11 provides a quick discharge path for C6. When the positive-going trailing edge of the negative end of sweep pulse occurs, CR2 conducts. This results in a sharp trailing edge to the pulse. The negative pulse on the grid of V4B increases plate resistance, resulting in a positive 40-volt pedestal at the plate. Because the cathode signal of V4B follows the grid signal, a negative end of sweep pulse is developed at the cathode of

V4B. The negative pulse is developed across resistor R46 R46 is a common cathode resistor of V4B and video amplifier V4A.

(b) *Video amplifier V4A*. Video amplifier V4A amplifies and combines the acquisition video and marks with the sweep gate pulse from V4B The negative end of sweep pulse from V4B is amplified by V4A. The signal at the plate of V4A is a negative pulse. This pulse is a pedestal for the acquisition video and marks signals and an unblanking pulse for the CRT. The setting of pedestal adjust variable resistor R33 controls the amplitude of the pedestal. Resistors R33 and R46 are cathode resistors for V4A. Resistor R6 and inductor L1 make up the plate load impedance for V4A. High-level positive acquisition video and marks signals at connector J5 are coupled through capacitor C3 to the grid of V4A. Crystal diode CR3 clips the negative portion of the input acquisition video and marks signals. Negative signals coupled through C3 drive CR3 into conduction, bypassing the signals to ground. This high-level clipping permits almost complete elimination of the negative portion of the signals without loss of weak position video. Positive signals cut off CR3 and are developed across resistor R4. This resistor reduces the positive signals to a value suitable for the grid of V4A. The positive acquisition video and marks signals are amplified and inverted by V4A, resulting in negative signals at the plate. Inductor L1 in the plate cir-

98.6

cuit of V4A prevents the high frequency acquisition video and marks signals from entering the +150-volt supply. Capacitor C22 and resistor R45 bypass low frequencies to ground and sharpen the trailing edge of the pulse. The negative end of sweep pulse from V4B and acquisition video and marks signals at the plate of V4A are coupled to the control grid of video mixer V5. These signals are developed across resistor R36. Crystal diode CR1 clips the positive portion of the signals. Positive signals drive CR1 into conduction, bypassing the signals to ground. Negative signals cut off CR1 and the signals are developed across R36.

(c) *Symbol cathode follower V2B.* Symbol cathode follower V2B provides the symbols unblanking pulse for unblanking the CRT. The input signal to V2B is a negative 80-microsecond pulse This pulse occurs when symbols are to be painted on the PPI. The negative symbols unblanking pulse from the PPI marker generator at connector J6 is coupled to the grid of V2B. Resistor R24 forms part of a voltage divider which determines the amplitude of the unblanking pulse. Since the cathode follows the grid, a negative pulse is developed across resistor R27. This negative symbols unblanking pulse is applied directly to the screen grid of V5

(d) *Video mixer V5.* Video mixer V5 amplifies and mixes the acquisition video and marks that are applied to the CRT. The negative acquisition video and marks signals at the control grid of V5 are amplified and inverted by V5. Positive acquisition video and marks signals are coupled from the plate of V5 through capacitor C15 to connector P1. The pedestal from V4B unblanks the CRT, allowing the acquisition video and marks to be presented on the CRT. Negative symbols unblanking pulses from V2B applied to the screen grid of V5 result in positive pulses at the plate. These positive pulses unblank the CRT during the symbol-painting period. Inductor L2 in the plate circuit of V5 prevents high frequency acquisition video and marks signals from entering the +250-volt supply.

(e) *Blanking amplifier V6A.* A positive 300-microsecond off time extension pulse from the PPI marker generator is applied through connector J7 to the grid of blanking amplifier V6A. Resistors R35, R37, and R38 set the dc level of the input pulse. This positive pulse, starting at the end of normal sweep time, is passed to the grid of V4B through resistor R15 Thus, V4B conducts for a minimum of 300 microseconds between sweeps. This insures that, regardless of range or sync pulse repetition frequency, there will always be sufficient time between sweeps for the FUIF symbols to be displayed.

(f) *Blanking circuits.* When ANT RPM switch S13 (fig. 28.2) on the acquisition control-indicator is placed in the OFF position, connector J2-11 of the PPI video amplifier is grounded. This places the plate of crystal diode CR6 at ground potential, which in turn essentially places

98.7

NOTE
DOTTED LINE INDICATES MISSING CABLING

V4B
VIDEO
GATE
5670

SIGNALS
FROM V2A

R15
10,000

R12
0.51
MEG

CR8

TO PULSE AMPLIFIER V6B

CR6

R32
1 MEG

J2

11

12

8

PPI

P1

C4
0.02
UF

R6
2.2 MEG

+250V

10

4   3

C3
0.02
UF

CR6

9

2

STEERABLE
AZIMUTH LINE
K1

21

22

(NOTE)

(NOTE)

ACQUISITION
CONTROL—INDICATOR

OFF

14

15

13

6

ANT
RPM
S13

S13B

2

AZIMUTH
S1

TARGET DESIGNATE
CONTROL—INDICATOR

-28V

ORD G81059
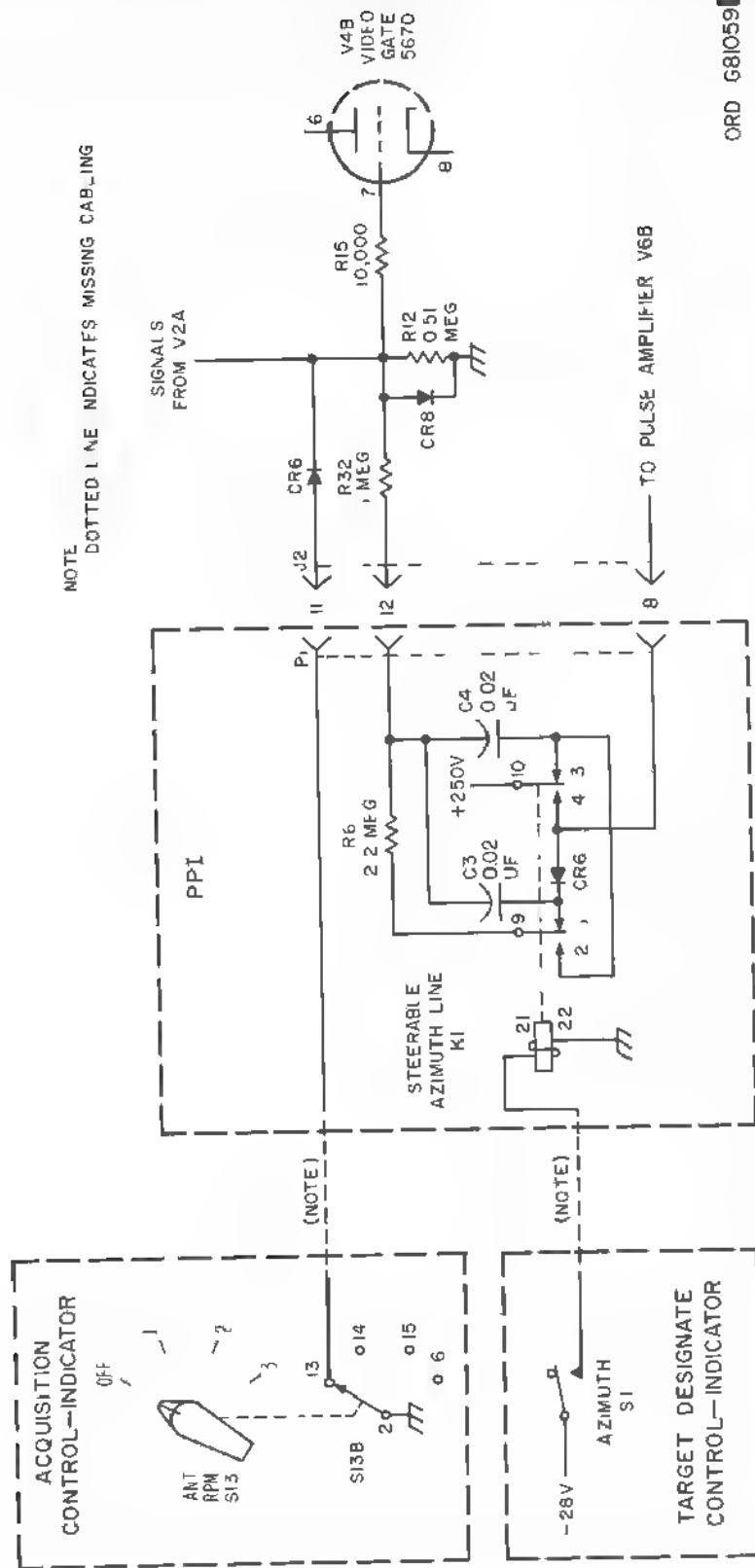
Figure 28.2 (U). PPI video amplifier blanking circuits — simplified schematic diagram.

the grid of V4B at ground. Thus, negative signals from V2A are essentially grounded, and this in turn keeps the CRT blanked. This blanking action takes place only when the acquisition antenna is not rotating. Crystal diode CR8 clips any positive signals at the grid of V4B. Negative signals cut off CR8 and are developed across R12 When switching from the radial sweep to the steerable azimuth line on the CRT, AZIMUTH switch S1 on the target designate control-indicator is operated. This activates steerable-azimuth line relay K1 in the PPI, closing K1 contacts 10 and 4. A sharp positive pulse is coupled to pulse amplifier V6B and through crystal diode CR6 and capacitor C3 in the PPI and resistors R32 and R15 in the PPI video amplifier to the grid of V4B. The charge path is from one plate of C3, CR6, the +250-volt supply, ground, resistor R12, and R32 to the other plate of C3. At the same time, capacitor C4 discharges through K1 contacts 2 and 9 and R6. The positive pulse at the grid of V4B, caused by the charging of C3, and the positive pulse at the grid of V6B result in blanking the CRT for the duration of the charging time of C3. A similar action occurs when K1 is deenergized Capacitor C4 charges at this time through one plate of C4, the +250-volt supply, ground, R12, R32, to the other plate of C4. Thus, two positive pulses applied to V4B and V6B blank the CRT during the switching action. Blanking the CRT prevents blossoming that would obscure the video presentations on the CRT screen.

(g) *Pulse amplifier V6B.* Pulse amplifier V6B and video gate V4B blank the CRT when switching from the radial sweep to the steerable azimuth line on the CRT. The blanking circuits apply a positive pulse to the grid of V6B through resistors R39 and R41. This positive pulse results in a positive pulse at the cathode of V6B. The cathode of V6B rises to a higher potential than the plate of V4A, which cuts off crystal diode CR5. This causes the plate voltage of V4A to rise and thus blanks the CRT to prevent blossoming. Resistor R44 is a cathode resistor and capacitor C25 is a cathode bypass resistor. Resistors R39, R40, R41, R42, and R43 form a voltage divider network for the grid of V6B.

39.7 (U). PPI Marker Generator 9143202

a. General. The PPI marker generator produces one of the three possible symbols, designated by the FUIF equipment, for presentation on the PPI cathode-ray tube screen. It also produces a symbols unblanking pulse for unblanking the PPI, and two gate control pulses for switching the electronic gates. The operating period of the PPI marker generator consists of three 80-microsecond intervals

b. Detailed Theory. PPI marker generator 9143202 (fig. 75, TM 9–1430–257–20) is the same as PPI marker generator 9007680, discussed in paragraph 39, except for the following modifications:

(1) Resistor R21 is connected to +250v instead of ground, which changes the discharge path of capacitor C10 described in paragraph 39b(3)(b) and

changes the operating time of V3 from 280 to 300 microseconds.

(2) The positive 300-microsecond pulse at the plate of V3B is also coupled through capacitor C25 and resistor R76 to connector J7. From J7, the pulse is coupled to the PPI video amplifier as an off-time extension pulse.

40 (U). Precision Indicator 8173218, 7007601

a. *General.*

(1) The precision indicator displays an enlarged sector of the plan-position indicator (PPI) presentation. This enlarged sector presents more accurate target azimuth and range information than the PPI. The sector of the PPI displayed on the precision indicator cathode-ray tube represents 533 mils (approximately 30°) in azimuth and 8000 yards in range. It is centered about the intersection of the flashing azimuth line and the range circle of the PPI display.

(2) The precision indicator contains four subassemblies listed in (a) through (d) below

(a) Range sweep generator 7617885

(b) Azimuth sweep generator mixer stage 7620604.

(c) Mark generator 8173013.

(d) Precision video amplifier 7620605.

b. *Functional Block Diagram Analysis.*

(1) The precision indicator (fig. 10, TM 9-1430-257 20) is composed of circuits shown in the functional block diagram in figure 29.

(2) The range sweep generator sends a trapezoidal range sweep pulse to the vertical deflection coils of the CRT to sweep the electron beam from the bottom to the top of the CRT screen. The input to the range sweep generator is the 50-microsecond acquisition range gate. The output range sweep pulse is 50 microseconds in duration and occurs at a repetition rate of 500 pps. Therefore, the vertical sweep

lasts for 50 microseconds and is cut off for approximately 1950 microseconds The 50-microsecond sweep represents an 8000-yard sector of the PPI display in range.

(3) The azimuth sweep generator mixer stage sends an azimuth sweep signal to the horizontal deflection coils of the CRT to sweep the electron beam across the screen of the CRT. The inputs to the azimuth sweep generator mixer stage are a 4-kc reference carrier and a modulated 4-kc signal. The output is a severely clipped sine wave with an unclipped sector equal to 533 mils (approximately 30°). This unclipped sector is practically linear and produces the horizontal sweep from left to right across the screen during the time the CRT is unblanked.

(4) The mark generator produces a 711-mil (approximately 40°) acquisition azimuth gate and a 1350-microsecond acquisition azimuth mark. The acquisition azimuth gate is used to unblank the CRT for 533 mils of one acquisition antenna revolution. During each revolution of the acquisition antenna, the acquisition azimuth mark brightens one sweep on the PPI to produce the flashing azimuth line. The inputs to the mark generator are the sync pulse, the 4-kc reference carrier, and the two modulated 4-kc signals that are 90° out of phase.

(5) The precision video amplifier applies the acquisition video and marks to the CRT and also unblanks the CRT. The acquisition video and marks are always applied to the cathode of the CRT but are not displayed until the CRT is unblanked. The inputs to the precision video amplifier are the acquisition video and marks, INTENSITY dc voltage, the acquisition azimuth gate, and the 50-microsecond acquisition range gate. GAIN variable resistor R9 determines the amplitude of the acquisition video and marks. IN-

RA PD 468138
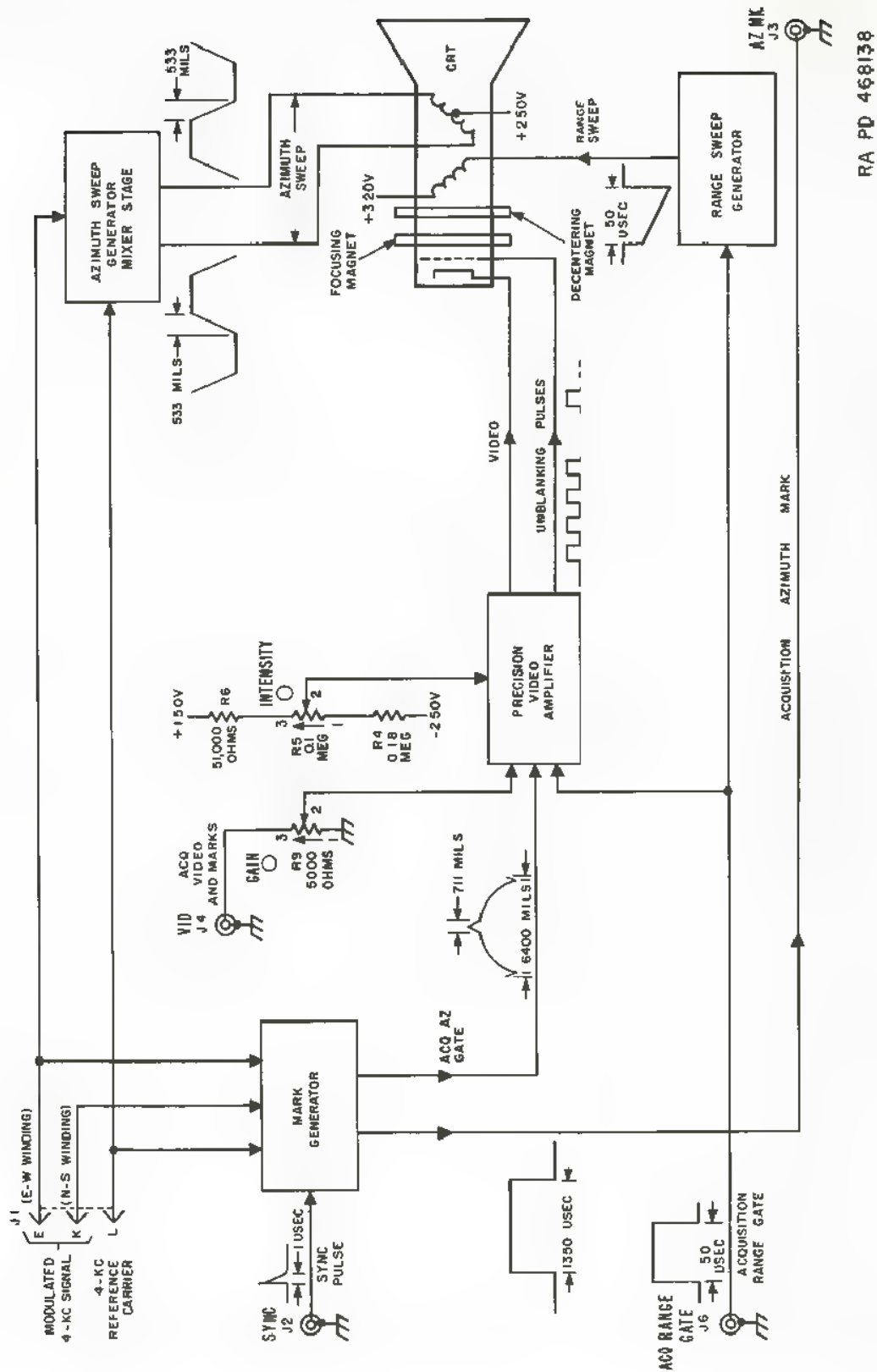
Figure 29 (U). Precision indicator—functional block diagram.

TENSITY variable resistor R5 determines the dc level baseline of the unblanking pulses, which in turn determines the brightness of the presentations on the screen of the CRT. The acquisition azimuth gate and the 50-microsecond acquisition range gate are mixed to form the unblanking pulses.

(6) The CRT circuit includes the horizontal and vertical deflection coils, the focusing magnet, and the decentering magnet. The azimuth sweep signal is applied to the horizontal deflection coils for sweeping the electron beam from left to right on the screen of the CRT. The range sweep pulse is applied to the vertical deflection coils for sweeping the beam from bottom to top.

(a) The focusing magnet is used to center the electron beam on the screen of the CRT. This magnet is cylindrical in shape with an adjustable shunt to vary the strength and configuration of the magnetic field. Electrons which are moving exactly on the axis of the magnetic field set up by the focusing magnet are not deflected. All other electrons are deflected by the magnetic field which produces inward radial accelerations to bring the electrons together at a common point. This common point is known as the focus point. The distance between the cathode and focus point is proportional to the intensity of the magnetic field which is controlled by the adjustable shunt. The adjustable shunt is adjusted so that the focus point is at the screen of the CRT. To correct for CRT element misalinements, a centering ring is provided on the focusing magnet to change the shape of the magnetic field. Altering the position of the centering ring changes the point where the electron beam strikes the screen of the CRT.

(b) The decentering magnet is used to return the electron beam to the bottom of the CRT screen. This magnet consists of two permanent bar magnets, two pole pieces, and two adjustable shunts. When the shunts are positioned close to the magnets, decreasing the air gaps, the magnetic field is decreased, which deflects the electron beam a slight amount. Increasing the air gaps increases the magnetic field, resulting in a greater deflection of the electron beam. The shunts are normally adjusted to place the electron beam at the bottom of the screen on the CRT.

c. *Precision Indicator 9007681.* Precision indicator 9007681 (fig. 10, TM 9-1430-257-20) is the same as precision indicator 8173218 which is covered in *a* and *b* above. The Ordance part number of the precision indicator was changed because two of the subassemblies were changed. Precision indicator 9007681 contains the four subassemblies listed in (1) through (4) below. The two precision indicators are not interchangeable.

(1) Range sweep generator 8607326.
(2) Azimuth sweep generator mixer stage 7620604.
(3) Mark generator 9007682.
(4) Precision video amplifier 7620605.

d. *Precision Indicator 9985665.* Precision indicator 9985665 (fig. 10.1, TM 9-1430-257-20) is the same as precision indicator 9007681 which is covered in *c* above except for the items covered in (1) through (3) below which were added by DA MWO 9-1400-263-30.

(1) CONTROL TRANSFER switch S1 is added to switch control of the NAR (Nike acquisition radar) receiver-transmitter control from the remote console to the acquisition control-indicator. This action occurs when S1 is set to AUTOMATIC and RADAR SELECTED switch S2 is set to NAR.

(2) RADAR SELECTED switch S2 is added to select video from either the NAR or AAR (auxiliary acquisition

radar). The switching function is controlled by S2 when S1 is set to AUTOMATIC. When S1 is set to REMOTE, the switching function is controlled from the remote console.

(3) CHANGE RADAR indicator light DS1 is added to advise the battery commander that the ECCM officer desires a change in radar video from the NAR to AAR or AAR to NAR.

41 (U). Range Sweep Generator 7617885, 8607326

a. General. The range sweep generator provides a range sweep pulse having a sawtooth current waveform to the vertical deflection coils of the cathode-ray tube in the precision indicator. This range sweep pulse generates a range sweep on the CRT screen.

Note. Continuous reference in *b* and *c* below is made to figure 11, TM 9–1430–257–20 unless otherwise indicated.

b. Detailed Theory.

(1) With no signal applied at connector J1, trapezoidal sweep generator V1A conducts. Current flows from ground through resistors R4 and R3, V1A, and resistors R2 and R1 to the +150-volt supply. A large voltage drop is developed across R1 and R2 because of their large values. This makes the plate volt-

age of V1A slightly higher than the cathode. Capacitor C1 charges to a voltage equal to the voltage across V1A and R3.

(a) Generator V1A cuts off when the positive acquisition range gate (A, fig. 30) is applied to the cathode. Capacitor C1 now charges along an RC curve determined by R4, C1, R2, and R1, and the +150-volt supply. The time constant of this path is long compared to the 50-microsecond acquisition range gate. Therefore, C1 can charge for only a fraction of the circuit RC curve which results in a linear voltage rise at the plate of V1A. The amplitude of the voltage rise is determined by the setting of amplitude variable resistor R2. If R2 is shorted (brush arm fully clockwise), C1 charges faster because the circuit time constant is smaller. Capacitor C1 charges to a higher voltage than it would if R2 were in the circuit. When the positive acquisition range gate drops to zero, V1A conducts, and the low resistance of V1A and R3 provides a path for rapid discharge of C1. This results in a sharp negative-going trailing edge at the plate of V1A, and a sawtooth waveform is created at the plate of V1A.

(b) To create a trapezoidal waveform, it is necessary to provide a step at the leading edge of the sawtooth. A small portion of the acquisition range gate applied at J1 is developed across R4 and applied to C1. Capacitor C1 acts as a short circuit to this step voltage which is the leading edge of the trapezoidal waveform. The resultant waveform (B, fig. 30) at the plate of V1A is a series of trapezoidal voltages 50 microseconds wide.

(2) The trapezoidal voltages at the plate of V1A are applied directly to the control grid of voltage amplifier V2, where they are amplified and inverted. Amplifier V2 is a voltage amplifier with degenera-

tive feedback in the cathode circuit. Resistor R17 can be considered as the cathode resistance of V2. Because of the small size of capacitor C6, R17 can be considered as being unbypassed. Capacitor C6 effectively short circuits the sharp rise time of the trapezoidal waveform, and no degenerative feedback is developed in the cathode circuit of V2. This action prevents the distributed capacitance in the circuits of power amplifiers V4 and V5 from affecting the trapezoid. The distributed capacitance would tend to distort the sharp rise time of the waveform. By removing the degenerative feedback during the sharp rise time, the gain of V2 is increased. This allows the distributed capacitance in the circuits of V4 and V5 to charge without distorting the waveform. Capacitor C2 and resistor R7 in the plate circuit of V2 prevents oscillations at high frequencies. Capacitor C3 couples the signal (C, fig. 30) from the plate of V2 to the control grid of voltage amplifier V3, which is a conventional voltage amplifier. After amplification and inversion by V3, the signal (B, fig. 30) is coupled through

A. ACQ RANGE GATE INPUT

B. PLATE VIA, V3 CONTROL GRID V2, V4, V5 CATHODE V1B

C. CONTROL GRID V3 PLATE V2, V4, V5

D. PLATE CURRENT V4, V5 FEEDBACK VOLTAGE TO CATHODE V2
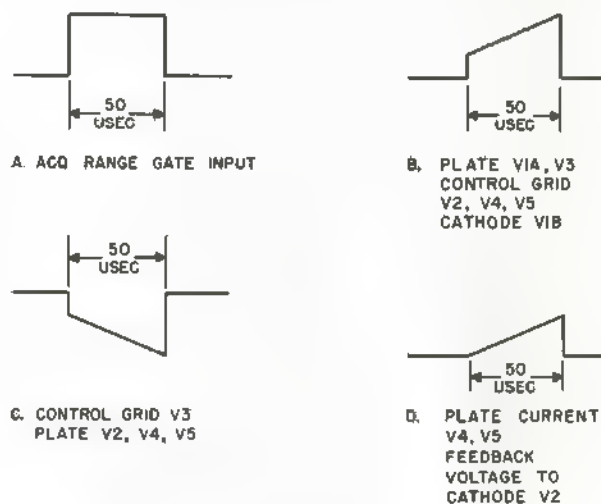
RA PD 468139

Figure 30 (U) Range sweep generator—waveforms

CONFIDENTIAL

capacitor C4 to the cathode of clamper V1B and the control grids of V4 and V5. Resistors R19 and R22 in the control grid circuits of V4 and V5 prevent parasitic oscillations.

(3) Power amplifiers V4 and V5 are operated in parallel to meet the current requirements of the output load. The plate load of V4 and V5 is the vertical deflection coils of the precision indicator CRT. Since considerable resistance in the coils prevents them from appearing as a pure inductance, the output load must be treated as an RL circuit. To produce a sawtooth of current through an RL circuit, it is necessary to apply a trapezoidal voltage, which contains both square-wave and sawtooth-wave components. The square-wave component produces a linear current increase through the inductance of the coils, and the sawtooth-wave component produces a linear increase through the resistance. The plate current waveform (D, fig. 30) of V4 and V5 is a linear sawtooth waveform and the plate voltage waveform (C, fig. 30) is a trapezoidal waveform.

(4) The current in the cathode circuit of V4 and V5 may be considered as having two components, a plate current and a screen current. Since the screen current does not flow in the output load, it is desired that only voltages representing the plate current waveform (D, fig. 30) of V4 and V5 be used for feedback to V2. To eliminate the screen current component, it is necessary to develop an inverse voltage to cancel the effect of the screen current. The screen current develops a voltage across resistors R23 and R27 that is fed through resistor R17 to the cathode of V2. The cathode of V2 becomes more positive than the cathode of V4 when a positive pulse is applied to the control grid of V4. However, a rise in screen current at this time causes the junction of R18 and R20 to become more negative. The voltage drop across resistor R25 is

reflected through resistor R20, causing the cathode of V2 to become more negative than the cathode of V4. Thus, the voltage developed across R25 is 180° out of phase with the voltage developed across R23 and R27. Canceling the effect of screen current in this manner improves linearity of the sawtooth current waveform in the output load.

(5) Clamper V1B returns the control grids of V4 and V5 to a constant voltage level at the end of each trapezoidal pulse. A constant bias voltage of approximately −80 volts is developed across resistors R12 and R13 and is applied to the grid of V1B. Since the plate of V1B is connected to +150 volts through resistor R28 and the cathode to −250 volts through resistor R11, V1B will conduct during the quiescent period. Current flow through R11 and V1B provides a voltage at the cathode of V1B that is approximately −72 volts. Capacitor C4 is charged to the difference in potential between the plate of V3 and the cathode of V1B.

(a) The positive trapezoidal voltage at the plate of V3 is coupled through C4 to the cathode of V1B and the control grids of V4 and V5. Because the charge on C4 cannot change instantaneously, this trapezoidal voltage appears on the cathode of V1B and the control grids of V4 and V5. This positive voltage on the cathode drives V1B toward cutoff. Because of the long time constant, the charge on C4 increases only a small amount during the trapezoidal pulse. Charge current flows from the plate of C4 connected to V3, through resistor R9, +250 volt supply, ground, −250-volt supply, and through R11 to the other plate of C4. The time constant of this path is long compared to the trapezoidal pulse.

(b) The trailing edge of the trapezoidal pulse adds algebraically to the charge on C4 and drives the cathode of V1B

CONFIDENTIAL

negative. Clamper V1B conducts and discharges C4 rapidly to its quiescent value. The discharge path for C4 is from the plate connected to R11, through V1B, R28, and the +150-volt supply, ground, and V3 to the other plate of C4. The discharge time is short and the cathode of V1B and control grids of V4 and V5 are returned rapidly to the quiescent value of −72 volts. This action insures that the negative extreme of the trapezoidal pulse to V4 and V5 is clamped at a fixed voltage level. During quiescence, current flowing in V4 and V5 and through the deflection coils always has the same value because the biasing voltage is always the same at this time. This causes the sweep on the CRT to always start from the same point.

a. Range Sweep Generator 8607326. Range sweep generator 8607326 is similar to range sweep generator 7617885 described in *a* and *b* above. It differs in that a clipper circuit is added to eliminate noise. Capacitor C7 acts as a short circuit to the positive pulse input at connector J1. Therefore, the input waveform is not distorted. Resistors R3 and R4 produce a bias of approximately +0.7 volt for the clipper circuit comprised of crystal diode CR1 and resistor R26. Signals more negative than the bias level are clipped at the bias level. Positive signals above the bias level are not clipped but are applied directly to the cathode of V1B. The bias voltage is above the level of noise which, if not eliminated, would create sweep jitter. Elimination of the noise results in a stabilized sweep on the precision indicator CRT. The remainder of detailed theory is the same as discussed in *b* above.

42. Azimuth Sweep Generator Mixer Stage 7620604

a. General. The azimuth sweep generator mixer stage provides a sawtooth current waveform to the horizontal deflection coils of the cathoderay tube in the precision indicator. This waveform generates a horizontal sweep on the screen of the CRT. This sweep represents 533 mils azimuth rotation of the acquisition antenna.

Note. Continuous reference in *b* below is made to figure 12, TM 9-1430-257-20 unless otherwise indicated

b. Detailed Theory.

(1) The 4-kc reference carrier (A, fig. 31) at connector P1-1 and 3 is applied to the primary of transformer T1. This signal has a constant amplitude of approximately 70 volts. It is used to provide switching action for rectifiers V1 and V2. The modulated 4-kc signal (A, fig. 31) at connector P1-5 and 7 is applied to the primary of transformer T2 which is in series with AZ ADJ variable resistor R2. This signal is sine-wave modulated by the rotation of the acquisition antenna. The two 4-kc signals are in phase during one-half revolution of the antenna and 180° out of phase during the other half revolution. Variable resistor R2 determines the amplitude of the modulated 4-kc signal which is approximately one-third the amplitude of the 4-kc reference carrier.

(2) The ring demodulator detailed theory is the same as the crystal bridge demodulator theory covered in paragraph 34*b* (1) through (5) and is not repeated here.

(3) The demodulator output is two sine-wave voltages (B, fig. 31), opposite in polarity, developed across resistors R8 and R9. Direction of current flow through R8 and R9 determines the polarity of the signals. Because the signals are taken from opposite ends of equal size resistors, they are equal in amplitude. One cycle of the sine wave across R8 and R9 corresponds to one revolution of the acquisition antenna.

(5) The voltage developed across R8 is filtered by the filter network composed of resistors R10 and R14 and capacitors C2 and C5. A similar network composed of resistors R12 and R15 and capacitors C3 and C4 filters the voltage developed

A · OV — MODULATED 4-KC SIGNAL · OV — 4-KC REFERENCE CARRIER

B · -9V — WAVEFORM ACROSS R8 · -9V — WAVEFORM ACROSS R9

C · -9V — AFTER RC FILTERING · -9V — AFTER RC FILTERING

D · -2V -9V — CLIPPED WAVEFORM AT GRIDS OF V4 · -2V -9V — CLIPPED WAVEFORM AT GRIDS OF V5

E · 533 MIL (30 DEG) — PLATE CURRENT OF V4 · 533 MIL (30 DEG) — PLATE CURRENT OF V5 · 0 CURRENT · 0 CURRENT
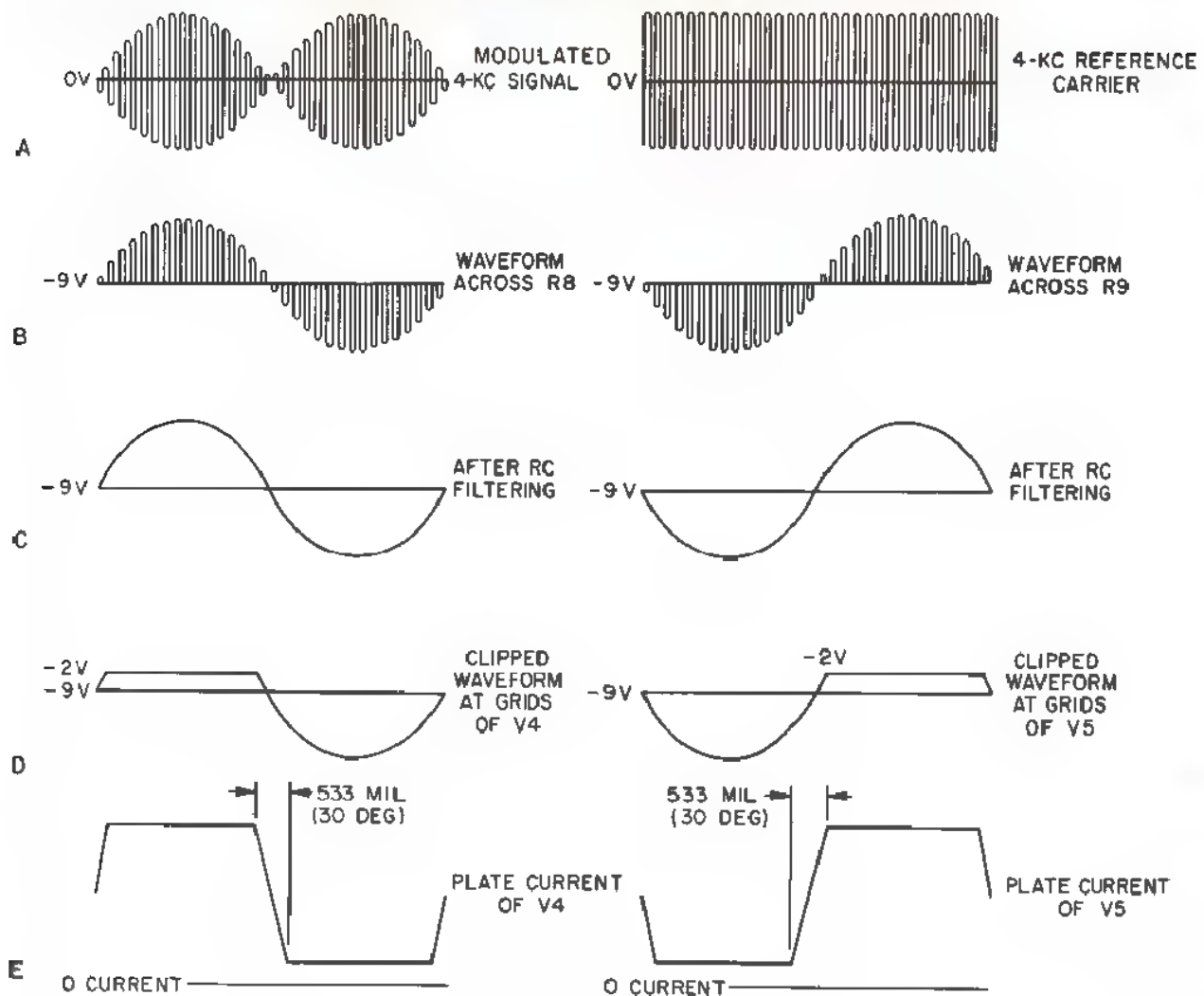
RA PD 468140

Figure 31. (U) Azimuth sweep generator mixer stage—waveforms

across R9. The two filter networks remove the 4-kc component from the signal (C, fig. 31) and apply the remaining sine waves to the plates of limiters V3A and V3B. Bias for both V3A and V3B is determined by the voltage drop across resistor R13 which is part of a voltage divider composed of resistors R13, R11, and R7 connected between -250 volts and ground. Therefore, a negative potential of approximately 2 volts is applied to the cathodes of V3A and V3B. A neg-

ative voltage of approximately -9 volts developed across R13 and R11 is the reference voltage for signals at the plates of V3A and V3B. When the plate voltage is more positive than the -2-volt bias at the cathode, V3A and V3B conduct and limit the signals at -2 volts amplitude. Since the plate voltages of V3A and V3B are 180° out of phase, V3A has an increasing plate voltage while V3B has a decreasing plate voltage and vice versa. Portions of the plate signals more

negative than −2 volts are not limited because that section (V3A or V3B) is cut off. The plate signals of V3A and V3B are sinusoidal voltages with the positive portion clipped at −2 volts and an unclipped negative portion. These voltages alternate about a −9-volt reference level. These voltages (D, fig. 31) are applied to the grids of drivers V4A, V4B, V5A, and V5B, which are connected in push-pull.

(5) The negative portions of the grid signals cause V4A, V4B, V5A, and V5B to cut off. The positive portions cause them to saturate. Therefore, the plate signals of V4A, V4B, V5A, and V5B resemble sinusoidal voltages with both negative and positive portions clipped. Since the grid signals are 180° out of phase, the current through one driver increases linearly while the current in the other driver decreases linearly. The portion of the plate signals not clipped corresponds to 533 mils (approximately 30°) in azimuth (E, fig. 31) and occurs twice during one revolution of the acquisition antenna. These 533-mil unclipped portions of the waveform are used to produce the sweep. Thus, there are two horizontal sweeps on the CRT per antenna revolution. One sweep appears on the CRT moving from left to right once per revolution of the acquisition antenna. The other sweep appears as a spot moving from right to left at the bottom of the CRT.

(6) With no signal input, the grid voltages of V4A, V4B, V5A, and V5B should be equal and the plate voltages should be equal. BAL ADJ variable resistor R17 varies the bias on the cathodes of V4A, V4B, V5A, and V5B to compensate for unbalance in component parts. This assures symmetrical presentations on the CRT. Variable resistor R2 is adjusted to make the sweep current equal to 533 mils in azimuth. Decreasing R2 causes a steeper slope in the modulated 4-kc signal input to transformer T2 which de creases the sweep interval. Increasing R2 increases the sweep interval. Resistors R18 through R25 are parasitic suppressors in the grid and plate circuits of V4A, V4B, V5A, and V5B

43. Mark Generator 8173013, 9007682

a. General. The mark generator produces two outputs; the acquisition azimuth gate produced by the gate channel, and the acquisition azimuth mark produced by the mark channel. The acquisition azimuth gate is 711 mils (approximately 40°) in duration and is used for unblanking the precision indicator cathode-ray tube and gating various other circuits of the acquisition radar system. The acquisition azimuth mark is a 1,350-microsecond pulse used to produce the flashing azimuth line on the plan-position indicato (PPI) once during each revolution of the acquisition antenna. It also provides the vertical li on the precision indicator CRT.

Note Continuous reference in *b* and *c* below is ma to figure 13, TM 9-1430-257-20 unless otherwise indicate

b. Detailed Theory

(1) *Gate channel.* The gate channel pr duces a 711-mil gate and a 14 mil ga Both gates are superimposed on a pe estal also generated in this channel. T 711-mil gate atop the pedestal is t acquisition azimuth gate. The 14 m gate atop the pedestal is used to trigg coincidence amplifier V7 in the ma channel.

(*a*) The modulated 4-kc signal (A, fig. 3. at connector P1-1 is developed acros resistor R2 and applied through resis tor R1 to the grid of clipper-limite V1A. Resistor R1 is a grid limiting resistor which clips the positive half cycles of the signal by drawing current. The negative half cycles of the signal are of sufficient amplitude to drive V1A into cutoff. At the plate of V1A, 711 mils (approximately 40°) of the waveform remains unaffected (B, fig. 32). This unaffected portion is centered about the null point. The

CONFIDENTIAL

null point is the point of minimum voltage every 3,200 mils of the modulated signal.

(b) From the plate of V1A, the 4-kc signal is coupled through capacitor C1 and resistor R7 to the grid of clipper-limiter V1B. The 4-kc signal is also coupled through C1 to the cathode of coincidence detector V4A, as discussed in (e) below. Resistor R7 limits grid current, and capacitor C16 prevents high-frequency noise from affecting the operation of V1B. For production of sharp gate pulses, the input cir-

+ PHASE   − PHASE   + PHASE   − PHASE

A 0V

MODULATED 4-KC INPUT SIGNAL

70-MIL (40-DEG) UNCLIPPED SECTION

B 0V

OUTPUT OF V1A

14-MIL (0.8-DEG) UNCLIPPED SECTION

C 0V

OUTPUT OF V1B

14-MIL GATES

D 0V

OUTPUT OF V2A AFTER FILTERING

E 0V

INPUT TO V3A

F 0V

6400 MILS
(360 DEG)

OUTPUT OF V2B AFTER FILTERING
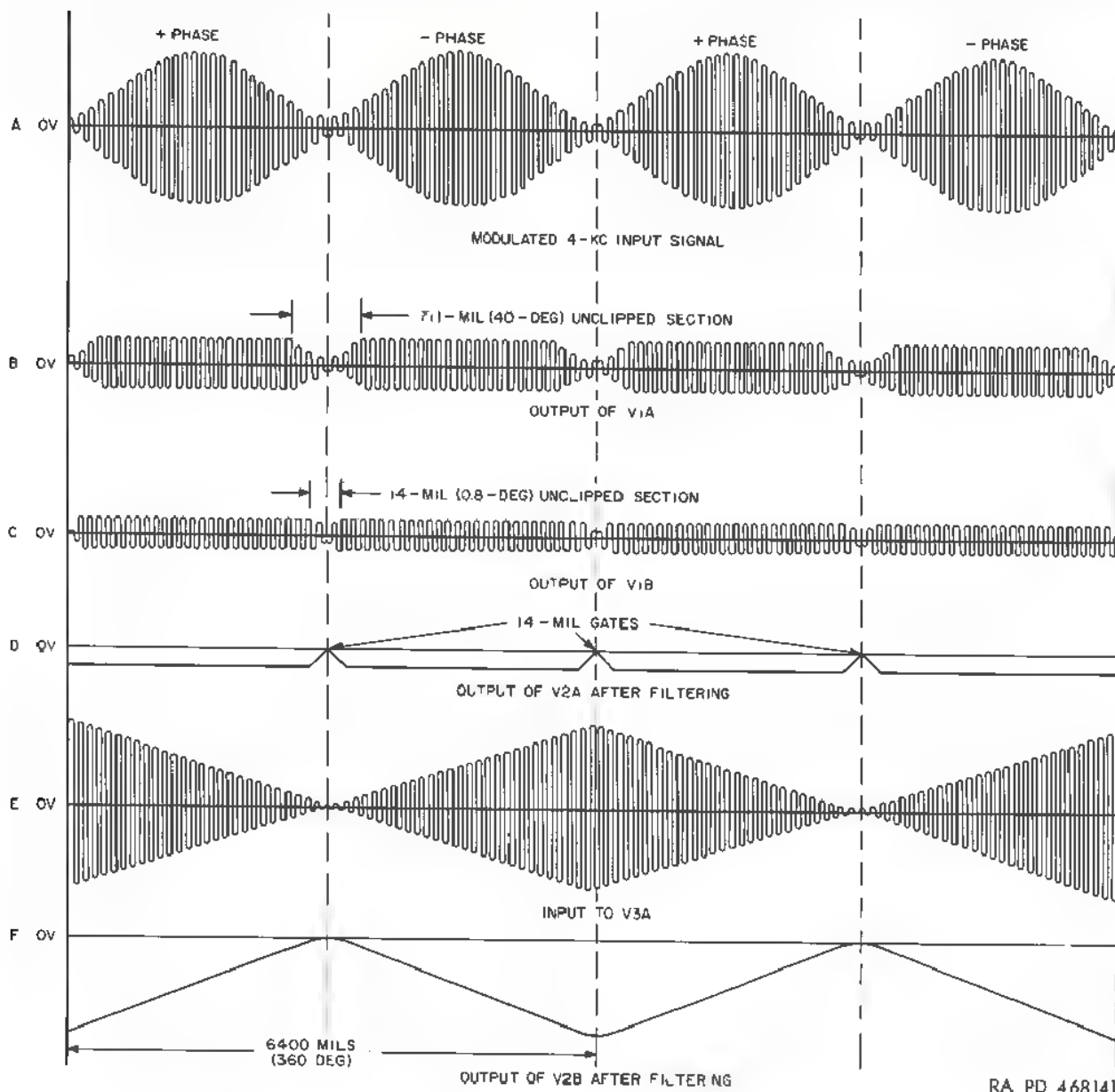
RA PD 468141

Figure 32 (U) Mark generator—V1, V2, and V3A—waveforms

CONFIDENTIAL

cut noise must be 0.2 volt or less. The action of V1B is similar to that of V1A. Clipper limiter V1B further limits and clips the 4-kc signal, reducing the unaffected portion to a 14-mil (0.8°) width (C, fig. 32). The 4-kc signal from the plate of V1B is coupled through capacitor C2 to the cathode of gate detector V2A which removes the positive portion of the signal. Bias for V2A is determined by GATE ADJ variable resistor R10 in series with resistor R9 and the +250-volt supply. Variable resistor R10 allows adjustment of the 14-mil unclipped section to an amplitude which accurately produces the acquisition azimuth mark, as discussed in (2) below, for all azimuth settings. The 4-kc signal at the plate of V2A is filtered by capacitor C3 and resistor R12 to remove the 4 kc component. This signal (D, fig. 32) is 14-mil gates occurring at 3,200-mil intervals. Since only one gate in 6,400 mils is desired, a pedestal is required to dispose of the undesired gate.

(c) The pedestal for the gates is formed by first mixing the 4-kc reference carrier from connector P1–7 and the modulated 4-kc signal from connector P1–5 developed across 4 KC ADJ variable resistor R20. The modulated 4-kc signal at P1–5 is either in phase or 180° out of phase with the 4 kc reference carrier at P1–1. The 4-kc reference carrier and the modulated 4-kc signal are in phase for the first half cycle and out of phase for the next half-cycle. This results in reinforcement during the in-phase half-cycle and subtraction during the out-of-phase half-cycle. The desired 4-kc signal at the brush arm of R20 is a 100-percent, sinusoidally-modulated waveform as shown in E, figure 32. Since the maximum amplitude of the modulated 4-kc signal and the 4-kc reference carrier are not equal, mixing the signals in R20

produces only one null point per antenna revolution. Test point TP1 is provided for externally monitoring the mixing of signals in R20 using an oscilloscope. Improper adjustment of R20 as viewed on an oscilloscope results in either undermodulation (fig. 33) or overmodulation. Proper adjustment of R20 provides the desired 100-percent modulation.

100–PCT MODULATION

UNDERMODULATION

OVERMODULATION

RA PD 226143
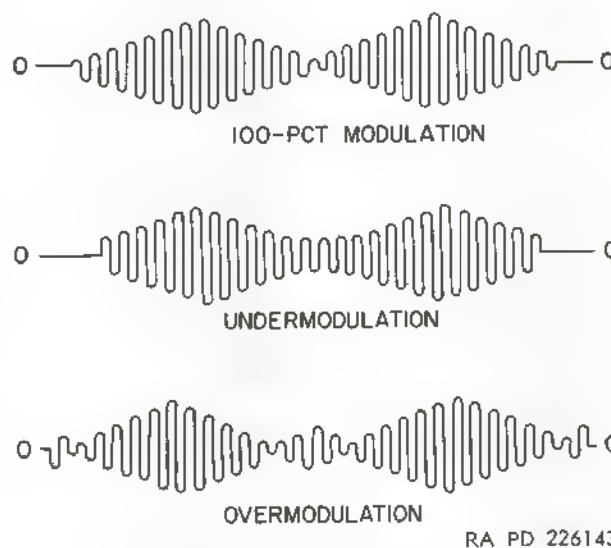
Figure 33. (U) Modulated waveforms

(d) The 100-percent modulated signal (E, fig. 33) from the brush arm of R20 is coupled through capacitor C14 to the grid of gate amplifier V3A. Grid bias for V3A is the voltage drop across resistor R15, part of a voltage divider consisting of resistors R13 and R15 connected between −250 volts and ground. After the signal is amplified by V3A, it is coupled through capacitor C13 to coincidence detector V4B and through resistor R18 to the cathode of gate detector V2B. Resistors R14 and R42 form a voltage divider between +250 volts and ground. The voltage drop across R42 provides positive cathode bias to V2B and V4B. Resistor R16 effectively isolates cath-

CONFIDENTIAL

ode signals from the voltage divider. Since the cathode must be negative with respect to the plate before V2B and V4B conduct, positive portions of the 4-kc signal are eliminated. The remaining negative portions at the plate of V2B are then filtered by C3 and R12 to remove the 4 kc component (F, fig. 32). The pedestal waveform from V2B is mixed with the 14-mil

gate from V2A and the composite gate on a pedestal (A, fig. 34) is applied to the suppressor grid of V7. The negative portions of the 4-kc signal at the plate of V4B are filtered by capacitor C5 and resistor R21 to remove the 4-kc component. This waveform (B, fig. 34) is the pedestal for the 711-mil gate.

(e) The 711-mil acquisition azimuth gate is obtained by using the output of V1A

Figure 34. (C) Mark generator—V3B through V7—waveforms.

108
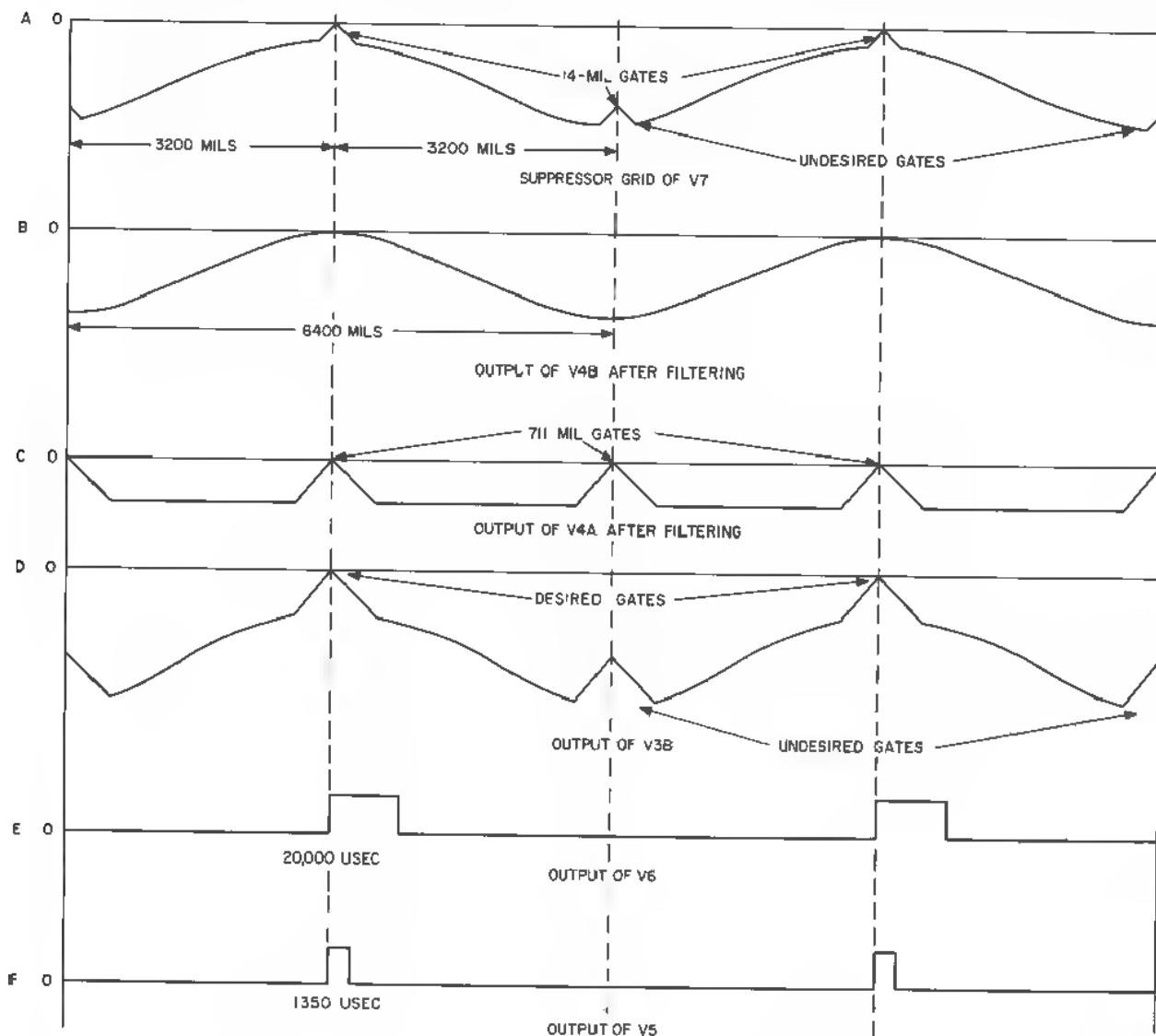
RA PD 468142

(B, fig. 32) after the 4-kc signal has been through only one stage of clipping and limiting. The 4-kc signal from V1A is coupled through C1 to the cathode of V4A. Positive portions of the 4-kc signal are eliminated by V4A. The negative portions of the 4-kc signal are filtered by C5 and R21 to remove the 4-kc component (C, fig. 34). The signal at the grid of gate cathode follower V3B, an isolation stage, is a combined waveform consisting of a 711-mil gate from V4A superimposed on a pedestal from V4B as discussed in (d) above. Selection of the desired gate is determined by the pedestal. The acquisition azimuth gate output from the cathode of V3B to connector P1–10 is shown in D, figure 34.

(2) *Mark channel.* The function of the mark channel is to generate the 1,350-microsecond acquisition azimuth mark.

(a) The undesired 14-mil gate (A, fig. 34) has no effect on V7, since the pedestal from V2B is at its most negative point when the acquisition antenna is passing through the position 3,200 mils away from the desired azimuth setting. The desired 14-mil gate atop the pedestal raises the suppressor grid potential of V7 toward zero. Positive sync pulses which are always present at SYNC connector J1 are developed across resistor R41 and coupled through capacitor C12 to the control grid of V7. Control grid bias for V7 is the voltage drop across R40 which is part of the voltage divider consisting of resistors R40 and R39 connected between −250 volts and ground. Only the sync pulses in coincidence with the 14-mil gate atop the pedestal are amplified and inverted through V7. The signal at the plate of V7 is coupled through capacitor C11 to the grid of monostable multivibrator V6A which allows only the gated pulses to be transmitted.

(b) Monostable multivibrator V6A is normally conducting because of the positive voltage at the grid. This positive grid voltage is developed by the voltage divider consisting of resistors R33 and R31 connected between ground and the +250-volt supply. The multivibrator is triggered by the first pulse exceeding −10 volts. Because of the long time constant (20,000 microseconds), no other pulse selected by the 14-mil gate can again trigger the multivibrator during this cycle. When the multivibrator is triggered, V6A cuts off, resulting in a voltage decrease across common cathode resistor R37 of V6A and monostable multivibrator V6B. This voltage decrease causes V6B to conduct, which causes a voltage decrease at the plate of V6B. The plate voltage decrease of V6B is coupled through capacitor C10 as feedback to the grid of V6A. The time constant of the multivibrator is determined by the discharge of C10, which is from one plate of C10 through resistors R34, R33, ground, resistor R37, and V6B to the other plate of C10. The discharging action of C10 continues until the grid potential of V6A rises above cutoff, causing V6A to conduct. This action cuts off V6B and the multivibrator returns to the quiescent state of operation.

(c) The square wave developed at the plate of V6A (E, fig. 34) is differentiated by capacitor C9 and resistors R25 and R26, which results in a sharp positive pip at the grid of monostable multivibrator V5A. Multivibrator V5A is normally cut off by the negative voltage at the grid developed by the voltage divider consisting of resistors R25 and R24 connected between the −250-volt supply and ground. The positive pip drives V5A into conduction. From the plate of V5A, a negative-going signal is coupled through capacitor C8 to the

CONFIDENTIAL

grid of monostable multivibrator V5B. The negative-going signal at the grid drives V5B to cutoff, resulting in a positive-going signal at the plate. The positive-going signal is coupled through capacitor C7 back to the grid of V5A. This regenerative feedback causes conduction in V5A to increase rapidly. The feedback also assures quick recovery after the multivibrator cycle is complete. This results in a square-wave pulse with sharp leading and trailing edges. A 1,350-microsecond (minimum) positive-going square-wave pulse (F, fig. 34), the acquisition azimuth mark, appears at the cathode of V5A. The length of the acquisition azimuth mark is determined by the discharge time of C8 through resistor R30. The complete discharge path of C8 is from one plate of C8 through R30, the +250-volt supply, ground, resistor R27, and V5A to the other plate of C8.

c. Mark Generator 9007682. Beginning with system 1049, mark generator 9007682 replaces mark generator 8173013. In mark generator 9007682, MARK LENGTH variable resistor R32 is connected from one end of R30 to the grid of V5B. Resistor R30 is changed from 0.953 to 0.56 megohm. Capacitor C8 is changed from 3,000 to 3,600 micromicrofarads. The changing of these components causes C8 to discharge for a longer period of time which results in a longer acquisition azimuth mark. Variable resistor R32 is normally adjusted for an output pulse width of $1,600 \pm 25$ microseconds. The pulse width can be varied by R32 between 1,400 and 1,800 microseconds. The remainder of the detailed theory is the same as discussed in *b* above.

44. Precision Video Amplifier 7620605

a. General The precision video amplifier applies the video and unblanking pulses to the cathode-ray tube of the precision indicator. The precision video amplifier consists of two channels, a video channel and an unblanking channel. The video channel consists of clamper CR1 to permit

rapid bias recovery and video amplifier V2 to amplify the video signals. The unblanking channel unblanks the CRT for 500 mils in azimuth and 8,000 yards in range. This channel consists of azimuth blank V3A and blanking amplifier V3B.

Note Continuous reference in *b* below is made to figure 14, TM 9-1430-257-20 unless otherwise indicated

b. Detailed Theory.

(1) Positive acquisition video and marks signals applied at VIDEO connector J3 are coupled through capacitor C5 to the control grid of V2. These positive signals cause C5 to charge. The charge path is from ground through V2 when grid current flows and through the external circuit connected at J3. The negative grid bias voltage for V2 is developed across resistors R8 and R10. Crystal CR1 is a clamper for this voltage. Capacitor C6 shorts transient voltages to ground. Capacitor C5 discharges through CR1 and R10 when the signal tends to go negative from the bias level. If CR1 were not in the circuit, discharge would occur through resistors R9 and R10 to ground. The long time constant of this path would require considerable time for C5 to return to bias level. The long time constant would cause loss of the smaller video signals. With CR1 in the circuit, C5 discharges immediately. The input video signals are amplified and inverted by V2. Peaking coil L1 and resistor R11 in series form the plate load of V2. Peaking coil L1 improves high frequency response. It has practically no effect on the lower frequencies. The negative acquisition video and marks signals at the plate of V2 are applied directly to the cathode of the CRT. The result is intensity modulation of the CRT. Acquisition video and marks signals are always present at the cathode of the CRT but are not displayed until unblanking occurs.

(2) With no acquisition azimuth gate signal applied at connector J1 3, V3A conducts and current flows through resistors R4,

110

CONFIDENTIAL

R5, and R7 to ground. The plate load of V3A is essentially R4 since R5 and R7 are very small. Plate current of V3A causes a voltage drop across R4. Resistor R4 is also between the control grid and cathode of V3B. The voltage difference between grid and cathode is sufficient to cut off V3B. The +150 volts at the plate of V3B, during cutoff, is blocked from the CRT by capacitor C4.

(a) The acquisition azimuth gate at J1–3 is a triangular wedge atop a positive-going sine wave (A, fig. 35). This gate represents a predetermined 711-mil (40°) azimuth rotation of the acquisition antenna. When the gate is applied to the cathode of V3A, it cuts off V3A. Only a portion of the acquisition azimuth gate representing 533 mils azimuth is used to cut off V3A (B,
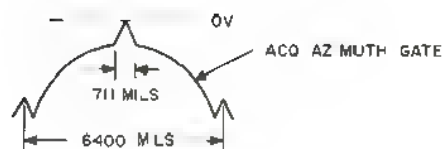
A. INPUT TO V3A
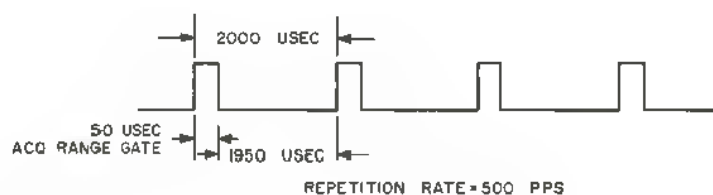
D. INPUT TO CATHODE V3B
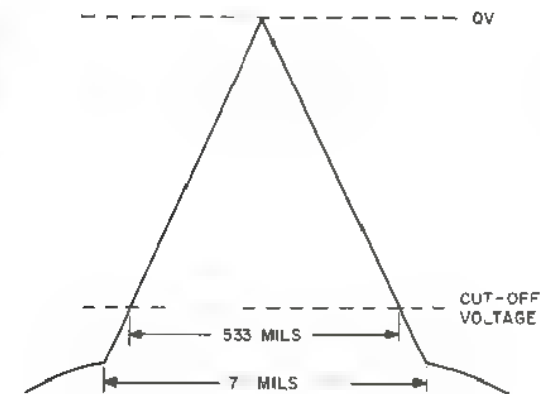
B. EXPANDED INPUT TO V3A
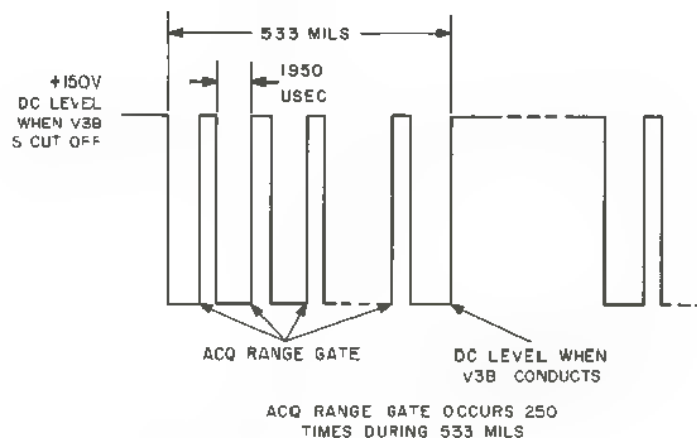
E. OUTPUT AT PLATE V3B
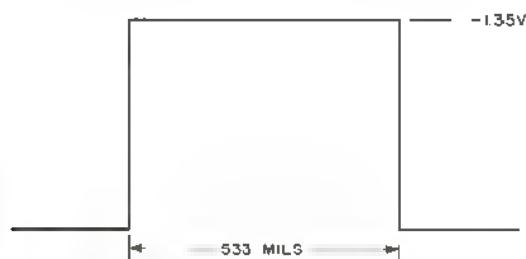
C. INPUT AT GRID V3B
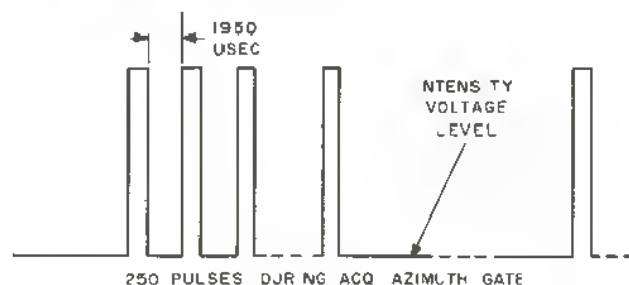
F. INPUT TO CONTROL GRID CRT

RA PD 468|43

Figure 35 (U). Precision video amplifier — waveforms.

111

fig. 35). The cutoff time of V3A is controlled by AZ BLANK ADJ variable resistor R2. Capacitor C2 at the control grid of V3A shorts transient voltages to ground. Capacitor C3 at the plate of V3A serves the same purpose. When V3A cuts off, the plate voltage increases. This increase in voltage is coupled directly to the control grid of V3B. The grid bias voltage of V3B becomes 1.35 volts (C, fig. 35) and V3B conducts.

(b) A positive acquisition range gate signal (D, fig. 35) at RANGE GATE connector J2 is coupled through capacitor C7 to the cathode of V3B. The acquisition range gate is a 50-microsecond pulse having a repetition rate of 500 pps. It appears approximately 250 times during the 533-mil (30°) acquisition azimuth gate and is of sufficient amplitude to cut off V3B. The signal at the plate of V3B is a combination of the two gates (E, fig. 35). The output waveshape is produced by the alternate conduction and cutoff of V3B during the acquisition azimuth gate. Capacitor C4 couples the signal (F, fig. 35) at the plate of V3B to the control grid of the CRT. The positive portion of this signal unblanks the CRT.

(3) A dc voltage from INTENSITY variable resistor R5 (fig. 10, TM 9–1430–257 20), a precision indicator front panel adjustment, is applied through connector J1-5 and resistor R12 to the control grid of the CRT. This voltage provides a dc level for the acquisition video and marks signals from V3B. The filaments of the CRT are at the same dc voltage as the cathode to prevent arcing. The high impedance of resistor R14 isolates signals at the plate of V2 from the filaments of the CRT. Decoupling networks are formed by resistor R15 and capacitor C1A, and resistor R13 and capacitor C1C.

44.1 (U). Precision Indicator 9139583

a. *General.*

(1) The precision indicator displays an enlarged sector of the plan-position indicator (PPI) presentation. This enlarged sector permits a more accurate analysis of target azimuth and range information than the PPI. The sector of the PPI displayed on the precision indicator cathode-ray tube represents 533 mils (approximately 30°) in azimuth and 25,000 yards in range. It is centered about the intersection of the flashing azimuth line and the range circle of the PPI display.

(2) The precision indicator contains four subassemblies listed in (a) through (d) below.

(a) Range sweep generator 9141066.

(b) Azimuth sweep generator mixer stage 7620604.

(c) Precision mark generator 9144718.

(d) Precision video amplifier 7620605.

b. *Functional Block Diagram Analysis.*

(1) The precision indicator (fig. 76, TM 9–1430–257–20/1) is composed of circuits shown in the functional block diagram in figure 35 1.

(2) The range sweep generator sends a trapezoidal range sweep pulse to the vertical deflection coils of the CRT to sweep the electron beam from the bottom to the top of the CRT screen. The input to the range sweep generator is the 152.4-microsecond acquisition range gate. The output range sweep pulse is 152.4 microseconds in duration and occurs at a repetition rate of either 400 or 500 pps, depending on whether the HIPAR or LOPAR is in use. The lower rate is for the HIPAR. The 152.4-microsecond sweep represents a 25,000-yard sector of the PPI display in range.

(3) The azimuth sweep generator mixer stage sends an azimuth sweep signal to the horizontal deflection coils of the CRT to sweep the electron beam across the screen of the CRT. The inputs to the azimuth sweep generator mixer stage are a 4-kc reference carrier and
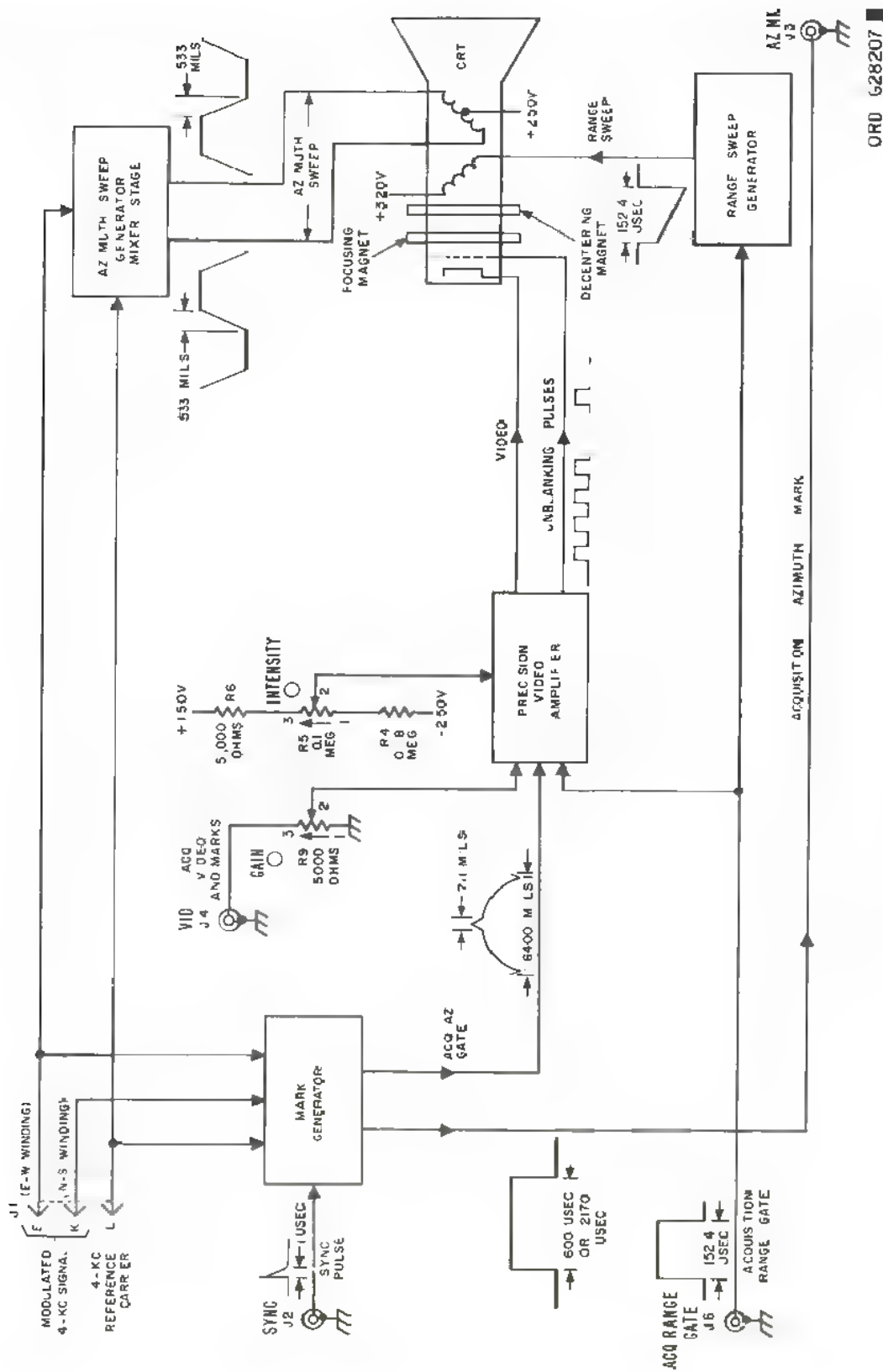
Figure 35.1 (U) Precision indicator – functional block diagram.

ORD 628207

a modulated 4-kc signal. The output is a severely clipped (truncated) sine wave with an unclipped sector equal to 533 mils (approximately 30°). This unclipped sector is practically linear and produces the horizontal sweep from left to right across the screen during the time the CRT is unblanked.

(4) The mark generator produces a 711-mil (approximately 40°) acquisition azimuth gate and a 1600 or 2170- microsecond acquisition azimuth mark. The duration of the mark depends on whether the HIPAR or LOPAR is in use. This long pulse is for the HIPAR. The acquisition azimuth gate is used to unblank the CRT for 533 mils of one acquisition antenna revolution. During each revolution of the acquisition antenna, the acquisition azimuth mark brightens one sweep on the PPI to produce the flashing azimuth line. The inputs to the precision mark generator are the sync pulse, the 4-kc reference carrier, and the two modulated 4-kc signals that are 90° out of phase.

(5) The precision video amplifier applies the acquisition video and marks to the CRT and also unblanks the CRT. The acquisition video and marks are always applied to the cathode of the CRT but are not displayed until the CRT is unblanked. The inputs to the precision video amplifier are the acquisition video and marks, INTENSITY dc voltage, the acquisition azimuth gate, and the 152 4-microsecond acquisition range gate. GAIN variable resistor R9 determines the amplitude of the acquisition video and marks. INTENSITY variable resistor R5 determines the dc level baseline of the unblanking pulses, which in turn determines the brightness of the presentations on the screen of the CRT. The acquisition azimuth gate and the 152.4-microsecond acquisition range gate are mixed to form the unblanking pulses.

(6) The CRT circuit includes the horizontal and vertical deflection coils, the

focusing magnet, and the decentering magnet. The azimuth sweep signal is applied to the horizontal deflection coils for sweeping the electron beam from left to right on the screen of the CRT. The range sweep pulse is applied to the vertical deflection coils for sweeping the beam from bottom to top.

(a) The focusing magnet is used to center the electron beam on the screen of the CRT. This magnet is cylindrical in shape with an adjustable shunt to vary the strength and configuration of the magnetic field. Electrons which are moving exactly on the axis of the magnetic field set up by the focusing magnet are not deflected. All other electrons are deflected by the magnetic field which produces inward radial accelerations to bring the electrons together at a common point. This common point is known as the focus point. The distance between the cathode and focus point is proportional to the intensity of the magnetic field which is controlled by the adjustable shunt. The adjustable shunt is adjusted so that the focus point is at the screen of the CRT. To correct for CRT element misalinements, a centering ring is provided on the focusing magnet to change the shape of the magnetic field. Altering the position of the centering ring changes the point where the electron beam strikes the screen of the CRT.

(b) The decentering magnet is used to return the electron beam to the bottom of the CRT screen. This magnet consists of two permanent bar magnets, two pole pieces, and two adjustable shunts. When the shunts are positioned close to the magnets, decreasing the air gaps, the magnetic field is decreased, which deflects the electron beam a slight amount. Increasing the air gaps increases the magnetic field, resulting in a greater deflection of the

electron beam. The shunts are normally adjusted to place the electron beam at the bottom of the screen on the CRT.

44.2 (U). Range Sweep Generator 9141066

a. General. The range sweep generator provides a range sweep pulse having a sawtooth current waveform to the vertical deflection coils of the cathode-ray tube in the precision indicator. This range sweep pulse generates a range sweep on the CRT screen

Note. Continuous reference in *b* and *c* below is made to figure 77, TM 9-1430-257 20 1 unless otherwise indicated.

b. Detailed Theory.

(1) The positive 152.4-microsecond acquisition range gate is applied through connector J1, coupled through capacitor C7, developed across resistor R21, and applied to the clipper circuit made up of crystal diode CR1 and resistor R26. Approximately 0.7 volt of bias for the clipper circuit is developed across resistor R3 and R4. Signals more negative than the bias level are clipped at the bias level. Positive signals above the bias level are not clipped but are applied directly to the cathode of trapezoidal sweep generator V1A. The bias level is above the level of noise which, if not eliminated, would create sweep jitter. Elimination of the noise results in a stabilized sweep on the precision indicator CRT.

(2) With no signal applied at connector J1, V1A conducts. Current flows from ground through resistors R4 and R3, V1A, and resistors R2 and R1 to the +150-volt supply. A large voltage drop is developed across R1 and R2 because of their large values. This makes the plate voltage of V1A slightly higher than the cathode voltage. Capacitor C1 charges to a voltage equal to the voltage across V1A and R3.

(a) Generator V1A cuts off when the positive acquisition range gate (A, fig. 35.2) is applied to the cathode. Capacitor C1 now charges along an RC curve determined by R4, R1,

R2, and C1, and the +150-volt supply. The time constant of this path is long compared to the 152.4-microsecond acquisition range gate. Therefore, C1 can charge for only a fraction of the RC time constant which results in a linear voltage rise at the plate of V1A. The amplitude of the voltage rise is determined by the setting of range adjust variable resistor R2. If R2 is shorted (brush arm fully clockwise), C1 charges faster because the circuit time constant is smaller. Capacitor C1 charges to a higher voltage than it would if R2 were in the circuit. When the positive acquisition range gate drops to zero, V1A conducts, and the low resistance of V1A and R3 provides a path for rapid discharge of C1. This results in a sharp negative-going trailing edge at the plate of V1A, and a sawtooth waveform is created at the plate of V1A.

(b) To create a trapezoidal waveform, it is necessary to provide a step at the leading edge of the sawtooth. A small portion of the acquisition range gate applied at J1 is developed across R4 and applied to C1. Capacitor C1 acts as a short circuit to this step voltage which is the leading edge of the trapezoidal wave-

A. ACQ RANGE GATE INPUT   B. PLATE V1A, V3 CONTROL GRID V2, V4, V5 CATHODE V1B

C. CONTROL GRID V3 PLATE V2, V4, V5   D. PLATE CURRENT V4, V5 FEEDBACK VOLTAGE TO CATHODE V2

ORD G28206

Figure 35.2 (U). Range sweep generator — waveforms.

form. The resultant waveform (B, fig. 35.2) at the plate of V1A is a series of trapezoidal voltages 152.4 microseconds wide.

(3) The trapezoidal voltages at the plate of V1A are applied directly to the control grid of voltage amplifier V2, where they are amplified and inverted. Amplifier V2 is a voltage amplifier with degenerative feedback in the cathode circuit. Resistor R17 can be considered as the cathode resistance of V2. Because of the small size of capacitor C6, R17 can be considered as being unbypassed. Capacitor C6 effectively short circuits the sharp rise time of the trapezoidal waveform, and no degenerative feedback is developed in the cathode circuit of V2. This action prevents the distributed capacitance in the circuits of power amplifiers V4 and V5 from affecting the trapezoid. The distributed capacitance would tend to distort the sharp rise time of the waveform. By removing the degenerative feedback during the sharp rise time, the gain of V2 is increased. This allows the distributed capacitance in the circuits of V4 and V5 to charge without distorting the waveform. Capacitor C2 and resistor R7 in the plate circuit of V2 prevent oscillations at high frequencies. Capacitor C3 couples the signal (C, fig. 35.2) from the plate of V2 to the control grid of V3, which is a conventional voltage amplifier. After amplification and inversion by V3, the signal (B, fig. 35.2) is coupled through capacitor C4 to the cathode of clamper V1B and the control grids of V4 and V5. Resistors R19 and R22 in the control grid circuits of V4 and V5 prevent parasitic oscillations.

(4) Power amplifiers V4 and V5 are operated in parallel to meet the current requirements of the output load. The plate load of V4 and V5 is the vertical deflection coils of the precision indicator CRT. Since considerable resistance in the coils prevent them from appearing as pure inductance, the output load must be treated as an RL circuit. To produce a sawtooth of current through an RL circuit, it is necessary to apply a trapezoidal voltage, which contains both square-wave and sawtooth-wave components. The square-wave component produces a linear current increase through the inductance of the coils, and the sawtooth-wave component produces a linear increase through the resistance. The plate current waveform (D, fig. 35.2) of V4 and V5 is a linear sawtooth waveform and the plate voltage waveform (C, fig. 35.2) is a trapezoidal waveform.

(5) The current in the cathode circuit of V4 and V5 may be considered as having two components, a plate current and a screen current. Since the screen current does not flow in the output load, it is desired that only voltages representing the plate current waveform of V4 and V5 be used for feedback to V2. To eliminate the screen current component, it is necessary to develop an inverse voltage to cancel the effect of the screen current. The screen current develops a voltage across resistors R23 and R27 that is fed through R17 to the cathode of V2. The cathode of V2 becomes more positive than the cathode of V4 when a positive pulse is applied to the control grid of V4. However, a rise in screen current at this time causes the junction of R18 and R20 to become more negative. The voltage drop across resistor R25 is reflected through resistor R20 causing the cathode of V2 to become more negative than the cathode of V4. Thus, the voltage developed across R25 is 180° out of phase with the voltage developed across R23 and R27. Cancelling the effect of screen current in this manner improves linearity of the sawtooth current waveform in the output load.

(6) Clamper V1B returns the control grids of V4 and V5 to a constant voltage level at the end of each trapezoi-

dal pulse. A constant bias voltage of approximately —83 volts is developed across resistors R12 and R13 and applied to the grid of V1B. Since the plate of V1B is connected to +150 volts through resistor R28 and the cathode of —250 volts through resistor R11, V1B will conduct during the quiescent period. Current flow through R11 and V1B provides a voltage at the cathode of V1B that is approximately —72 volts. Capacitor C4 is charged to the difference in potential between the plate of V3 and the cathode of V1B.

(a) The positive trapezoidal voltage at the plate of V3 is coupled through C4 to the cathode of V1B and the control grids of V4 and V5. This positive voltage on the cathode drives V1B toward cutoff. Because of the long time constant, the charge on C4 increases only a small amount during the trapezoidal pulse. Charge current flows from the plate of C4 connected to V3, through resistor R9, the +250-volt supply, ground, the —250-volt supply, and R11 to the other plate of C4. The time constant of this path is long compared with the trapezoidal pulse.

(b) The trailing edge of the trapezoidal pulse adds algebraically to the charge on C4 and drives the cathode of V1B negative. Clamper V1B conducts and discharges C4 rapidly to its quiescent value. The discharge path for C4 is from the plate connected to R11, through V1B, R28, the +150-volt supply, ground, and V3 to the other plate of C4. The discharge time is short and the cathode of V1B and control grids of V4 and V5 are returned rapidly to the quiescent value of —72 volts. This action insures that the negative extreme of the trapezoidal pulse to V4 and V5 is clamped at a fixed voltage level. During quiescence, current flowing in V4 and V5 and through the deflection coils always has the same value because the biasing voltage is always the same at this time. This causes the sweep on the CRT to always start from the same point.

44.3 (U). Azimuth Sweep Generator Mixer Stage 7620604

See paragraph 42.

44.4 (U). Precision Mark Generator 9144718

a. General. Precision mark generator 9144-718 produces two outputs: the acquisition azimuth gate produced by the gate channel and the acquisition azimuth mark produced by the mark channel. The acquisition azimuth gate is 711 mils (approximately 40°) in duration and is used for unblanking the precision indicator cathode-ray tube and for gating various other circuits of the acquisition radar system. The acquisition azimuth mark is a 1600-microsecond or 2170-microsecond pulse used to produce the flashing azimuth line on the plan-position indicator (PPI) once during each revolution of the acquisition antenna. It also provides the vertical line on the precision indicator and B scope indicator during alinement. The duration of the acquisition azimuth mark is selected for the acquisition radar being used. The shorter mark is for the LOPAR; the longer mark is for the HIPAR.

b. Detailed Theory. The theory of precision mark generator 9144718 (fig. 78, TM 9–1430–257 20/1) is the same as that given in paragraph 43, except that the azimuth mark is either 1600 or 2170 microseconds and paragraph 43b(2)(c) would read as follows: The square wave developed at the plate of V6A (E, fig. 35.3) is differentiated by capacitor C9 and resistors R25 and R26, which results in a sharp positive pip at the grid of monostable multivibrator V5A. Multivibrator V5A is normally cut off by the negative voltage at the grid developed by the voltage divider consisting of resistors R24 and R25 connected between the —250-volt supply and ground. The positive pip drives V5A into conduction. From the plate of V5A, a negative-going signal is coupled through capacitor C8 to the grid of monostable multivibrator V5B. The negative-going signal at the grid drives V5B to cutoff, resulting in a positive-going signal at the plate. The positive-going signal is coupled through capacitor C7
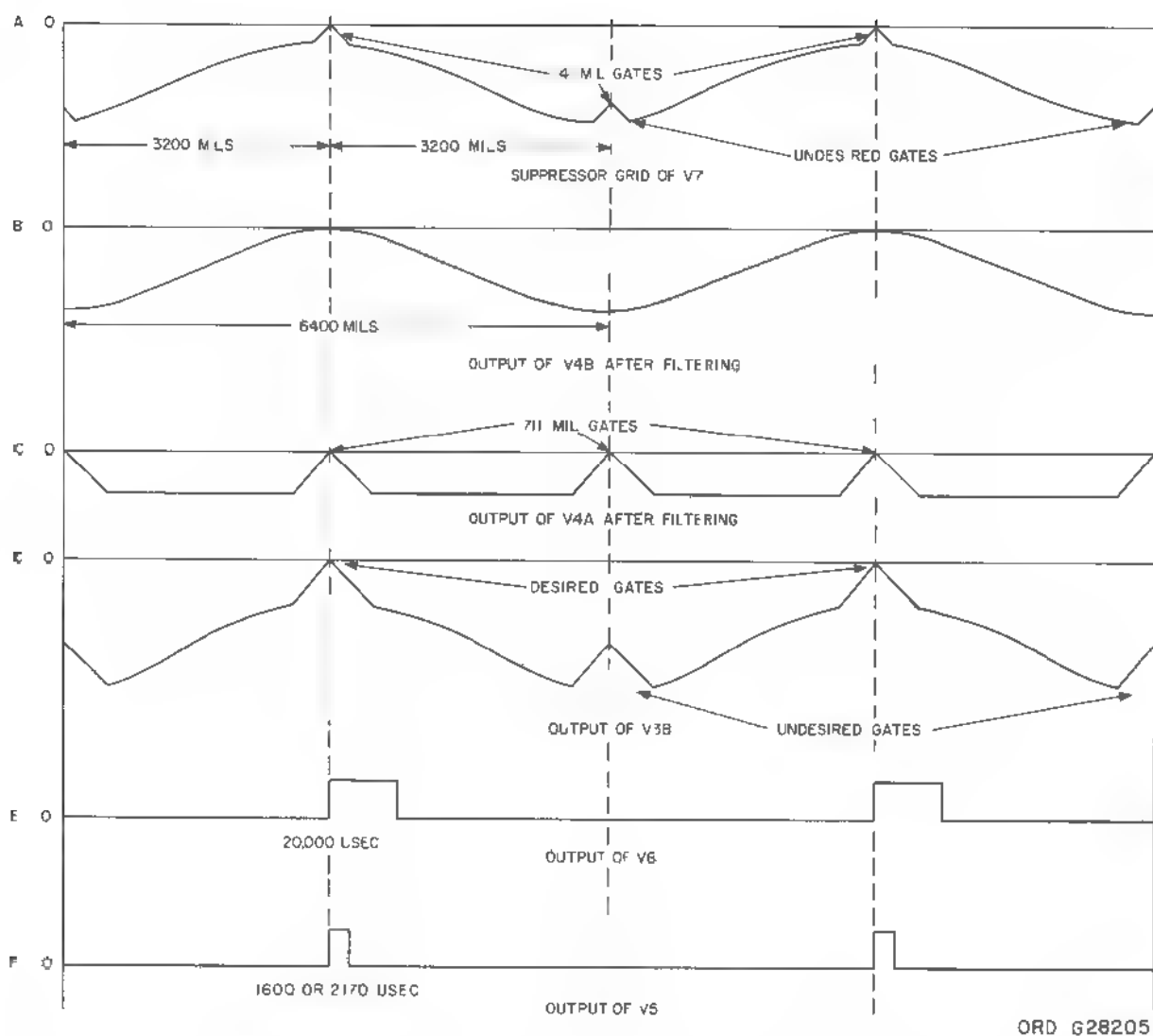
Figure 35.3 (U). Precision mark generator V3B through V7 - waveforms.

ORD G28205

back to the grid of V5A. The regenerative feedback causes conduction in V5A to increase rapidly. The feedback also assures quick recovery after the multivibrator cycle is complete. This results in a square-wave pulse with sharp leading and trailing edges A 1600-microsecond or 2170-microsecond positive-going square wave (F, fig. 35.3), the acquisition azimuth mark, appears at the cathode of V5A. The length of the azimuth mark is determined by the discharge time of capacitor C8 and resistor R30 plus variable resistor R32 or resistor R30 plus variable resistor R43. When RADAR SELECT switch S7 on the IFF control indicator is operated to LOPAR, HIPAR relay K1 on the precision mark generator is deenergized, and the 1600-microsecond acquisition azimuth mark is produced. The pulse length is determined by the discharge of C8 through resistor R30, MARK LENGTH LOPAR variable resistor R32, contacts 1 6 of relay K1, the +250-volt supply, ground, resistor R27, and V5A to the other plate of C8. When S7 is operated to HIPAR, relay K1 is energized and MARK LENGTH HIPAR variable resistor R43 is substituted for R32 in the discharge path. Due to the greater resistance of R43, the output pulse is lengthened to 2170 microseconds in the HIPAR mode.

44.5 (U). Precision Video Amplifier 7620605

See paragraph 44

45 (U). Acquisition Range Generator 8172913, 9007684

a. General. The acquisition range generator provides the acquisition radar presentation system with an acquisition range mark and an acquisition range gate. The acquisition range mark is a 0.5-microsecond pulse that appears on each sweep of the acquisition PPI. Because an acquisition range mark appears on each sweep, it generates a range circle on the PPI screen. The acquisition range marks also appear on the precision indicator as a horizontal line. The acquisition range gate is a 50-microsecond (8000-yard) positive pulse. This pulse is centered about the acquisition range mark. The acquisition range gate is utilized by the range sweep generator of the battery control console precision indicator to generate an 8000-yard range sweep.

Note Continuous reference in *b* and *c* below is made to figure 20, TM 9-1430 257-20 unless otherwise indicated.

b. Detailed Theory.

(1) *Phantastron delay circuit.* The phan-

tastron delay circuit consists of blocking diodes V1A and V1B, phantastron V2, cathode follower V3A, and associated circuit compounds. The circuit is used to produce an output pulse with a duration proportional to the control voltage tapped off range variable resistor R1, located externally on the target designate control-indicator.

(a) Phantastron V2 has a sharp suppressor-to-plate cutoff. During the quiescent period, the screen grid of V2 draws a sufficient amount of current through cathode resistor R11 to keep the suppressor grid negative with respect to the cathode and thereby keep the plate of V2 cut off. The plate of V2 is at the same voltage as the control voltage applied at connector P1-5 because the resistance of blocking diode V1A is negligible in comparison with the resistance of resistor R9. Since the control grid of V2 is returned to the +150-volt supply through a high resistance, it will draw sufficient current to keep

the control grid voltage essentially equal to the cathode voltage. The control voltage is applied from V1A to the plate of V2 and to the grid of V3A.

(b) The positive 1-microsecond preknock pulse (A, fig. 36) at connector J2, used to trigger the circuit, is applied directly to the plate of blocking diode V1B. Diode V1B conducts during the time the positive preknock pulse is present at the plate. The positive pulse appearing at the cathode of V1B is coupled directly to the suppressor grid of V2. This pulse brings the normally cutoff section of V2 into conduction. The gain of V3A is approximately unity. Therefore, the drop in plate voltage of V2 (B, fig. 36) is transmitted to the control grid of V2 (C, fig. 36) through V3A and C3. The plate current of V2 is thereby reduced. This reduction in plate current slows the voltage drop at the plate and brings it to a standstill at a point where the control grid is slightly above cutoff. The drop in the control grid voltage, in conjunction with the action of the plate, lowers the cathode voltage of V2 to approximately zero and prevents the screen grid from drawing current. The suppressor grid is no longer biased negatively with respect to the cathode; consequently, the plate of V2 will continue to draw current after the expiration of the trigger pulse.

(c) The circuit action described takes place instantaneously. It results in abrupt voltage drops at the plate, control grid, and cathode of V2. The voltage drop at the cathode of V2 forms the leading edge of the negative phantastron delay pulse output (D, fig. 36). This initial switching action is followed by a period of relative stability, during which the actual timing wave is generated by discharging C3.

(d) During the stable period following the initial switching, the high negative feedback in V2 is the result of the plate-to-control grid coupling through V3A. Any further change in the control grid voltage of V2 sets up currents in the circuit to oppose such a change. Control grid voltage increases gradually to quiescence as C3 discharges through resistor R12, RATE variable resistor R13, and resistor R14 to the +150-volt supply, and from the −250-volt supply through resistors R51 and R15 to the other side of C3. This current discharges C3 at a constant rate, resulting in a linear change of voltage across C3.

(e) The rate of discharge and thus the slope of the voltage drop (B, fig. 36) at the plate of V2 is proportional to the charge in C3. The setting of R13 determines the slope of discharge (fig. 37). The rate of discharge with a constant slope is proportional to the variations in plate voltage of V2 (fig. 38) caused by moving the brush arm of acquisition range variable resistor R1 on the target designate control indicator.

(f) When the discharge of C3 has progressed to a certain point, a second switching action takes place. At this point, the plate current of V2 has reached a point where an increase in the control grid voltage no longer causes an increase in place current. When this occurs, the control grid voltage rises (C, fig. 36), since there is no longer enough negative feedback through V3A and C3 to keep the control grid voltage of V2 constant. As the control grid voltage of V2 rises, screen grid current increases. This action takes place rapidly and stops when the screen grid of V2 is drawing enough current to raise the cathode voltage sufficiently to cause the suppressor grid to cut off the plate. The control grid of V2 draws current and quickly recharges C3. The charge path of this current is from one plate of C3 through

CONFIDENTIAL

A - INPUT PREKNOCK PULSE AT J2

B - PHANTASTRON DELAY PULSE AT PLATE OF V2

C - PHANTASTRON DELAY PULSE AT CONTROL GRID OF V2

D - PHANTASTRON DELAY PULSE AT CATHODE OF V2

E - DELAYED TRIGGER PULSE AT PLATE OF V3B

50 USEC   F - SQUARE-WAVE OUTPUT AT PLATE OF V4A

50 USEC   G - SQUARE-WAVE ACQ RANGE GATE OUTPUT AT J1

H - SQUARE-WAVE OUTPUT AT PLATE OF V5B

J - 25-MICROSECOND DELAY PULSE AT GRID OF V6A

25 USEC   K - SQUARE-WAVE OUTPUT AT PLATE OF V6A

L - SQUARE-WAVE OUTPUT AT PLATE OF V6B

M - NEGATIVE PIP AT PLATE OF V7

N - POSITIVE PIP ACQ RANGE MARK OUTPUT AT J3

VARIABLE WITH RANGE

RA PD 468144

Figure 36. (U) Acquisition range generator—voltage waveforms in relation to time.
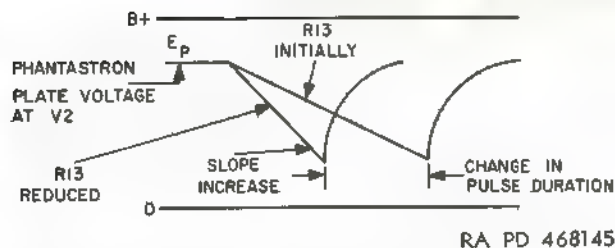
Figure 37 (U) Acquisition range generator—effect of changing rate variable resistor R13.

V3A, to the +250-volt supply, from ground through R11, cathode-to-control grid of V2 to the other plate of C3. As C3 is recharged, the voltages at the cathode and grid of V3A rise. This rise causes the voltage at the plate of V2 to return to the control voltage applied through P1 5. The circuit remains quiescent until the next positive trigger pulse is applied to the suppressor grid of V2.

(g) The purpose of V1B is to isolate the suppressor grid of V2 from the low impedance output of the acquisition-track synchronizer, except when the preknock pulse is applied.

(h) Calibration of the acquisition range generator is accomplished by adjustment of R13 and ZERO variable resistor R2. Variable resistor R2 is connected in series with resistor R3 to ground at one end and to connector P1 3 at the other end. The setting of R2 determines the control voltage at P1 5 when range variable resistor R1 (B3, fig. 18, TM 9–1430–257 20) on the target designate control-indicator is set to minimum range.

(i) The operating voltage of the cathode of V3A varies with the control voltage at P1–5 and may become as high as 140 volts at long ranges. Since the maximum allowable heater-to-cathode voltage for V3 is 90 volts, a positive bias of +75 volts is applied to the heater from the voltage divider consisting of resistors R7 and R8, thus keeping the heater-to-cathode voltage within allowable limits. For this reason, V3 is
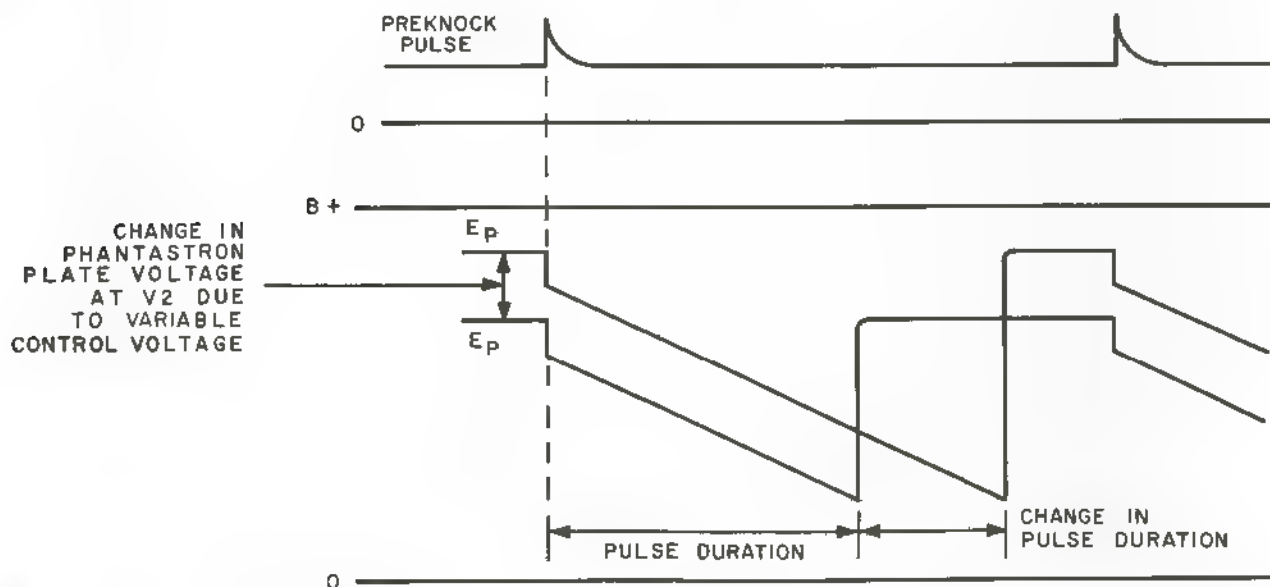
RA PD 468146

Figure 38 (U) Acquisition range generator—effect of changing plate voltage of V2.

CONFIDENTIAL

connected to a separate filament transformer winding.

(2) *Acquisition range gate channel.* The acquisition range gate channel is triggered by the trailing slope of the phantastron delay pulse and generates a positive 50-microsecond pulse. This channel consists of differentiating and clipping amplifier V3B, monostable multivibrator V4A and V4B, pulse shaping cathode follower V5A, and associated circuit components.

(*a*) During quiescence, cathode resistor R16 develops sufficient bias to operate V3B slightly above cutoff. The leading edge of the negative phantastron delay pulse from the cathode of V2 drives the grid of V3B negative. Since quiescent operation of V3B is slightly above cutoff, the lowering of the grid voltage produces a small rise in plate voltage. Amplifier V3B returns to quiescent operation as capacitor C2 becomes discharged by current flow from one plate of C2 through resistor R17, coupled through capacitor C5, resistor R18, to the + 150-volt supply, and from ground through R11 to the other plate of C2.

(*b*) The trailing edge of the phantastron delay pulse attempts to drive the grid of V3B positive. The currents resulting from this are such that the change is counteracted and the grid remains at zero voltage. The voltage across C2 must increase as rapidly as the voltage at the cathode of V2 increases. This requires that a charging current, proportional to the positive going trailing edge of the cathode voltage of V2, be coupled through C2. The charging path for C2 is from ground, through R11 to one plate of C2, and from the other plate of C2 through R17, coupled through C5, R18, and to the + 150-volt supply. Since the positive-going trailing edge of the phantastron delay pulse

is steep, a large voltage rise appears initially on the grid of V3B, which drives V3B into conduction causing a sharp instantaneous drop in plate voltage of V3B. This sharp drop in plate voltage is coupled through the degenerative feedback circuit, consisting of C5 and R17, to the grid of V3B, immediately cutting off conduction in V3B. This causes an instant rise in plate voltage to a small positive peak above the quiescent point; the voltage at the plate then immediately returns to quiescence. Since the voltage across C5 cannot change instantaneously, the small positive peak of the output pulse is due to the addition of voltages across C5 and R17 which are in parallel with V3B. The sudden drop and rise of plate voltage at V3B results in a sharp negative pip output (E, fig. 36). This delayed trigger pulse is coupled through capacitor C4 and crystal diode CR1 to the grid of monostable multivibrator V4A.

(*c*) Crystal diode CR1 isolates the input to V4A from the low output impedance of V3B, except for the duration of the negative delayed trigger pulse, which triggers the multivibrator.

(*d*) During quiescence, preceding the negative delayed trigger pulse, V4A is conducting heavily since its grid is returned to the + 250-volt supply. The cathode voltage developed across resistor R27, by the conduction of V4A, keeps monostable multivibrator V4B biased beyond cutoff. The delayed trigger pulse cuts off V4A and enables V4B to conduct; 50 microseconds later the circuit returns to quiescence. GATE LENGTH variable resistor R20 in the discharge path of capacitor C7 is adjusted for a pulse duration of 50 microseconds, which provides a range gate of 8,000 yards. Since V4A is cutoff for 50 microseconds, a positive square-wave pulse (F, fig. 36), 50 microseconds in duration, is coupled

CONFIDENTIAL

from its plate. The leading edge of this 50-microsecond square-wave pulse is in time coincidence with the trailing edge of the phantastron delay pulse. The square-wave output of V4A is coupled through capacitor C10 and resistor R33 to the grid of pulse shaping cathode follower V5B.

(e) Cathode follower V5B performs the function of squaring the square-wave pulse by baseline clipping and limiting and providing a low-impedance output for the range gate. Cathode follower V5B is biased below cutoff by the voltage divider consisting of resistor R31 and R32, which provides baseline clipping. Resistor R33 in the grid circuit of V5B provides grid current limiting. The square-wave acquisition range gate output (G, fig. 36) is coupled from the cathode of V5B to RG. GATE connector J1

(3) *Acquisition range mark channel.* The acquisition range mark channel is triggered by the leading edge of the square-wave pulse generated by V4A and provides a positive pip 25 microseconds later. This channel consists of the delay circuit composed of network driver V5A range mark, delay network Z1, and pulse forming triode V6A; baseline clipping amplifier V6B; differentiating and clipping amplifier V7; and associated circuit components.

(a) The square-wave output of V4A is coupled through capacitor C12 to the grid of V5A. Network driver V5A is held cut off in its quiescent state by a fixed bias obtained from the voltage divider composed of resistors R36 and R37. The leading edge of the positive 50-microsecond square-wave pulse at the plate of V4A raises the grid of V5A above cutoff. The conduction of V5A continues for 50 microseconds, producing a 50-microsecond square wave (H, fig. 36) at terminals 3-4 of delay network Z1. The capacitors of

Z1 are charged to +150 volts during the quiescent period. The voltage across these capacitors cannot change instantaneously, and all the negative voltage must appear across the inductor of Z1. Therefore, the end of the inductor connected to terminal 2 of Z1 is negative with respect to ground by an amount equal to the drop in plate voltage of V5A. Network Z1 is a shock-excited LC series resonant circuit. The circuit constants are chosen so the period of one-fourth cycle is 25 microseconds. The voltage (J, fig. 36) at terminal 2 of Z1 is, therefore, driven to maximum negative at the start of the square wave and rises toward ground for 25 microseconds. At the end of this time, pulse forming triode V6A, which was cut off by the negative 25-microsecond voltage across the inductor, conducts again. When terminal 2 of Z1 and the grid of V6A attempt to go positive, as this oscillatory circuit would require, the grid of V6A draws current and dampens further oscillation. The inductance of Z1 is adjusted by the range mark delay variable inductor so that normally conducting V6A is cut off for 25 microseconds.

(b) Because V6A is cut off for the first 25 microseconds, a positive 25-microsecond square wave (K, fig. 36) appears at its plate; only the trailing edge is of interest. The trailing edge of the square wave is a sharp negative-going voltage because the plate resistance of V6A is much lower than the plate load resistance of R40 at conduction. This ratio causes V6A to appear as a short circuit as soon as conduction begins, resulting in a sharp trailing edge of the positive square wave at the plate of V6A. The 25-microsecond square-wave pulse at the plate of V6A is coupled through capacitor C14 to the grid of V6B.

(c) Baseline clipping amplifier V6B in-

verts and squares the 25-microsecond square-wave pulse. Amplifier V6B is biased below cutoff by the voltage divider composed of resistors R41 and R42. The positive square wave is clipped along the baseline and a negative 25-microsecond square wave (L, fig. 36) appears at the plate of V6B.

(d) The plate signal of V6B is differentiated at the control grid of differentiating and clipping amplifier V7 by the RC circuit composed of capacitor C16 and resistor R46. This RC circuit has a time constant that is small compared with the duration of the pulse. It differentiates the negative square wave developed at the plate of V6B; for, when the plate voltage drops, the voltage at the control grid of V7 drops momentarily and returns to ground potential rapidly as C16 discharges. The plate voltage of V6B rises sharply 25 microseconds later; the control grid of V7 rises momentarily and returns rapidly to ground potential as C16 charges. A negative pulse results at the control grid of V7, corresponding to the leading edge of the acquisition range gate, and a positive pulse corresponding to the delay established by Z1 Since V7 is biased near cut-off due to the large cathode resistance of resistor R50, the negative pulses are eliminated. The positive pulses produce heavy surges of plate current, which result in negative voltage pips (M, fig. 36) appearing at the plate of V7. Transformer T1 is connected so that the output pulse (N, fig. 36) at RG MK connector J3 is positive. This pulse is transmitted to the PPI and to the video and mark mixer as the acquisition range mark.

c. *Acquisition Range Generator 9007684.* Acquisition range generator 9007684 is similar to acquisition range generator 8172913. Acquisition range generator 9007684 differs in that it extends the range of the PPI by providing a longer time delay in the phantastron circuit and by increasing the limits of allowable

error at maximum ranges. Values of C3 and R13 were increased to provide a longer RC time constant, producing a longer phantastron delay pulse generated by discharging C3.

45.1 (U). Acquisition Range Generator 9143997

a. *General.* The acquisition range generator provides the acquisition radar presentation system with an acquisition range mark and an acquisition range gate. The acquisition range mark is a 0.5-microsecond pulse that appears on each sweep of the acquisition PPI. Because an acquisition range mark appears on each sweep, it generates a range circle on the PPI screen. The acquisition range marks also appear on the precision indicator and B scope indicator as a horizontal line during alinement. The acquisition range gate is a 152.4-microsecond (25,000-yard) positive pulse, centered about the acquisition range mark. The acquisition range gate is utilized by the range sweep generator of the precision indicator to generate a 25,000 yard range sweep.

Note. Continuous reference in b and c below is made to figure 80, TM 9–1430–257–20/1 unless otherwise indicated.

b. *Detailed Theory.*

(1) *Phantastron delay circuit* The phantastron delay circuit consists of blocking diodes V1A and V1B, phantastron V2, cathode follower V3A, and associated circuit components. The circuit is used to produce a delayed output pulse with a delay proportional to the control voltage tapped off range variable resistor R1, located externally on the target designate control-indicator.

(a) Phantastron V2 has a sharp suppressor-to-plate cutoff During the quiescent period, the screen grid of V2 draws sufficient current through cathode resistor R11 to keep the suppressor grid negative with respect to the cathode and thereby keep the plate of V2 cut off. The plate of V2 is at the same voltage as the control voltage applied at connector P1–5 because the resistance of blocking diode V1A is negligible in comparison with the re-

sistance of resistor R9. Since the control grid of V2 is returned to the +150-volt supply through a high resistance, it will draw sufficient current to keep the control grid voltage essentially equal to the cathode voltage.

(*b*) The positive 1-microsecond preknock pulse (A, fig. 38.1) at connector J2 is applied directly to the plate of blocking diode V1B. Diode V1B conducts while the positive preknock pulse is present at the plate. The positive pulse at the cathode of V1B is coupled directly to the suppressor grid of V2 and causes V2 to conduct. The drop in plate voltage of V2 (B, fig. 38.1) through cathode follower V3A and capacitor C3 is transmitted to the control grid of V2. The drop in the control grid voltage reduces the plate current and lowers the cathode voltage of V2 to approximately zero. This prevents the screen grid from drawing current. The suppressor grid is no longer biased negatively with respect to the cathode; consequently, the plate of V2 will continue to draw current after the expiration of the trigger pulse.

(*c*) The circuit action described takes place instantaneously. It results in abrupt voltage drops at the plate, control grid, and cathode of V2. The voltage drop at the cathode of V2 forms the leading edge of the output (D, fig. 38.1). This initial switching action is followed by a period of relative stability, during which the actual timing wave is generated by discharging C3.

(*d*) During the stable period following the initial switching, the high negative feedback in V2 is the result of the plate-to-control grid coupling through V3A. Any further change in the control grid voltage of V2 sets up currents in the circuit to oppose such a change. Control grid voltage increases gradually to quiescence as C3 discharges through resistor R12, RATE variable resistor R13, and resistor R14 to the

+150-volt supply, ground, the —250-volt supply, and resistors R51 and R15 to the other side of C3. This current discharges C3 at a constant rate, resulting in a linear change of voltage across C3.

(*e*) The rate of discharge and thus the slope of the voltage drop (B, fig. 38.1) at the plate of V2 is proportional to the charge in C3. The setting of R13 determines the slope of discharge (fig. 37). The rate of discharge with a constant slope is proportional to the variations in plate voltage of V2 (fig. 38) caused by moving the brush arm of acquisition range variable resistor R1 on the target designate control-indicator.

(*f*) When the discharge of C3 has progressed to a certain point, a second switching action takes place. At this point, the plate current of V2 has reached a value where an increase in the control grid voltage no longer causes an increase in plate current. When this occurs, the control grid voltage rises (C, fig. 38.1), since there is no longer negative feedback through V3A and C3 to keep the control grid voltage of V2 constant. As the control grid voltage rises, screen grid current increases. This action takes place rapidly and stops when the screen grid of V2 is drawing enough current to raise the cathode voltage sufficiently to cause the suppressor grid to cut off the plate. The control grid of V2 draws current and quickly recharges C3. The charge path of this current is from one plate of C3 through V3A, to the +250-volt supply, ground, R11, and cathode-to-control grid of V2 to the other plate of C3. As C3 is recharged, the voltages at the cathode and grid of V3A rise. This rise causes the voltage at the plate of V2 to return to the control voltage applied through P1-5. The circuit remains quiescent until the next positive trigger pulse is applied to the suppressor grid of V2.

(*g*) The purpose of V1B is to isolate the

A – INPUT PREKNOCK PULSE AT J2

B – PHANTASTRON DELAY PULSE AT PLATE OF V2

C – PHANTASTRON DELAY PULSE AT CONTROL GRID OF V2

D – PHANTASTRON DELAY PULSE AT CATHODE OF V2

E – DELAYED TRIGGER PULSE AT PLATE OF V3B

152.4 USEC

F – SQUARE-WAVE OUTPUT AT PLATE OF V4A

152.4 USEC

G – SQUARE WAVE ACQ RANGE GATE OUTPUT AT J1

H – SQUARE-WAVE OUTPUT AT PLATE OF V5B

J – 76-MICROSECOND DELAY PULSE AT GRID OF V6A

76 USEC

K – SQUARE-WAVE OUTPUT AT PLATE OF V6A

L – SQUARE-WAVE OUTPUT AT PLATE OF V6B

M – NEGATIVE PIP AT PLATE OF V7

N – POSITIVE PIP ACQ RANGE MARK OUTPUT AT J3

VARIABLE WITH RANGE
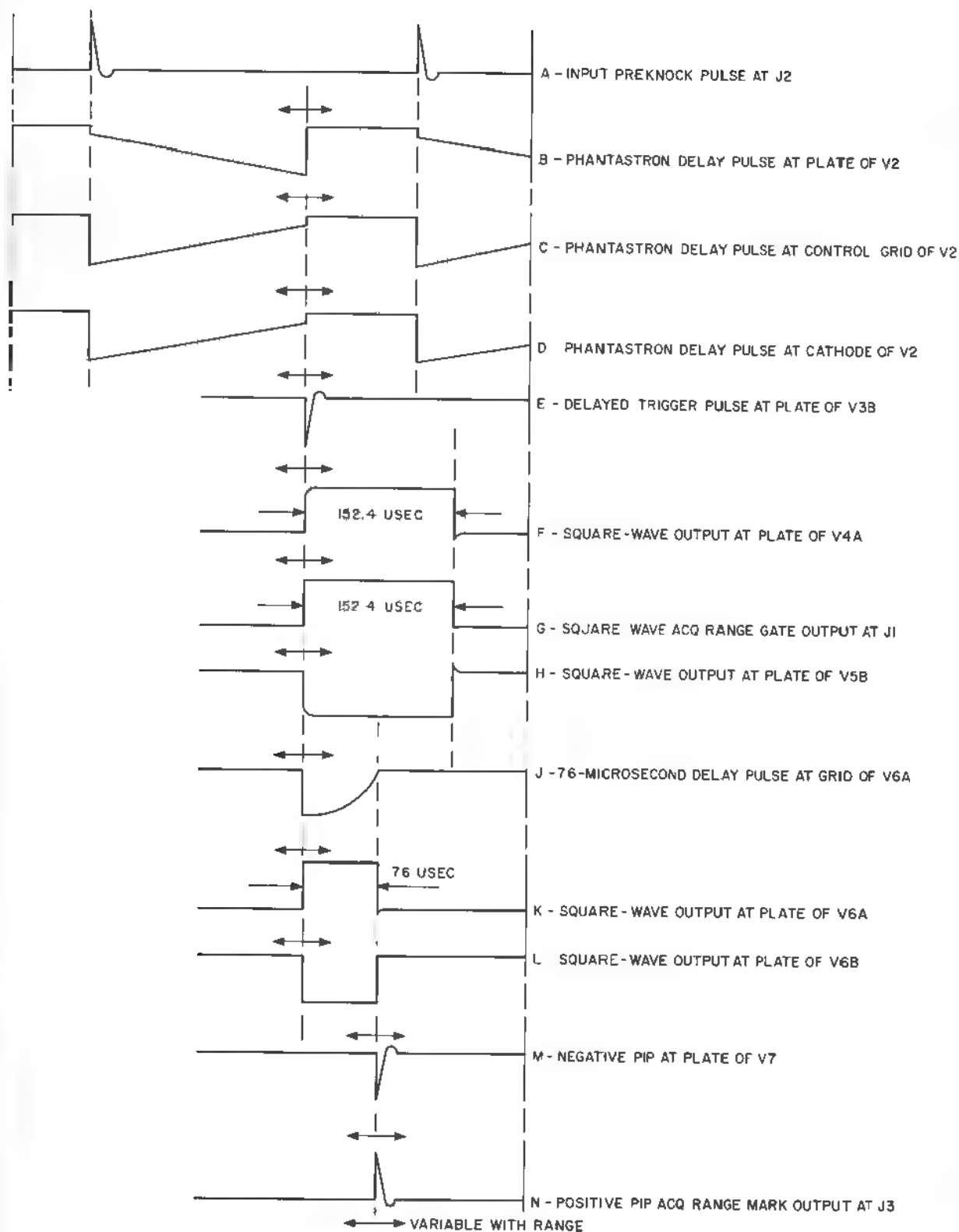
ORD G28247

Figure 38.1 (U). Acquisition range generator voltage waveforms in relation to time.

118.2

suppressor grid of V2 from the low impedance output of the acquisition-track-synchronizer, except when the preknock pulse is applied.

(h) Calibration of the acquisition range generator is accomplished by adjustment of R13 and ZERO variable resistor R2. Variable resistor R2 is connected in series with resistor R3 to ground at one end and to connector P1–3 at the other end. The setting of R2 determines the control voltage at P1–5 when range variable resistor R1 on the target designate control-indicator is set to minimum range.

(i) The operating voltage of the cathode of V3A varies with the control voltage at P1–5 and may become as high as 140 volts at long ranges. Heater-to-cathode voltage for V3 is 90 volts, a positive reference of +75 volts is applied to the heater from the voltage divider consisting of resistors R7 and R8, thus keeping the heater-to-cathode voltage within allowable limits. For this reason, V3 is connected to a separate filament transformer winding.

(2) *Acquisition range gate channel.* The acquisition range gate channel is triggered by the trailing edge of the phantastron delay pulse and generates a positive 152.4-microsecond pulse. This channel consists of differentiating and clipping amplifier V3B, monostable multivibrator V4A and V4B, pulse shaping cathode follower V5A, and associated circuit components.

(a) During quiescence, cathode resistor R16 develops sufficient bias to hold V3B slightly above cutoff. The leading edge of the negative phantastron delay pulse from the cathode of V2 drives the grid of V3B negative. Lowering the grid voltage produces a small rise in plate voltage. Amplifier V3B returns to quiescent operation as positive feedback coupled through capacitor C5 and resistor R17 to the control grid counteracts the negative pulse.

(b) The trailing edge of the phantastron delay pulse tends to drive the grid of V3B positive. The voltage across C2 must increase as rapidly as the voltage at the cathode of V2 increases. This requires that a charging current, proportional to the positive-going trailing edge of the cathode voltage of V2, be coupled through C2. The charging path for C2 is from ground, through R11 to one plate of C2, and from the other plate of C2 through R17, coupled through C5 and R18, and to the +150-volt supply. Since the positive-going trailing edge of the phantastron delay pulse is steep, a large voltage appears initially on the grid of V3B, which drives V3B into conduction causing an instantaneous drop in the plate voltage of V3B. This drop in plate voltage is coupled through the degenerative feedback circuit consisting of C5 and R17 to the grid of V3B, immediately cutting off conduction in V3B. This causes an instant rise in the plate voltage to a small positive peak above the quiescent point; the voltage at the plate then immediately returns to quiescence. The small positive peak of the output pulse is due to the addition of voltages across C5 and R17 which are in parallel with V3B. The sudden drop and rise of the plate voltage at V3B results in a sharp negative pip output (E, fig. 38.1). This delayed trigger pulse is coupled through capacitor C4 and crystal diode CR1 to the grid of V4A.

(c) Crystal diode CR1 isolates the input to V4A from the low output impedance of V3B, except for the duration of the negative delayed trigger pulse, which triggers V4A.

(d) During quiescence, V4A is conducting heavily since its grid is returned to the +250-volt supply. The cathode voltage developed across resistor R27 keeps V4B biased beyond cutoff. The delayed trigger

pulse cuts off V4A and enables V4B to conduct; 152.4 microseconds later the circuit returns to quiescence. GATE LENGTH variable resistor R20 in the discharge path of capacitor C7 is adjusted for a pulse duration of 152.4 microseconds, which provides a range gate of 25,-000 yards. Since V4A is cut off for 152.4 microseconds, a positive square-wave pulse (F, fig. 38.1) is coupled from its plate. The leading edge of this square-wave pulse is in time coincidence with the trailing edge of the phanstrom delay pulse. The square-wave output of V4A is coupled through capacitor C10 and resistor R33 to the grid of V5B.

(e) Cathode follower V5B performs the function of squaring the square-wave pulse by baseline clipping and limiting and providing a low-impedance output for the range gate. Cathode follower V5B is biased below cutoff by the voltage divider consisting of resistors R31 and R32, which provides baseline clipping. Resistor R33 in the grid circuit of V5B provides grid current limiting. The square-wave acquisition range gate output (G, fig. 38 1) is coupled from the cathode of V5B to RG. GATE connector J1.

(3) *Acquisition range mark channel.* The acquisition range mark channel is triggered by the leading edge of the square-wave pulse generated by V4A and provides a positive pip 76 microseconds later. This channel consists of the delay circuit composed of network driver V5, range mark delay network Z1, capacitor C19, and pulse-forming triode amplifier V6A; baseline clipping amplifier V6B; differentiating and clipping amplifier V7; and associated circuit components.

(a) The square-wave output of V4A is coupled through capacitor C12 to the grid of V5A. Network driver V5A is held cut off by a fixed bias obtained from the voltage divider composed of resistors R36 and

R37. The leading edge of the positive 152.4-microsecond square-wave pulse at the plate of V4A raises the grid of V5A above cutoff. The conduction of V5A produces a 152.4-microsecond square wave (H, fig. 38.1) at terminals 3 and 4 of delay network Z1. Capacitor C19 and the capacitors of Z1 are charged to +150 volts during the quiescent period. The voltage across these capacitors cannot change instantaneously, and all the negative voltage must appear across the inductor of Z1. Therefore, the end of the inductor connected to terminal 2 of Z1 is negative with respect to ground by an amount equal to the drop in plate voltage of V5A. Network Z1 is a shock-excited LC series resonant circuit. The circuit constants are chosen so the period of one-fourth cycle is 76 microseconds. The voltage (J, fig. 38.1) at terminal 2 of Z1 is, therefore, driven to maximum negative at the start of the square wave and rises toward ground for 76 microseconds. At the end of this time, V6A, which was cut off by the negative voltage across the inductor, conducts again. When terminal 2 of Z1 and the grid of V6A attempt to go positive, as the oscillatory circuit would require, the grid of V6A draws current and dampens further oscillation. The inductance of Z1 is adjusted by the range mark delay variable inductor so that normally conducting V6A is cut off for 76 microseconds.

(b) Because V6A is cut off for the first 76 microseconds, a positive square wave (K, fig. 38.1) appears at its plate; only the trailing edge is of interest. The trailing edge of the square wave is a sharp negative-going voltage because the plate resistance of V6A is much lower than the plate load resistance of R40 at conduction. This ratio causes V6A to appear as a short circuit as soon as conduction begins, resulting in

a sharp trailing edge of the positive square wave at the plate of V6A. The 76-microsecond square-wave pulse at the plate of V6A is coupled through capacitor C14 to the grid of V6B.

(c) Baseline clipping amplifier V6B inverts and squares the 76-microsecond square-wave pulse. Amplifier V6B is biased below cutoff by the voltage divider composed of resistors R41 and R42. The positive square wave is clipped along the baseline and a negative 76-microsecond square wave (L, fig. 38.1) appears at the plate of V6B.

(d) The plate signal of V6B is differentiated at the control grid of V7 by the RC circuit composed of capacitor C16 and resistor R46. This RC circuit has a time constant that is small compared with the duration of the pulse. It differentiates the negative square wave developed at the plate of V6B: for, when the plate voltage drops, the voltage at the control grid of V7 drops momentarily and returns to ground potential rapidly as C16 discharges. The plate voltage of V6B rises sharply 76 microseconds later; the control grid of V7 rises momentarily and returns rapidly to ground potential as C16 charges. A negative pulse results at the control grid of V7, corresponding to the leading edge of the acquisition range gate, and a positive pulse corresponding to the delay established by Z1. Since V7 is biased near cutoff due to the large cathode resistance of resistor R50, the negative pulses have no effect. The positive pulses produce heavy surges of plate current, which result in negative voltage pips (M, fig. 38.1) appearing at the plate of V7. Transformer T1 is connected so that the output pulse (N, fig 38.1)

at RG. MK. connector J3 is positive. This pulse is transmitted to the PPI and to the video and mark mixer as the acquisition range mark

46 (U). Low-Power Servo Amplifier 7614253

a. General. The low-power servo amplifier receives 400-cps error signals and converts them into corresponding driving power necessary to drive a motor-generator of servo systems. The low-power servo amplifier has high gain, a nonvarying phase characteristic, and a low noise level at 400 cps. At maximum signal amplitude, the power output is 10 watts

b. Detailed Theory. The low-power servo amplifier (fig. 19, TM 9-1430-257-20) contains two-stage voltage amplifiers V1A and V1B; driver amplifiers V2A and V2B; power amplifiers V3 and V4; output transformer T1; bridged-T network composed of resistors R6 and R7 and capacitors C2 and C3; and associated circuit components.

(1) *Voltage amplifiers V1A and V1B.* A 400-cps error signal is applied to connector P1-3 which is connected directly to the grid of voltage amplifier V1A. The bias applied to the grid of V1A is developed by the voltage divider composed of resistors R2, R3, and R8. The bias applied to the grid of voltage amplifier V1B is developed by the voltage divider composed of resistors R4, R5, and R1. During dynamic operation, the bias connection causes degenerative current feedback from V1B to V1A. If the plate current of V1B increases, the voltage across cathode resistor R8 increases, making the cathode of V1B more positive. The voltage rise on the cathode of V1B is fed back to the grid of V1A through R3, causing the grid of V1A to go more positive. This rise in grid voltage of V1A causes an increase in plate current, thereby causing a drop in plate voltage of V1A. Capacitor C1 couples this drop in plate voltage of V1A to the grid of

V1B, which results in reduction of current through V1B. Thus, the degenerative current feedback counteracts any increase in plate current of V1B, causing the plate current of V1B to remain essentially constant. Consequently, the effective output impedance is high, so that V1A and V1B may be regarded as a constant current generator.

(2) *Driver amplifiers V2A and V2B.*

(a) The 400-cps plate signal from V1B is coupled through capacitor C3 to the grid of driver amplifier V2A. Driver amplifiers V2A and V2B are coupled by common cathode resistor R10. When V2A is increasing in conduction the voltage drop across R10 goes positive, causing V2B conduction to decrease, which results in paraphrase amplifier outputs at the plates of V2A and V2B. The two output voltages of opposite phase are necessary for driving power amplifiers V3 and V4. Amplifier V2A inverts the signal and increases its amplitude to the desired level. Amplifier V2B amplifies it to the same level as obtained from V2A, but of opposite polarity. The grids of V2A and V2B are at circuit ground potential. Due to the symmetry of both stages, the quiescent currents of V2A and V2B are nearly equal. The two quiescent currents add in R10 and produce a drop across R10 sufficient to keep the cathodes at a low positive dc potential. This value will not fluctuate significantly when the −250-volt supply fluctuates, since this biasing arrangement provides for highly effective self-compensation. For example, an increase in the value of negative supply voltage causes an increase in the quiescent tube currents and thus an increase in the voltage drop across R10, making up for the drop in supply voltage. Therefore, a stable cathode bias is effective on both V2A and V2B.

(b) In dynamic operation, the large cathode resistor, R10, has the effect of preventing any appreciable change in the sum of the current flow through V2A and V2B. When the current of V2A decreases, due to the application of a negative signal to the grid, the potential of the cathode tends to drop. This decreases the cathode-to-grid voltage of V2B, causing an increase in the current through V2B. The sum current flowing through R10 thus remains essentially constant, since a small variation in the sum current in enough to allow the cathode potential to swing an amount sufficient for adjusting the current through V2B, as required. The cathode voltage variation of V2A and V2B allows the currents to compensate each other in the described manner: that is, the cathodes of V2A and V2B swing in phase with the grid signal applied to V2A and with an amplitude equal to half the grid signal amplitude at V2A. The 400-cps error signals on the plates of V2A and V2B are equal in amplitude and opposite in phase.

(3) *Power amplifiers V3 and V4.*

(a) The push pull 400-cps error signal outputs of V2A and V2B are coupled through capacitors C4 and C5 and parasitic suppressor resistors R12 and R15 to the grids of power amplifiers V3 and V4, respectively. The plates of V3 and V4 are coupled to output transformer T1. Resistor R14 provides the bias for class AB operation of V3 and V4. Resistors R17 and R19 are inserted in the plate circuit to suppress parasitic oscillations. The load, which is connected to the secondary of T1 (terminal 1) through connector P1 11, is the control winding of the driven motor-generator. This inductive load is resonated by capacitors C6 and C7, so that the impedance reflected into the primary of T1 is almost a pure resistance. Both V3 and V4 see half of this reflected resistance. Resistors R21

CONFIDENTIAL

and R22 function as a voltage divider to furnish degenerative feedback voltage to the bridged-T network. Resistor R18 is used to drop the supply voltage to the value required at the screen grids of V3 and V4.

(b) The plate voltage supply for V3 and V4 is the unfiltered output of a full-wave rectifier located in the +270v. −28v, and +75v or +175v power supply. This power supply is located in the director station group. The 208-volt, 400-cps, phase A and C ac input to a full-wave rectifier in the power supply is taken from the same source that provides the servo excitation voltage. The unfiltered rectifier output is a 400-cps, full wave, rectified sine wave with a peak value of approximately 420 volts and an average value of +270 volts. The rectified unfiltered voltage applied to the plates of V3 and V4 is in phase with the 400-cps error voltage applied to the control grids of V3 and V4. Because the plate voltage is unfiltered, only input signals of 400 cps and the same phase as the plate voltage can be successfully amplified. The power output is approximately 10 watts obtained from the 420-volt peak voltage at 800-cps ripple.

1. The rectified unfiltered plate voltage supply, with an average value of +270 volts, allows class AB operation of the power amplified with an efficiency greater than is ordinarily obtained using a filtered 270-volt dc plate supply for class B operation. In addition, output power is obtained with a rectified unfiltered 270-volt plate supply that would ordinarily require a filtered 420-volt plate supply. In normal class AB operation with a filtered dc plate supply (fig. 39), both V3 and V4 will conduct for more than a half-cycle of grid input voltage E_{C1} and E_{C2}. This conduction of more than a half-cycle occurs

when the output current waveform goes below the operating point toward the cutoff point. Since both V3 and V4 are conducting at this time, the two currents below the operating point are cancelled in the primary of T1. The currents that are cancelled represent wasted power that heats V3 and V4 unnecessarily.

2. In this circuit, using an unfiltered plate supply (fig. 40), the rectified unfiltered 400-cps plate voltage returns to 0 volts simultaneously for each half cycle of the 400-cps voltage waveform. The 400-cps voltage waveform appears across terminals 4 and 5 of T1 (fig. 19, TM 9-1430-257 20) when V4 is conducting and across terminals 6 and 5 of T1 when V3 is conducting so that both V3 and V4 are cut off at the same instant. The 400-cps voltage appears across terminals 1 and 3 of T1. At no time when sufficient 400-cps control signals are applied to the control grid of V3 and V4 is there wasteful cancellation of currents in T1. Thus, this circuit operates as class AB, which is equivalent to class B operation.

(c) At higher frequencies caused by spurious oscillations and by vibrations in the motor-generator shaft, the 400-cps feedback voltage and the 400-cps servo error voltage applied at P1 3 (fig. 19, TM 9-1430 257-20) cannot be maintained at 180° phase opposition; regeneration instead of degeneration results. To prevent this condition, the system is made insensitive to rapid fluctuations in speed and error by shunting the grids of V3 and V4 with series RC network C8 and R20. At 400 cps, the reactance of C8 is so large that attenuation due to this network is neglible. At frequencies above 1,000 cps caused by spurious oscillations, the reactance of the series RC network decreases.

CONFIDENTIAL

DYNAMIC CHARACTERISTIC OF V3

OPERATING POINT

CUT-OFF POINT

I_{b1}

E_{C1}

OUTPUT CURRENT WAVEFORM

O

WASTED POWER

E_{C2}

CUT-OFF POINT

OPERATING POINT

O

WASTED POWER

OUTPUT CURRENT WAVEFORM

I_{b2}

DYNAMIC CHARACTERISTIC OF V4
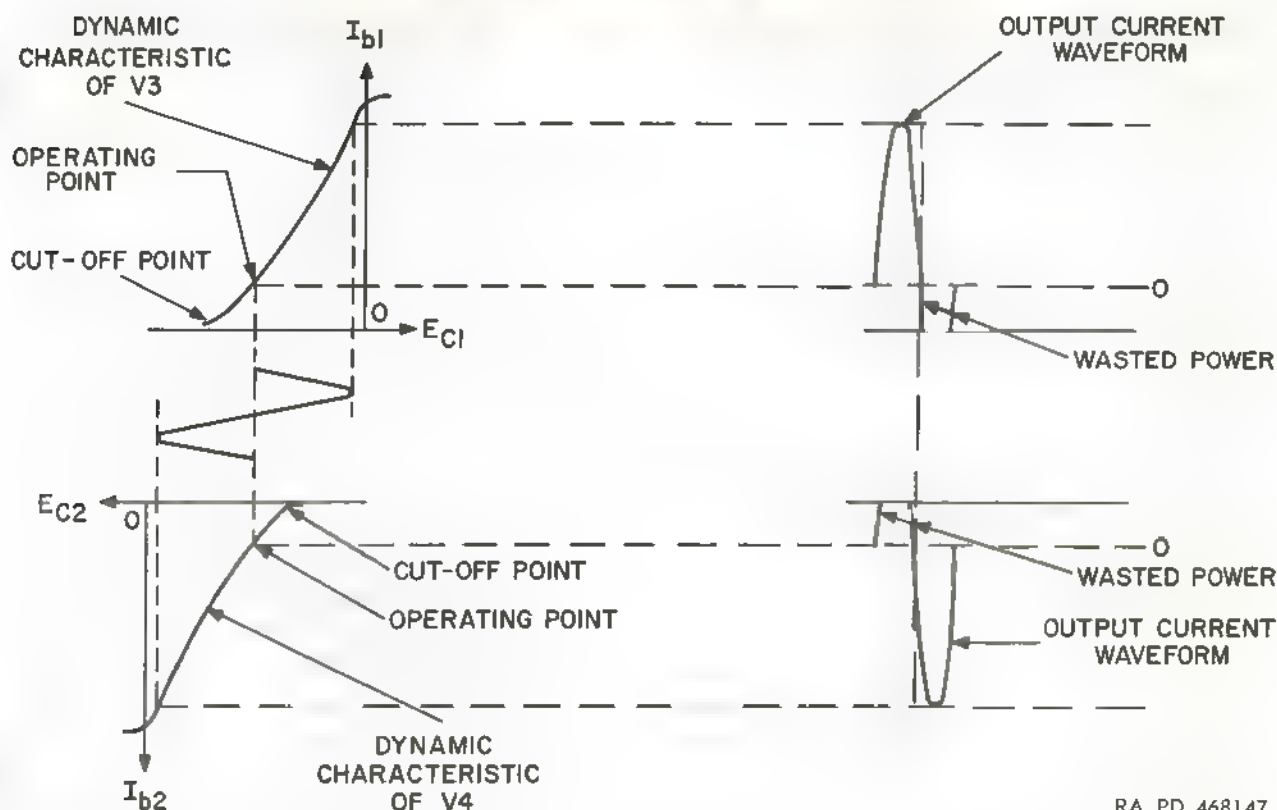
RA PD 468147

Figure 39 (U) Dynamic characteristics showing the effect of class AB push-pull amplifier operation with a filtered plate voltage supply.

The gain of the amplifier decreases sharply for signals beyond 1,000 cps caused by signal attenuation between grids. The output from the low-power servo amplifier is applied to its load through P1-11.

(4) *Bridged-T network.*

(a) The 400-cps error signal applied at P1-3 is the sum of a 400-cps servo error voltage and a 400-cps feedback voltage 180° out of phase. This voltage, applied to the grid of V1A, is not a pure sine wave since it contains third harmonic distortion. This distortion is of no use in driving the motor-generator. Moreover, it would add to the current flowing through V3 and V4 causing unnecessary heating and loading of the plates. To minimize plate dissipation, it is necessary to discriminate against

third harmonic distortion. Since LC components required to resonate at 400 cps are too bulky, it is more practical to use a selective feedback or bridged-T network to obtain the required frequency response. The bridged-T network consists of C2, C3, R6, and R7.

(b) Assuming that the frequency approaches zero in the bridged-T network, most of the feedback signal fed into the network must pass through R7 since C2 offers a large reactance to low frequencies. Assuming that the frequency approaches infinite frequency in the bridged-T network, most of the feedback signal fed into the network must pass through C2 and C3 since the reactance of C2 and C3 is much smaller than the resistance of R6 and R7. Therefore, frequencies below and above

CONFIDENTIAL
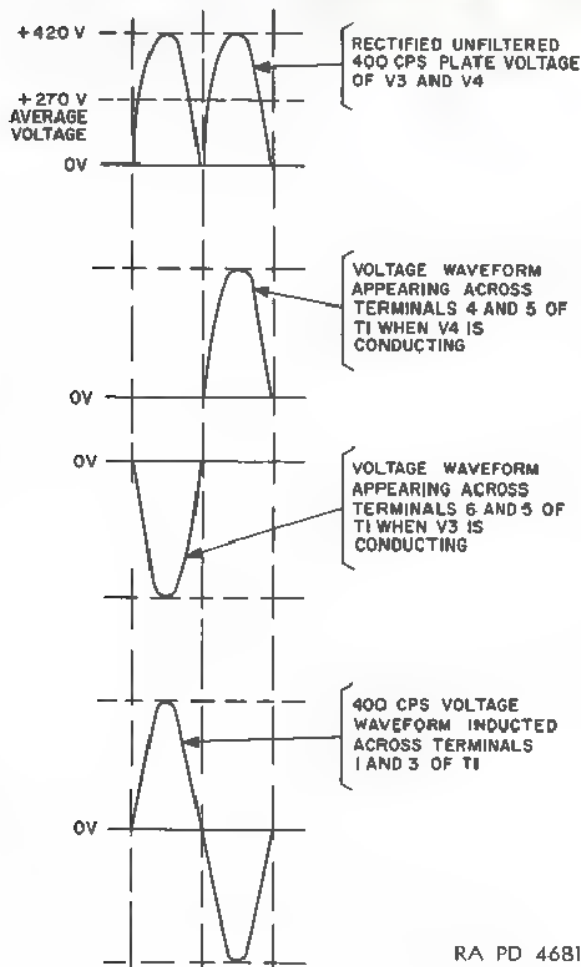
Figure 40. (U) Class AB push-pull amplifier operation with a rectified unfiltered plate voltage supply.

400 cps cancel through degeneration since the bridged-T network offers little impedance to these frequencies. Since the bridged-T network is frequency selective at 400 cps, maximum attenuation occurs at 400 cps. Therefore, all four branches are effective since the reactance of C2 and C3 are of comparable magnitude to both R6 and R7 ($X_c = R$). Since the bridged-T network offers maximum impedance to the 400-cps feedback signal, the 400-cps feedback signal cannot be developed across R6 and therefore is attenuated in the bridged-T network. The

400-cps error signal is developed across R6 and coupled through C3, resulting in maximum amplification of the 400-cps error signal.

47. Target Designate Control-Indicator 9005253, 9007683

a. General. The target designate control-indicator contains the necessary controls and indicators for moving the acquisition range circle and steerable azimuth line produced on the plan-position indicator (PPI). A RANGE dial, calibrated in thousands of yards, indicates the range established on the PPI. The target designate control-indicator provides the operator with the necessary controls to determine the position of a target in range and azimuth and to initiate the action required to transfer this information to the target tracking radar system from the acquisition radar system. The target designate control-indicator contains two subassemblies listed in (1) and (2) below.

(1) Acquisition range generator 8172913 or 9007684.

(2) Low-power servo amplifier 7614253.

> *Note.* The key letter-number combinations shown in parentheses in *b* below refer to zone locations in figure 18, TM 9–1430–257 20 unless otherwise indicated.

b. Detailed Theory.

(1) *Acquisition azimuth control resolvers.*

(*a*) *General.* Line slew resolver B1 (D7) and acquisition line resolver B2 (D8) are essentially transformers with two fixed primaries and two rotating secondaries. The stator and rotor each has two windings that are physically in quadrature.

(*b*) *Line slew resolver B1.*

1. Line slew resolver B1 is normally de-activated by deenergized line slew relay K1. The modulated 4-kc signals which produce the rotating radial sweeps on the PPI are applied at connector J3–b and f for the north-south (N–S) signal and at connector J3–e and j for the east-west (E W) signal. The N–S and E W

CONFIDENTIAL

signals are fed through contacts 6–11 and 3–10 of deenergized K1 to connector J3 D and V, respectively. Normally, K1 is deenergized and contacts 5 and 4, which connect to R1 and R4 of B1, are open. Mounted beneath the azimuth knob is a ring type azimuth switch S1 (D10) that controls K1. When S1 is depressed, −28 volts is applied through connector J3 g to steerable azimuth line relay K1 located in the PPI of the battery control console. Steerable azimuth line relay K1 energizes and applies 28 volts through connector J3–G, thereby energizing line slew relay K1. With line slew relay K1 energized, the modulated 4–kc signal which produces the PPI rotating radial sweep positioning voltage is replaced by the output from B1; the acquisition video and marks are removed from the PPI in the battery control console because of the action of energized externally-mounted steerable azimuth line relay K1.

2. A constant amplitude 4-kc reference carrier from the 4-kc oscillator is applied at connector J3–L to stator terminal S1 of B1. Stator terminals S2, S3, and S4 of B1 are returned to ground through connector J3 M. The output at rotor terminals R1–R3 of B1 is the N–S signal. The output at rotor terminals R2–R4 of B1 is the E–W signal. When K1 is energized, these outputs, the N–S and E–W signals, produce a stationary sweep on the PPI of the battery control console. This sweep is called the steerable azimuth line. This steerable azimuth line can be moved to any azimuth by rotating the azimuth knob. Releasing S1 deenergizes K1 and returns the rotating radial sweep and the acquisition video and marks to the PPI. Resolver B1 is mechanically connected to acquisition line re-

solver B2 discussed in (c) below and control transformer B3 discussed in (d) below.

(c) *Acquisition line resolver B2.* The modulated 4-kc signals are applied across J3–b and f for the N S signal and across J3 e and j for the E–W signals and are fed to stators S1 S3 and S2–S4, respectively, of acquisition line resolver B2. Rotor terminals of R1–R3 of B2, for the N–S output signal, are connected to connector J3–P and Z. Rotor terminals of R2–R4, for the E–W output signal, are connected to connector J3–Q and a. The modulated N–S and E–W 4-kc signals, which are sinusoidally modulated at a frequency dependent upon the frequency of the acquisition antenna rotation, are modified by the azimuth position of B2. The modified modulated 4-kc signals are used in the precision indicator of the battery control console for generating azimuth sweeps and for unblanking the cathode-ray tube screen. The modified modulated 4-kc signals are also used in the precision indicator of the battery control console for generating an acquisition azimuth mark which appears on the PPI as a flashing azimuth line. This line appears as the rotating radial sweep rotates past the designated azimuth. By rotating the azimuth knob, the flashing azimuth line can be made to appear at any azimuth position on the PPI.

(d) *Control transformer B3.* The rotor of control transformer B3 is mechanically connected to the rotors of B1, B2, and the azimuth knob. Rotor terminals R1 and R2 of B3 are connected to connector J4–L and K. The stator terminals S1, S2, and S3 of B3 are connected to connector J4–J, H, and C Any rotation of the azimuth knob will cause a voltage to be induced in the rotor of B3. The voltage induced in the rotor of B3 is the error voltage between

azimuth control transmitter B1, located in the target track antenna receiver-transmitter group, and B3. The error voltage is used as a slewing voltage for slewing the target track antenna when ACQUIRE switch S5, located in the target track control drawer of the target radar control console, is closed. Upon application of the error voltage, the target track antenna slews to a position in azimuth corresponding to the azimuth designated by the azimuth position of B3.

(2) *Range MAN-AID switch S6 and range SLEW switch S5.*

(a) There are three methods of controlling the range servo system; manual, aid, and slew. With MAN-AID switch S6 (B7) in MAN position, clutch coil L1 is energized, disengaging range handwheel generator B5 from the brush arm of aid variable resistor R3 (B8) because of the mechanical action of the clutch. The brush arm of R3 is returned to the electrical center of R3 since the brush arm is spring-loaded. As B5 is rotated by hand, the generator rotor is turned and a 400-cps error voltage is developed. The amplitude of this 400-cps error voltage varies directly with the speed of rotation of B5. The phase relationship between the 400-cps error voltage and the 400-cps excitation voltage applied through connectors J4-B and A changes 180° as the direction of rotation of B5 is changed. The amplitude determines the speed of acquisition range mark movement while the direction determines the phase. The 400-cps error voltage, developed across resistor R15, is coupled to connector J1-3 and to the low power servo amplifier through either R6, R7, or R8, depending on the operating condition of 15 rpm and 10-rpm relays K2 and K3, respectively.

(b) When S6 is placed in the AID position, L1 is deenergized. This releases

the spring loaded clutch allowing the friction plates to engage B5 mechanically to the brush arm of R3. A 400-cps excitation voltage from transformer T1 is applied across parallel connected BAL. 1, BAL. 2, and aid variable resistors R20, R14, and R3, respectively. To prevent range motor generator B4 from creeping when there is no 400-cps error voltage being applied to the low power servo amplifier, balance switch S7 is closed and R20 is adjusted for zero creep of B4. Switch S7 is opened after the adjustment of R20 is completed. By balancing R14 and the centering lever on R3, no 400-cps error voltage can be developed, thereby preventing B4 from creeping when B5 is stationary. Essentially, R3 and R14 form a bridge circuit. The brush arm of R14 determines the ground reference point, since it is connected through R12 and R13 to ground. By adjusting R14, the voltages that cause creeping are canceled by applying an amplitude balance voltage to B4 that is equal to the algebraic sum of all the voltages that cause creep but is opposite in phase. Since the brush arm of R3 is at ground potential when it is centered, any rotation of B5 displaces the brush arm of R3 and a 400-cps error voltage is developed. The amplitude of this 400-cps error voltage is determined by the amount by which the brush arm of R3 has been displaced from electrical center. The phase relationship between this 40-cps error voltage and the 400-cps excitation voltage is that of being in phase or being 180° out of phase, depending on the direction in which the brush arm of R3 is displaced from electrical center. The 400-cps error voltage that is developed between the brush arm of R3 and ground is coupled through resistor R5 and J1-3 to the low-power servo amplifier.

(c) When range SLEW switch S5 (B8) is held closed, the full 400-cps error voltage across R3 is developed across R17 and coupled through resistor R9 and J1-3 to the low-power servo amplifier. The phase of this 400-cps error voltage, with reference to 400-cps servo excitation is either zero or 180°, depending upon whether S5 is closed in the IN or OUT position.

(d) The low-power servo amplifier receives the 400-cps error voltage whether the MAN, AID, or SLEW method of positioning is used. If the MAN position is being used, the gain of the amplifier varies inversely with the rotational speed of the antenna. This causes the acquisition range mark, presented on the indicators, to move a greater amount at a given speed of RANGE handwheel rotation when operating the antenna at a low speed. This is considered necessary since the target moves a greater distance between echoes when the antenna is rotating slowly. The gain of the low-power servo amplifier is changed by changing the input impedance through the operation of 15-rpm and 10-rpm relays K2 (B10) and K3, respectively. At acquisition antenna rotation of 15 revolutions per minute (rpm), K2 operates when a ground is supplied to connector J4-g from ANTENNA-AZIMUTH RPM switch S7 located on the acquisition control-indicator. With K2 energized, the 400-cps error voltage from B5 is coupled to the low-power servo amplifier through R6 and J1-3. As ground is removed from J4-g and applied to connector J-4c; K2 deenergizes and K3 energizes. With K3 energized, and with the acquisition antenna rotation of 10 rpm, the 400-cps error voltage from B5 is coupled to the low-power servo amplifier through R7 and J1-3. At acquisition antenna rotation of 5 rpm,

both K2 and K3 are deenergized and the 400-cps error voltage from B5 is coupled to the low-power servo amplifier through R8 and J1-3. The low-power servo amplifier consists of a push-pull power amplifier that receives the 400-cps servo error voltage through voltage amplifiers which produce a suitable phase inversion. The 400-cps servo error voltage, from the output of the low-power servo amplifier, is fed to motor stator winding 1 2 of B4.

(e) If only the acquisition radar system is operative, the 400-cps excitation voltages are applied to B4 (A6) from the acquisition power control panel. As the target track radar power is turned on, track generator excitation relay K4 (B11) is operated to change the source of the 400-cps excitation voltage from the acquisition power control panel to the target track control power supply. This insures that the aid voltage supplied to the target track radar during the acquire process is of the correct phase relationship with the 400-cps excitation voltage used to position the rate variable resistor in the target track radar.

(f) With 400-cps excitation voltage applied to B4, the 400-cps servo error voltage output of the low-power servo amplifier causes the rotor of B4 to rotate. The speed of rotation is determined by the amplitude of the 400-cps servo error voltage.

(g) As B4 turns, the brush arm of range variable resistor R1 (B3), mechanically connected to B4, is positioned. A 400-cps voltage is developed across generator winding 7-8. A portion of this voltage is returned through resistor R10 (C4) to the input of the low-power servo amplifier where it mixes as a degenerative 400-cps servo feedback voltage with the 400-cps error voltage from B5 to produce the 400-cps servo error voltage. This prevents overshooting or mechanical oscilla-

tions of the range servo system. As B4 rotates, the brush arm of R1 is placed at a new position. This changes the dc input range control voltage to the phantastron within the acquisition range generator, as discussed in paragraph 45. An aid voltage comparable to the rate of range change is available across R11. This voltage is supplied to the target track radar to assist in acquiring the designated target.

(h) Normally closed cam-operated limit switches S2 (A6) and S3 prevent B4 from driving R1 against its mechanical stops when the gear train reaches either end limit. When either S2 or S3 opens, the motor excitation voltage is dropped across R16, causing B4 to become inoperative until B4 reverses its direction of rotation.

(3) *DESIGNATE-ABANDON switch S4.* DESIGNATE-ABANDON switch S4 (A3) is a toggle switch that is spring-loaded to center position. Its direction of operation from the center position determines whether a new target is designated or a target being tracked is abandoned. Switch S4 controls an external light and buzzer that indicate a target is designated.

c. Target Designate Control-Indicator 9007683. Target designate control-indicator 9007683 is similar to target designate control-indicator 9005253. Target designate control-indicator 9007683 (fig. 18, TM 9-1430-257-20) differs in that it has a new range dial indicating a maximum range of 250,000 yards and a new subassembly, acquisition range generator 9007684, extending the range on the PPI. The indicators are not interchangeable.

47.1 (U). Target Designate Control-Indicator 9143718

a. General. The target designate control-indicator contains the necessary controls and indicators for moving the acquisition range circle and steerable azimuth line produced on the plan-position indicator (PPI). A RANGE dial, calibrated in thousands of yards, indicates the range established on the PPI. The target

designate control-indicator provides the operator with the necessary controls to determine the position of a target in range and azimuth and to initiate the action required to transfer this information to the target tracking radar system from the acquisition radar system. The target designate control-indicator contains two subassemblies listed in (1) and (2) below.

(1) Acquisition range generator 9143997.
(2) Low-power servo amplifier 7614253.

b. Detailed Theory. The detailed theory of target designate control-indicator 9143718 (fig. 79, TM 9-1430-257-20/1) is the same as that given in paragraph 47 except for TRACK CROSS switch S8. This switch controls presentation of the track electronic cross on the indicators. In the OFF position, S8 provides a ground for the target ranging radar cross-off relay in the video and mark mixer. The relay removes the track range mark and track range gate from the presentation system.

47.2 (U). Target Designate Control-Indicator 9986487

Target designate control-indicator 9986487 is similar to target designate control-indicator 9007683. Target designate control-indicator 9986487 (fig. 18, TM 9-1430-257-20) differs in that it has RANGE RATE variable resistor R21 added and resistor R10 changed to permit adjustment of the feedback voltage to the low-power servo amplifier.

47.3 (U). Target Designate Control-Indicator 9988785

Target designate control-indicator 9988785 similar to target designate control-indicator 9143718. Target designate control-indicator 9988785 (fig. 79, TM 9-1430-257-20) differs in that it has RANGE RATE variable resistor R21 added and resistor R10 changed to permit adjustment of the feedback voltage to the low-power servo amplifier.

48 (U). Acquisition Control-Indicator 9137929

a. General. The acquisition control-indicator contains various controls, switches, lamps, and meters for monitoring and adjusting the circuits of the acquisition radar system. The meters indicate the acquisition antenna elevation, the currents and voltages of the mag-

netron, its associated high-voltage power supply, and the acquisition magnetron frequency. The acquisition control-indicator contains one subassembly, which is STC 8512082.

b. Detailed Theory.

Note. The key letter-number combinations shown in parentheses in (1) through (21) below refer to zone locations in figure 21, TM 9-1430-257-20 unless otherwise indicated.

(1) *MAGNETRON switch S1 and MAG- NETRON meter M1.* MAGNETRON switch S1 (A2) is a 3-position toggle switch spring-loaded to center position. Switch S1 provides a means for monitoring the voltage and current output of the acquisition HV power supply and the current output of the magnetron. MAGNETRON meter M1 indicates the amplitude of either the acquisition magnetron current, acquisition HV power supply current, or acquisition HV power supply voltage, depending on the position of S1. Both S1 and M1 comprise the monitoring circuit. With S1 in the FS—

50 MA position, a portion of the magnetron current is applied to M1 through connector J3-D and U. With S1 in the MA FS—1000 position, a portion of the high-voltage power supply output current is applied to M1 through connector J3-T and frame ground. With S1 in the KV FS=10 position, a voltage proportional to the high-voltage power supply output voltage is applied to M1 through J3-V and frame ground.

(2) *MAGNETRON-ON switch S2, MAG- NETRON-OFF switch S4, and MAG- NETRON-HV variable transformer T1.* MAGNETRON-HV supply variable transformer T1 is used to vary the dc output of the acquisition HV power supply. When MAGNETRON- READY indicator light I2, connected across connector J3-d and k, is illuminated, it indicates that the acquisition HV power supply is ready to be energized. Turning MAGNETRON- HV supply knob T1 (fig. 41) counterclockwise closes START

switch S3, since T1 and S3 are mechanically coupled. When MAGNETRON-ON switch S2 is closed, the acquisition HV power supply is energized. This action operates high voltage on relays K3 and K4 located in the acquisition power control panel, whose contacts bypass S2 and S3. MAGNETRON-ON indicator light I1, connected in parallel with T1, is illuminated to indicate that the acquisition HV power supply has been energized. When S2 is released, the ac-

quisition HV power supply remains energized. When T1 is rotated clockwise, S3 opens. The acquisition HV power supply continues to be energized until MAGNETRON-OFF switch S4 is depressed, which deenergizes the circuit.

(3) *IND HV switch S5.* IND HV switch S5 (B2), a 2-position toggle switch, applies 120-volt, 400-cps, phase B ac voltage to the PPI HV power supply through connector J3-c, contacts 1 and 2 of S5, and connector J3-R. This occurs when

RA PD 468149

Figure 41. (U) *Magnetron high-voltage circuit—partial schematic diagram.*

542106 O - 60 - 9

CONFIDENTIAL

S5 is closed, also causing IND HV-ON indicator light I3 to illuminate. The +1,550 volts from the PPI HV power supply, which is applied to the PPI, is interlocked through contacts 4 and 5 of S5.

(4) *MAG FREQ & REC NOISE switch S9.* MAG FREQ & REC NOISE switch S9 (C9), a 3-position toggle switch spring-loaded to center position, is connected to magnetron tuning drive motor B2 in the acquisition receiver-transmitter. By closing S9 in either the DECREASE FREQ or INCREASE FREQ position, S9 reverses the direction of rotation of B2 by reversing the phase of the alternating current applied to B2. A 120-volt, 400-cps, phase C ac voltage is applied to S9 and is used to change the acquisition magnetron frequency remotely.

(5) *AFC switch S11 and AFC-RELEASE switch S10.* AFC switch S11 (C4), a 2-position toggle switch, and AFC-RELEASE switch S10 (C5), a pushbutton type switch, are associated with the acquisition AFC. An AFC-HUNT indicator light I4 is provided to indicate that the AFC is in the hunt condition. When the magnetron is energized and S11 is in the ON position, the acquisition AFC is energized and will begin hunting, causing I4 to illuminate. This hunting condition will continue until the acquisition local oscillator is tuned to the correct frequency. In actual operation the acquisition AFC hunts for the proper acquisition local oscillator frequency. When this frequency is reached, the acquisition local oscillator is said to be locked on and I4 is extinguished. However, the acquisition AFC might attempt to lock the acquisition local oscillator on an incorrect frequency. In this event, I4 will not be extinguished but will flash rapidly at an intermittent rate. When this occurs, S10 can be depressed to cause the acquisition AFC to resume searching the frequency band. Indicator light I4 will again be illuminated and will remain so until the acquisition AFC has found and locked the acquisition local oscillator on the proper frequency. Although I4 should extinguish when the acquisition AFC is locked on the proper frequency, I4 may flash slowly at an intermittent rate.

(6) *ANTENNA-ELEVATION scan switch S6.* ANTENNA-ELEVATION scan switch S6 (C2) is a 3-position toggle switch which is spring-loaded to center position from the UP position only. Switch S6 permits adjustment of the acquisition antenna radar beam elevation. When S6 is placed in either the UP or DOWN/SCAN position, a ground is provided to operate the relays in the acquisition antenna, which are necessary to control the acquisition antenna elevation. When S6 is in the UP position, the acquisition antenna reflector increases in elevation until it reaches its upper limit. It remains in this position until S6 is operated downward. When S6 is placed in the DOWN/SCAN position, the acquisition antenna reflector automatically scans up and down in elevation.

(7) *ANTENNA-ELEVATION synchro torque receiver and indicator B1.* ANTENNA-ELEVATION synchro torque receiver B1 (D3) receives the elevation data, for positioning purposes, from antenna synchro torque transmitter B1 in the acquisition antenna. Receiver B1 is mechanically coupled to the ANTENNA-ELEVATION indicator. The ANTENNA-ELEVATION indicator indicates the degree of tilt (in mils) of the acquisition antenna RF beam. This synchro transmitter-receiver system uses 120-volt, 400-cps, phase C power for synchro excitation.

(8) *ANTENNA-AZIMUTH RPM switch S7.* ANTENNA-AZIMUTH RPM switch S7 (C2) is a 4-position rotary switch. Its position determines the speed of rotation of the acquisition antenna. The acquisition antenna can be

128

CONFIDENTIAL

made to rotate at 5, 10, or 15 rpm by providing a ground on the proper contacts of switch S7A to operate the necessary relays in the acquisition antenna pedestal. In the OFF position, switch S7A applies a blanking voltage by grounding the intensity dc voltage of the PPI in the target radar control console. In the OFF position, switch S7B completes a blanking circuit (par. 38*b* (1)(*e*)) of the PPI in the battery control console. These blanking voltages blank the sweeps when the acquisition antenna is not rotating. In the 5-, 10-, or 15-rpm position, S7B makes the connection to the +250 volts to the resolver amplifier in the acquisition antenna pedestal

(9) *RECEIVER-STC variable resistor R1, RECEIVER-GAIN variable resistor R3, and transformer T2.* RECEIVER-STC variable resistor R1 (B5) is provided to give the operator control of the amplitude of the STC pulse. RECEIVER-GAIN variable resistor R3 is provided to adjust the acquisition IF preamplifier gain. Transformer T2 provides filament voltage to the various stages in the STC.

(10) *NOISE GEN switch S19 and MAG FREQ & REC NOISE meter M2.* NOISE GEN switch S19 is a 3-position rotary switch. When S19 is in the OFF position (fig. 42), a voltage tapped from frequency measure variable resistor R1 in the magnetron tuning drive of the acquisition receiver-transmitter is applied across MAG FREQ & REC NOISE meter M2. Since M2 is not calibrated in frequency but in volts, when the acquisition magnetron frequency increases, the voltage reading on M2 increases. This arrangement indicates the approximate acquisition magnetron frequency within the 3,100 to 3,500-megacycle range. When S19 is in the ADJ position (fig. 43), high voltage on relay K1, located in the acquisition RF power supply control, is energized. With K1 energized, the high voltage induced into the secondary of transformer T3, located in the acquisition receiver transmitter, ionizes argon gas tube V7, located in the noise generator, which generates the noise signal. This noise signal is fed back to M2, at which time M2 is calibrated to the specified meter deflection. When S19 is in the MEAS position, K1 is deenergized and the meter deflection should indicate normal receiver noise. The ADJ and MEAS positions of S19 are used to determine the receiver performance ratio. When S19 is in the ADJ position, NOISE GEN-ON indicator light I7 is illuminated to indicate that 120 volts, 400 cps is being applied to T3.

(11) *VID ALARM THRESHOLD variable resistor R5 and switch S8.* VID ALARM THRESHOLD variable resistor R5 (C8) and switch S8 are mechanically coupled. When R5 is rotated from the OFF position, S8 closes providing a ground for video alarm relay K1 located in the alarm control, thereby applying filament power to the various stages. When a target is present, the alarm control is used to alert the battery control console operator by an audible tone. As R5 is rotated, the voltage level at which the noise and video signals operate will be varied. For additional information, refer to paragraph 20*b*(16).

(12) *MTI—MODE switch S18 and MTI—SECTOR ANGLE resolver B2.* MTI—MODE switch S18 (C8) is a 3-position rotary switch. When in the OFF position, S18 removes the MTI presentation from the PPI. The 360° position of S18 provides an MTI presentation over the entire 360° of the PPI. The SECTOR position of S18 provides an MTI presentation for any sector of the PPI, as determined by the setting of MTI—SECTOR ANGLE resolver B2 (D8). The manual setting of the rotor of B2 transmits information to the MTI circuits and controls the sector over which the MTI is present. To further understand the

CONFIDENTIAL

Figure 42 (U) Noise gen switch S19—off position—simplified schematic diagram

purpose of S18 and B2, refer to paragraph 17.

(13) *IFF-GAIN variable resistor R10.* IFF-GAIN variable resistor R10 (A10) adjusts the gain of the IFF control group. The adjustment of R10 varies the brightness of the reply signals and sharpens the reply image on the PPI.

(14) *IFF-CHOP switch S12.* IFF-CHOP switch S12 (A10) is a 2-position toggle switch. When S12 is placed in the ON position, a chopping circuit in the IFF coder control unit is activated; this periodically interrupts the train of the transmitted pulses. This action will interrupt the reply signals from the target in a like manner, with the result that the IFF reply on the PPI will appear as a clearly defined series of dashes forming an arc. When S12 is placed in the OFF position, the IFF reply will have the same brightness, focus, and relative position but will appear as a solid arc.

(15) *IFF-CHALLENGE switch S13.* IFF-CHALLENGE switch S13 (B10) is a pushbutton type switch. The operator may interrogate or challenge targets by depressing S13. When a target is being challenged, IFF-CHALLENGE indicator light I5 should become illuminated. When I5 is illuminated, it indicates that an interrogation pulse of sufficient strength to be received by an aircraft transponder is being transmitted. If I5 does not become illuminated when S13 is depressed, it is an indication that the IFF transmitter is not transmitting a pulse of sufficient amplitude to be received by an airborne transponder.

(16) *IFF-ON indicator light I6.* IFF-ON indicator light I6 is illuminated to indicate that power is being applied to the

130

CONFIDENTIAL

Figure 43 (U). NOISE GEN switch S19 – ADJ position – simplified schematic diagram.

IFF units and that all switches in the IFF units are set for remote operation from the acquisition control-indicator. Should I6 be extinguished, it is an indication that one of the switches in the IFF units is not in its proper position.

(17) *IFF-GTC switch S14.* IFF-GTC switch S14 (C9) is a 2-position toggle switch. To conform with the operating range of the acquisition radar system, S14 is placed in either the LONG or SHORT position. This permits the IFF receiver system to obtain a high gain for reply signals from distant targets without overloading the PPI with strong signals from targets in close range. When S14 is placed in the SHORT position, the acquisition IFF receiver is set for short range operation. When S14 is placed in the LONG position, the acquisition IFF receiver is set for long range operation.

(18) *IFF-MODE switch S15.* IFF-MODE switch S15 (C10) is a 3-position toggle switch. Its function is to provide the operator with a means of selective identification.

(19) *IFF-FOE switch S16.* IFF-FOE switch S16 (C10) is of the pushbutton type. When depressed, S16 completes the energizing path for foe relay K1 on the battery signal panel-indicator. Contacts 4-10 of K1 close, completing the energizing path for ready to fire relay K8 on the battery signal panel-indicator.

(20) *IFF-FRIEND switch S17.* IFF-FRIEND switch S17 (C10) is a 2-position toggle switch spring-loaded to down position. With S17 in the FRIEND position, contacts 2-3 open, interrupting the lock-up circuit of foe relay K1 on the battery signal panel-

indicator when K1 is energized. Contacts 5-6 of S16 open, interrupting the energizing path for burst relay K1 in the combining amplifier of the missile radar control console.

(21) *INT SPR-OFF switch S20.* INT SPR-OFF switch S20 (A7) is a 2-position toggle switch. When S20 is in the INT SPR position, interference suppressor relay K1 in the trigger pulse amplifier is energized, switching IS and MTI-IS video into the presentation system.

48.1 (U). Acquisition Control-Indicator 9990574

Acquisition control-indicator 9990574 (fig. 81, TM 9-1430 257-20) consists of HIPAR control-indicator 9990575 (par. 48.2), LOPAR control-indicator 9156372 (par. 48.3), IFF control-indicator 9156348 (par. 48.4), alarm control 9156414 (par. 48.5), and STC 8512082 (par. 49). These subassemblies contain various controls, switches, lamps, and meters for monitoring and adjusting the LOPAR and HIPAR. The acquisition control-indicator also contains radar select relay K1 and auxiliary acquisition radar squelch relay K2 which are used in the HIPAR and LOPAR select circuits.

48.1.1 (U). Acquisition Control-Indicator 9985604

Acquisition control-indicator 9985604 (fig. 21.1, TM 9-1430-257 20) is the same as acquisition control-indicator 9137929 discussed in paragraph 48 except as follows: The video alarm circuit, consisting of switch S8, resistors R6 and R7, and variable resistor R5, is removed. Ground connection for IFF GAIN variable resistor R10 is changed and provision is made for remote control of receiver gain through connectors J5-V and J5-T.

48.1.2 (U). Acquisition Control-Indicator 9985650

a. General. Acquisition control-indicator 9137929 or 9985604 is modified by DA MWO 9-1400-268-50 to add the antijam display capability. The added components are discussed in *b* below. Refer to paragraph 48 for theory of unchanged components.

b. Detailed Theory.

(1) *Acquisition control-indicator modifications.* If acquisition control-indicator 9137929 is modified, the circuits and components discussed in paragraph 48.1.1 must be applied. If acquisition control-indicator 9985604 is modified, these circuits and components are already applied.

(2) *RECEIVER-GAIN variable resistor R3 and switch S22.* RECEIVER-GAIN variable resistor R3 (fig. 21.2, TM 9-1430-257-20) varies the gain of the acquisition IF preamplifier. When R3 is turned fully clockwise, S22 closes and provides ground through external circuitry to the AGC relay K2, which energizes and provides ground to relay K2 in the fast AGC amplifier 9990768.

(3) *IS/PROC switch S21.* When IS PROC switch S21 is set to the IS ON position, IS ON relay K1 in the acquisition interference suppressor is energized. When S21 is set to the PROC ON position, MTI MODE relay K1 and, external PROC ON relay K1 in the delay line driver and PROC ON relay K2 in the acquisition interference suppressor are energized. When MTI MODE relay energizes, MTI ground is applied through connector J5-C to the MTI gate in the electronic gate and disables the MTI channel.

(4) *AJD switch S20.* When AJD switch S20 is set to the ON position, K1 energizes and disables the MTI channel. AJD ON relay K1 in the target data processing unit, AJD ON relay K1 in the electronic gate, and AJD ON relay K1 and AGC ON relay K2 in the fast AGC amplifier are also energized when S20 is set to ON.

(5) *JS ONLY switch S11.* When JS ONLY switch S11 is operated, the same action occurs as does when S20 is set to ON except that MTI MODE relay is not energized and JS ONLY relay K2 in the electronic gate is energized.

(6) *NOISE GEN switch S19.* NOISE GEN switch S19 is a 5-position rotary switch. When S19 is in the OFF position, a voltage is tapped from the frequency measure variable resistor R1 in the magnetron tuning drive and applied across MAG FREQ & REC NOISE meter M2. M2 is voltage calibrated, with the voltage indication being proportional to the acquisition magnetron frequency. This arrangement indicates the approximate magnetron frequency within its limits from 3,100 to 3,500 megacycles. When S19 is in the MAIN ADJ position, the noise generator in the main receiver channel is enabled and M2 indicates the noise reference level. When S19 is in the MAIN MEAS position, the noise test circuit is enabled and M2 provides an indication that is used in conjunction with the noise reference level for calculating the noise of the main receiver channel. When S19 is in the AUX ADJ position, the noise generator in the auxiliary receiver channel is enabled and M2 indicates the noise reference level. When S19 is in the AUX MEAS position, the noise test circuit is enabled and M2 pro-

vides an indication that is used in conjunction with the noise reference level for calculating the noise of the auxiliary receiver channel.

48.2 (CMHA). HIPAR Control-Indicator 9990575

a. *General.* The HIPAR control-indicator contains various controls, switches, and lamps

for monitoring and adjusting the circuits of the HIPAR system.

b. *Detailed Theory.*

(1) *HIPAR SELECTED indicator light DS1.* When HIPAR SELECTED indicator light DS1 (fig. 82, TM 9–1430 –257–20) is illuminated, it indicates that RADAR SELECT switch S7 is in the HIPAR position.

(2) *HIPAR POWER indicator light DS2.* HIPAR POWER indicator light DS2 is illuminated by the alarm control when HIPAR transmitter power is sufficient to provide normal operation.

(3) *DISPLAY switch S1.* DISPLAY switch S1 is a 3-position rotary switch spring-loaded to the center position. When momentarily held to STROBE ONLY, ECM repeaters are identified in azimuth. When set to NORMAL, the HIPAR receiver is set for normal operation. When momentarily set to STAGGER OFF, ECM repeaters are identified in range.

(4) *RECEIVER switch S2.* RECEIVER switch S2 is a 2-position toggle switch. When S2 is set to NORMAL, CLUTTER GATE switch S3 and DISPLAY switch S1 are enabled. EMERGENCY GAIN variable resistor R1 is disabled. When S2 is set to EMERGENCY, R1 is enabled, allowing receiver gain to be manually controlled.

(5) *CLUTTER GATE switch S3.* CLUTTER GATE switch S3 is a 3-position rotary switch. When S3 is set to ALL RANGE, noncoherent MTI operation is obtained over the entire PPI range. When S3 is set to NORMAL, noncoherent MTI video is present beyond the range gate only. When S3 is set to OFF, noncoherent video is completely eliminated.

(6) *Resistor R2.* Resistor R2 is a current-limiting resistor for indicator light DS1.

48.3 (CMHA). LOPAR Control-Indicator 9156372

a. *General.* The LOPAR control-indicator contains switches, lamps, controls, a meter, and a dial indicator. The combined front panel controls adjust and monitor the performance of the LOPAR antenna, radar magnetron frequency, radar receiver, MTI presentation, and the selection and status of LOPAR energizing power.

b. *Detailed Theory.*

Note. Continuous reference is made to figure 83, TM 9–1430–257–20 unless otherwise indicated.

(1) *ANT RPM switch S3.* ANT RPM switch S3 is a 4-position rotary switch which determines the speed of rotation of the LOPAR antenna. When set to OFF, the LOPAR antenna remains stationary. When set to 5, 10, or 15, the LOPAR antenna rotates at 5, 10, or 15 rpm, respectively.

(2) *ANT ELEV indicator B1.* ANT ELEV indicator B1 is mechanically coupled to a dial indicator on the front panel. It indicates LOPAR beam angle. The indicator dial is graduated from 0 to 400 mils in increments of 50 mils.

(3) *Frequency switch S1.* Frequency switch S1 decreases LOPAR transmitter frequency to a minimum of 3100 megacycles when operated to the DECR position. When operated to the INCR position, it increases the frequency of the LOPAR transmitter to a maximum of 3500 megacycles.

(4) *UP-DOWN/SCAN switch S4.* UP-DOWN/SCAN switch S4 controls the beam deflection angle of the LOPAR antenna. When operated and held in the UP position, the elevation of the LOPAR transmitted beam increases to a maximum of 400 mils. When set to

132.1

the DOWN/SCAN position, the elevation of the LOPAR transmitted beam is decreased to a minimum of 0 mils. If allowed to remain in the DOWN/SCAN position, the LOPAR transmitted beam automatically scans between 0 mils and the upper limit of the prevailing scan condition. When released from the UP position, the elevation of the LOPAR beam remains at the elevation angle indicated on the ANT ELEV indicator discussed in (2) above.

(5) *INTFER SUPPR switch S5.* When INTFER SUPPR switch S5 is set to ON, it reduces noise and clutter on the PPI.

(6) *AFC RELEASE switch S2.* AFC RELEASE switch S2 provides AFC control on LOPAR only. When S2 is held depressed for 5 seconds and then released, it allows the LOPAR automatic frequency control (AFC) to begin the search cycle for the correct intermediate frequency (IF) as indicated on AFC HUNT indicator light DS3 discussed in (13) below.

(7) *MTI switch S6.* When MTI switch S6 is set to 360°, it causes fixed echoes to be blanked out over the present MTI range when either the LOPAR or HIPAR is in use. When the LOPAR is in use, and switch S6 is placed in the SECTOR position, the moving target indicator (MTI) acts only upon that portion of the PPI selected by the MTI SECTOR ANGLE knob on the LOPAR auxiliary control-indicator. When the HIPAR is in use, and switch S6 is placed in the 360° position, there is a 360° MTI presentation regardless of the setting of the MTI sector angle knob.

(8) *REC GAIN variable resistor R1.* REC GAIN variable resistor R1 controls the signal gain of the video display on the PPI and the precision indicator on the battery control console.

(9) *MAG FREQ meter M1.* MAG FREQ meter M1 indicates the relative LOPAR transmitter frequency. The scale of M1 is graduated from 0 to 100 in increments of 5.

(10) *STC variable resistor R2.* STC variable resistor R2 controls the negative step of the STC output pulse. When R2 is turned to the ccw position, R2 disables STC circuits in both the LOPAR and HIPAR receivers. When rotated cw, R2 varies the range (0 to 20,000 ±5000 yards) of the LOPAR STC which minimizes ground clutter and blooming, and enables the HIPAR STC, but has no effect on STC range.

(11) *LOPAR SELECTED indicator light DS1.* LOPAR SELECTED indicator light DS1 illuminates when the RADAR SELECT switch on the IFF control-indicator panel is set to LOPAR.

(12) *LOPAR POWER indicator light DS2.* LOPAR power indicator light DS2 illuminates when energizing power is applied to the LOPAR circuits.

(13) *AFC HUNT indicator light DS3.* When AFC HUNT indicator light DS3 glows steadily, the LOPAR AFC circuit is searching for the correct intermediate frequency. When DS3 is flickering or extinguished and a strong video appears on the PPI, the LOPAR AFC circuit is locked on the correct intermediate frequency. When DS3 is extinguished and no video appears on the PPI, the LOPAR AFC is locked on the incorrect intermediate frequency.

(14) *Indicator light DS4.* Indicator light DS4 provides illumination for the ANT ELEV indicator discussed in (2) above.

48.4 (U). IFF Control-Indicator 9156348

a. General. The IFF control-indicator contains the controls for the IFF equipment plus certain tactical controls for the radar.

b. Detailed Theory.

(1) *IFF ON indicator light DS1.* IFF ON indicator light DS1 (fig. 84, TM 9-1430-257-20/1) is illuminated to indicate that power is being applied to the IFF units and that all switches in the IFF units are set for remote operation from the IFF control-indicator. Should DS1 be extinguished, it is an indication that one of the switches in the IFF units is not in its proper position.

(2) *CHALLENGE switch S1.* CHALLENGE switch S1 is a pushbutton type switch. The operator may interrogate or challenge targets by depressing S1. When a target is being challenged, CHALLENGE ON indicator light DS2 should become illuminated. When DS2 is illuminated, it indicates that an interrogation pulse of sufficient strength to be received by an aircraft transponder is being transmitted. If DS2 does not become illuminated when S1 is depressed, it is an indication that the IFF transmitter is not transmitting a pulse of sufficient amplitude to be received by an airborne transponder.

(3) *CHOP switch S4.* CHOP switch S4 is a 2-position toggle switch. When S4 is placed in the ON position, a chopping circuit in the IFF coder control unit is activated; this periodically interrupts the train of the transmitted pulses. This action will interrupt the reply signals from the target in a like manner, with the result that the IFF reply on the PPI will appear as a clearly defined series of dashes forming an arc. When S4 is placed in the down position, the IFF reply will have the same brightness, focus, and relative position, but will appear as a solid arc.

(4) *GTC switch S6.* GTC switch S6 is a 2-position toggle switch. To conform with the operating range of the LOPAR, S6 is placed in either the LONG or SHORT position This will permit the IFF receiver system to obtain a high gain for reply signals from distant targets without overloading the PPI with strong signals from targets in close range. When S6 is placed in the SHORT position, the acquisition IFF receiver is set for short range operation. When S6 is placed in the LONG position, the acquisition IFF receiver is set for long range operation.

(5) *MODE switch S5.* MODE switch S5 is a 3-position toggle switch. Its function is to provide the operator with a means of selective identification.

(6) *FOE switch S3.* FOE switch S3 is of the pushbutton type. When depressed, S3 completes the energizing path for foe relay K1 on the battery signal panel-indicator. Contacts 4–10 of K1 close, completing the energizing path for ready to fire relay K8 on the battery signal panel-indicator

(7) *FRIEND switch S2.* FRIEND switch S2 is a 2-position toggle switch spring-loaded to down position. With S2 in the FRIEND position, contacts 2–3 open, interrupting the lock-up circuit of foe relay K1 on the battery signal panel-indicator when K1 is energized. Contacts 5 6 of S2 open, interrupting the energizing path for burst relay K1 in the combining amplifier of the missile radar control console.

(8) *IFF GAIN variable resistors R3A and R3B.* IFF GAIN variable resistors R3A and R3B, which are on a common shaft, adjust the gain of the IFF control groups on the HIPAR and LOPAR. The adjustment of R3A and R3B varies the brightness of the reply signals and sharpens the reply image on the PPI.

(9) *RADAR SELECT switch S7.* RADAR SELECT switch S7 is a 2-position toggle switch which is used to select either the LOPAR or HIPAR.

48.5 (U). Alarm Control 9156414

a. General. The alarm control is a switching circuit used to energize an external indicator lamp to determine the power status of the HIPAR.

b. Detailed Theory.

(1) With no input at connector J1–A (fig. 85, TM 9–1430–257–20/1), relay K1 and transformer T1 remain deenergized. Since there is no voltage applied to the plate of voltage regulator V1, there is no difference in potential between connectors J1–C and J1 D

(2) After a 30-second time delay, ground is connected to J1–A, relay K1 is energized, and contacts 2–6 are closed. A 120-volt, 400-cps energizing voltage is then applied to T1 through terminals 1 3. When the polarity of the secondary voltage at terminal 4 is negative, current flows through crystal diode CR2, resistor R2, PWR SENS variable resistor R3, resistor R4, and into the secondary of T1 through terminal 6. Capacitor C1 charges negatively in proportion to the voltage drop across the lower part of R3 and all of R4.

(3) On the next alternation, terminal 4 of T1 is positive and the plate of CR1 is positive, allowing V1 to conduct according to the conduction level set by PWR SENS variable resistor R3.

(4) When a power monitoring signal is applied through connector J1–E and capacitor C3, the negative portions are clamped by CR3 and the positive portions are passed through CR4 and R8 to the junction of capacitor C2 and resistor R6.

(5) The voltages across capacitors C1 and C2 are added algebraically in the symmetrical network consisting of resistors R5 and R6. The resultant voltage is applied to the control grid of V1. Consequent current flow through V1 produces a voltage drop across V1 sufficient to illuminate the external HIPAR POWER indicator light DS2 on the HIPAR control-indicator.

(6) PWR SENS variable resistor R3 is adjusted so that HIPAR POWER indicator light DS2 is illuminated when the monitor voltage at connector J1–E reaches the correct level.

49 (U). STC 8512082

a. General. The STC generates a negative STC gate with an exponentially decaying trailing edge. This STC gate controls the gain of the acquisition receiver system over the first portion of the range of the acquisition radar system. This is done to reduce returned signals from nearby objects and thereby equalize signals from nearby and distant objects.

b. Detailed Theory.

(1) *Monostable multivibrator V1A and V1B.*

(a) *Quiescent operation.* A positive voltage is applied to the grid of monostable multivibrator V1A (fig. 22, TM 9–1430–257–20) from a series voltage divider composed of resistor R3, FLAT variable resistor R2, and resistor R1 from ground to the +150-volt supply. This potential can be varied by R2 from +13 volts to +5.8 volts. Capacitor C2 is connected from the brush arm of R2 to ground and stabilizes this potential. Since

the grid of monostable multivibrator V1B is returned through current limiting resistor R9 to +150 volts, a heavy current is drawn through V1B. This current develops a high positive potential across common cathode resistor R5, which biases V1A beyond cutoff.

(b) *Dynamic operation.* The positive preknock pulse at connector J1 is applied across a series capacitor voltage divider composed of C1 and C10 to ground. A large current flows in C1 and C10 at the leading edge of the preknock pulse, and the sharp rise in voltage across C10 insures accurate triggering of V1A. Since the positive pulse is superimposed on the positive voltage level set by R2, the current through V1A is determined by the setting of R2. This current determines the amplitude of the negative voltage coupled from the plate of V1A through capacitor C3 to the grid of V1B. The voltage, in turn, determines how long V1B remains cut-

off. FLAT variable resistor R2 permits the width of the positive output gate from V1B to be varied from 10 to 30 microseconds.

(2) *Paraphase amplifier V2A.*

(*a*) The positive gate from V1B is coupled through capacitor C4 to the grid of paraphase amplifier V2A. The voltage potential across cathode resistor R11 follows the rise in grid potential, and capacitor C5 charges to this potential through the low-forward resistance of crystal diodes CR1 and CR4. The potential across the cathode remains constant during the 10- to 30-microsecond gate. When the trailing edge of the positive gate passes, the voltage across R11 drops sharply, and capacitor C5 must discharge to this potential. Since the back impedance of CR1 and CR4 effectively presents an open circuit, C5 discharges exponentially through resistor R14 and DURATION variable resistor R13. The decay time of the output waveform across C5 can be varied from 2 to 1,000 microseconds by R13. The RC time constant of C5, R13, and R14 is 250 microseconds, and C5 is discharged for all practical purposes in 4 time constants or 1,000 microseconds. The resultant waveform across C5 is the STC gate. It has a flat top which can be varied from 10 to 30 microseconds and an exponentially decaying trailing edge which can be varied from 2 to 1,000 microseconds.

(*b*) In V2A, the positive gate from V1B is also inverted. A negative gate is coupled from the plate of V2A through isolating resistor R28 and through part of the external RECEIVER-STC variable resistor R1 (B4, fig. 21, TM 9–1430–257 20) to the plate of converter amplifier V2B (fig. 22, TM 9–1430–257 20)

(3) *Cathode follower V3A.* Cathode follower V3A provides isolation between the STC gate-forming network in the cathode output of V2A and the clipper network in the input of V2B. The STC gate is directly coupled from C5 through parasitic suppressor resistor R15 to the grid of V3A. A decreased amplitude STC gate is developed across cathode resistor R16 and coupled through capacitor C6 and parasitic suppressor resistor R20 to the grid of V2B.

(4) *Converter amplifier V2B.*

(*a*) With no signal applied, converter amplifier V2B is biased beyond cutoff by −9 volts applied to the grid by the voltage divider network composed of resistors R17 and R18 which are connected between ground and the −250-volt supply. The lower extremity of the positive STC gate is clamped to the −9-volt level by crystal diode CR2. Since V2B is biased beyond cutoff, it conducts only during the upper portion of the positive STC gate. This clipping action removes the lower extremity of the STC gate, thus reducing the width of the trailing edge of the input STC gate from 2–1,000 microseconds to 2–100 microseconds. Negative feedback developed across unbypassed cathode resistor R21, minimizes distortion, thus insuring accurate reproduction of the STC gate. However, this feedback also lowers stage gain considerably.

(*b*) In the plate circuit of V2B, the negative STC gate is developed across RECEIVER-STC variable resistor R1, located on the acquisition control-indicator. The negative output square wave from V2A is also coupled through R1 to the plate circuit of V2B. Since both waveforms are negative, they are additive. The amount of addition is determined by the setting of the brush arm of R1. If the brush arm of R1 is fully counterclockwise, R1 is effectively removed from the plate circuit of V2B since the plate is directly connected to the +150-volt supply. Consequently,

CONFIDENTIAL

the plate of V2B is at a constant potential, and the output waveform to V3B is the negative square wave from V2A (A, fig. 44). If the brush arm of R1 is fully clockwise, the full resistance of R1 is in the plate circuit of V2B. The addition of the two negative waveforms produces an STC gate with an increased negative step (B, fig. 44). With the brush arm of R1 at any intermediate position, a lower amplitude gate from V2B is added to the negative gate from V2A, producing a resultant STC gate to V3B with a negative step voltage of proportionately less amplitude (C, fig. 44).

(5) *Cathode follower V3B.*

(a) The grid of cathode follower V3B (fig. 22, TM 9–1430–257–20) is returned to +30 volts by means of a voltage divider consisting of resistors R23 and R22 connected between ground and the +150-volt supply. The +30-volt bias places V3B in the linear part of the tube characteristic curve. The biasing arrangement was necessitated by large-size cathode resistor R26, required for proper impedance matching to the IF preamplifier.

(b) The input waveform to V3B is a negative STC gate as explained in (4)(b) above. This STC gate is coupled through C7 and parasitic suppressor resistor R25. The STC gate drives the grid negative, resulting in a reduction of current through V3B and a reduced voltage drop across R26. Thus, the cathode follows the grid and a negative STC gate is coupled through capacitor C8 to connector P1–9. Crystal diode CR3 is connected between connector P1–9 and 11. A variable dc level (0 to
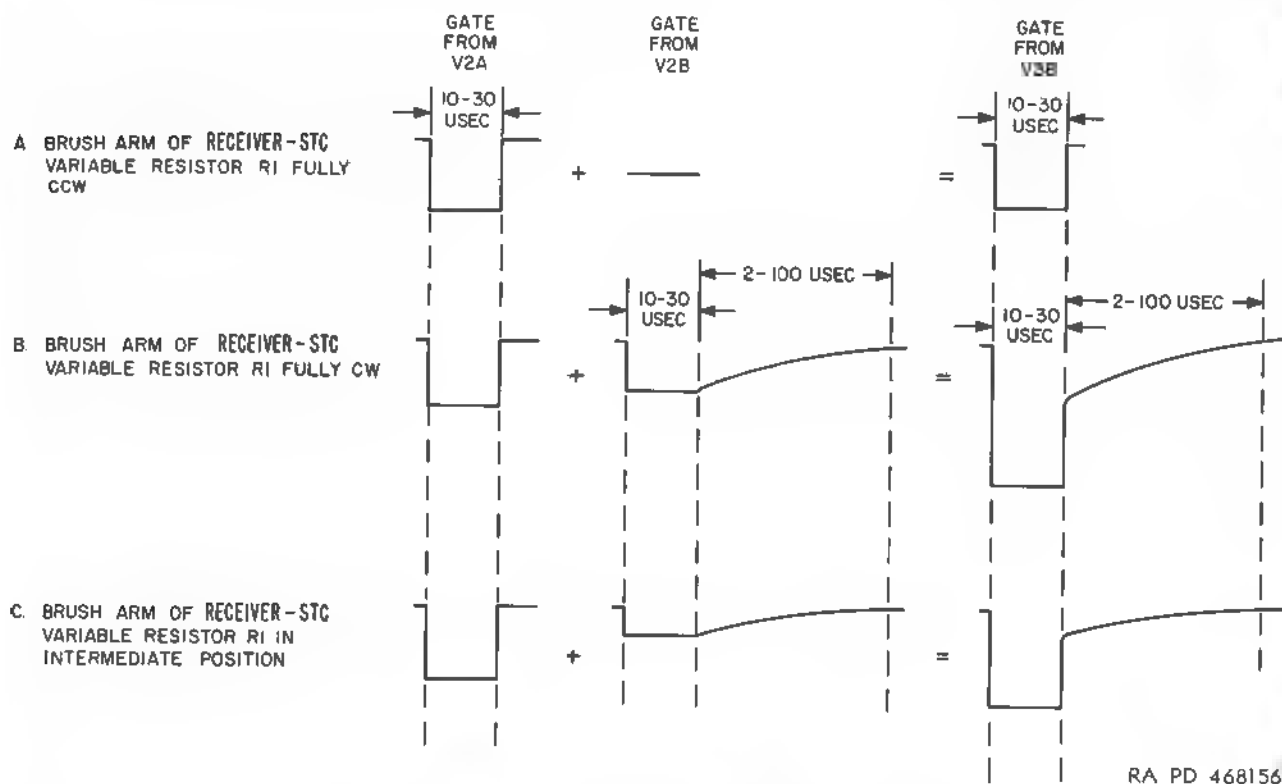
Figure 44. (U) Converter amplifier—addition of gates.

RA PD 468156

CONFIDENTIAL

−11 volts) is applied to the cathode of CR3 from P1-11. This level is determined by the setting of RECEIVER-GAIN variable resistor R3, located on the acquisition control-indicator. Diode CR3 conducts whenever the output STC gate at the plate of CR1 attempts to go positive with respect to this level. This action clamps the upper extremity of the negative STC waveform to the setting of RECEIVER-GAIN variable resistor R3.

50. PPI HV Power Supply 8518077, 9007757

a. General. The PPI HV power supply (fig. 17, TM 9-1430-257 20) furnishes the necessary high voltage to the plan-position and precision indicators of the battery control console. This unit contains three hermetically sealed power supplies PS1, PS2, and PS3, one hermetically sealed voltage regulator VR1, and two filament transformers T1 and T2. The individual power supplies furnish +1,550 volts dc, −8,000 volts dc, and +5,000 volts dc.

Note. Continuous reference in *b* below is made to figure 17, TM 9-1430-257 20 unless otherwise indicated.

b. Detailed Theory.

(1) The +1,550-volt supply, PS1 (fig. 45), uses 3-phase transformer T1, with Y-connected primary and secondary windings, and associated circuit components. A 400-cps, 3-phase input at connectors J1-K, L, and M is applied to the primary of T1 (fig. 45) between terminals 1, 2,

and 3. Connector J1 N and T1-4 are connected to neutral. The secondary of T1 is connected to the rectifier circuits. The rectifier circuits include six silicon crystal diodes connected in two Y-configurations producing full-wave rectification. Phases A, B, and C maintain a 120° phase relationship, thereby causing the diodes to conduct alternately. Output filtering is accomplished by an inductance-capacitance L-type filter network L1 and C1. The filtered 1,550-volt dc output appears across bleeder resistor R1 and PS1-5 and 6. Terminal PS1-5 is connected to J4 and PS1 6 is connected to frame ground. Voltage dividing resistors R1 and R2, located outside PS1, are connected in series between terminal 5 and frame ground and are in parallel with the +1,550-volt output. Output voltage developed across R2 is used to monitor the +1,550-volt output at J1-J.

(2) The input to terminals 1 and 2 of the −8,000-volt supply, PS2 (fig. 46), is from output terminals 3 and 4 of voltage regulator VR1 (fig. 47). Regulator VR1 furnishes a regulated 120-volt, 400-cps excitation voltage to the primary of transformer T1 (fig. 46). The secondary of T1 is connected to the rectifier circuit. The rectifier circuit consists of four silicon crystal diodes CR1, CR2, CR3, and CR4 connected as a full-wave bridge-rectifier. The output is filtered by two
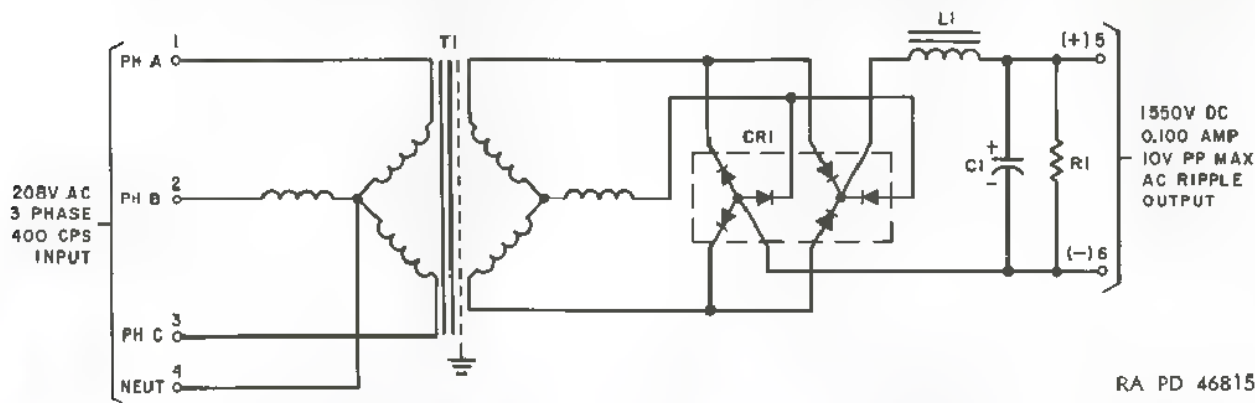
Figure 45 (1) +1,550-volt supply PS1 8519407—schematic diagram.

RA PD 468152

CONFIDENTIAL

resistance-capacitance L-type filters R1, C1 and R2, C2. The filtered −8,000-volt dc output appears across bleeder resistor R3 and PS2–3 and 4. Load limiting resistor R3 is connected in series between PS2–3 and J3. Terminal PS2–4 is connected to frame ground. Bypass capacitor C1 is connected in series between frame ground and J2. Both R3 and C1 are part of a decoupling network to provide a discharge path for the high voltage of the PPI immediately after the power has been turned off. This high voltage is discharged in the power supply chassis

rather than through the PPI chassis for the protection of the operator in the PPI position.

(3) The +5,000-volt supply, PS3 (fig. 48), uses single-phase transformer T1 and associated circuit components. A 120-volt, 400-cps input at connectors J1–A and N is applied across PS3 1 and 3 to the primary of T1 (fig. 48). The primary is tapped to permit adjusting for a slightly higher or lower output voltage. The secondary of T1 is connected to the rectifier circuit. The rectifier circuit consists of four silicon crystal diodes CR1
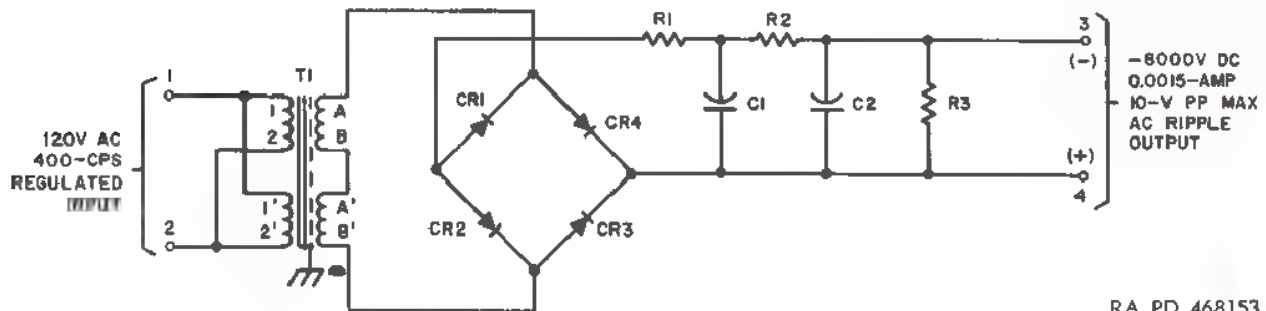
RA PD 468153

Figure 46. (U) −8,000-volt supply PS2 8519408—schematic diagram.
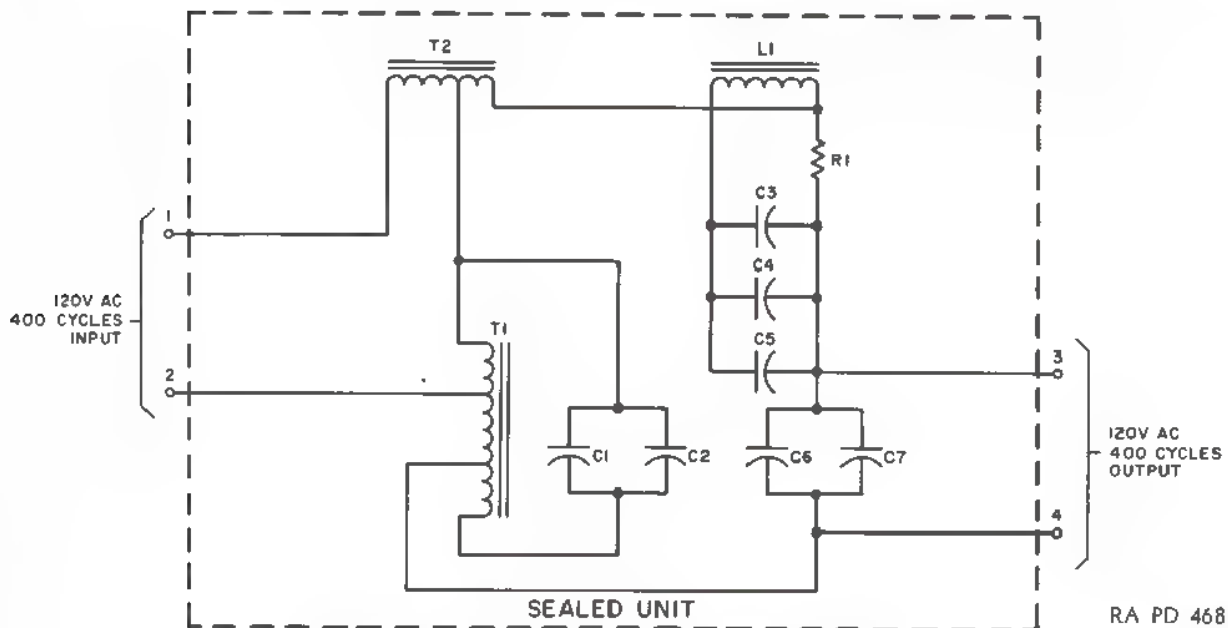
RA PD 468154

Figure 47. (U) Voltage regulator VR1 8519410—schematic diagram.

136

CONFIDENTIAL

and CR2 connected as a full-wave bridge-rectifier. Filtering is accomplished by two resistance-capacitance type filters R1, C1, R3 and R2, C2, R4. The filtered +5,000-volt dc output appears across bleeder resistor R5 and PS3-5 and 6. Terminal PS3-5 is connected to J7 and PS3-6 is connected to frame ground.

(4) The 120-volt, 400-cps voltage regulator VR1 (fig. 47) is used to maintain a constant value of voltage applied to the input of PS2 (fig. 46). A 120-volt, 400-cps input at connectors J1-A and N is applied across VR1-1 and 2 to auto-transformer T1 and T2 (fig. 47). Auto-transformer T1, and capacitors C1 and C2 compensate for any fluctuation of input voltage to stabilize the output voltage. Resistor R1, inductor L1, and capacitors C3, C4, and C5 compensate for any fluctuation of input frequency to stabilize the output voltage. Capacitors C6 and C7 correct any phase shift inherent in the voltage and frequency networks. The regulated voltage appears across VR1-3 and 4 and across PS2-1 and 2.

(5) Filament transformer T1 furnishes 6.3-volt, 400-cps filament voltage to the PPI cathode-ray tube in the battery control console. A 120-volt, 400-cps input at connectors J1-G and F is applied across T1-1 and 2. Terminals T1-3 and 4 of the secondary are connected to J5 and J6. The 6.3-volt, 400-cps output is superimposed on -8,000 volts dc.

(6) Filament transformer T2 furnishes 6.3-volt, 400-cps filament voltage to the PPI battery control console circuits. A 120-volt, 400-cps input at J1-F and G is applied across T2-1 and 2. The input is coupled through T2 to three secondary windings. The 6.3-volt, 400-cps output appears across connectors J8-A and B, C and F, and D and E. The 6.3-volt, 400-cps output across J8-D and E is superimposed on 150 volts dc.

51. 28V Power Supply 8512751 or 9906424

a. *General.* The -28v power supply (fig. 23, TM 9-1430-257-20) furnishes -28 volts at a maximum current of 5.0 amperes to various circuits in the battery control console, computer group, recorder group, utility cabinet, and the director station interconnecting box.

b. *Detailed Theory.* The input to the -28v power supply is a 120-volt, 400-cps voltage applied through connectors TB1-4 and 5. This input is applied to single-phase stepdown trans-
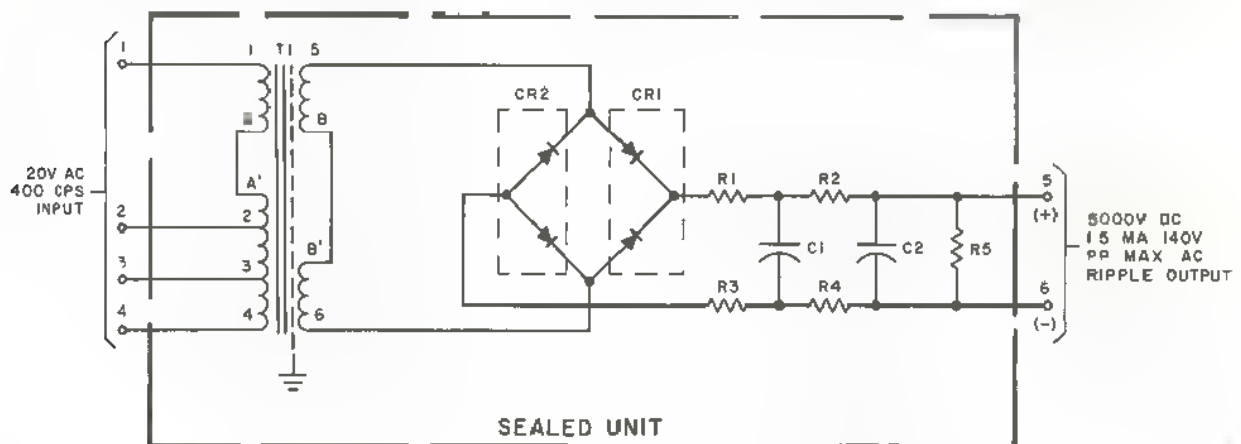
RA PD 468155

Figure 48 (U). +5,000-volt supply PS3 8519409—schematic diagram.

former T1 at T1–1 and 2. The secondary wind-
ing of T1 is tapped to permit adjustment of
-28 volts at the output of the power supply.
The stepped-down voltage from the secondary
winding of T1 is applied to a full-wave bridge
rectifier consisting of crystal diodes CR1, CR2,
CR3, and CR4. The rectified output is filtered
by an inductance-capacitance L-type filter net-
work L1 and C1. The —28-volt output appears
across capacitor C1 and TB1 1 and 2.

52. Miscellaneous Cabinet-Mounted Components in Battery Control Console 8173147

a. General. The miscellaneous cabinet-
mounted components in the battery control con-
sole are associated with various chassis in the
director-computer group.

b. Detailed Theory.

Note. The key letter-number combinations shown in
parentheses in (1) through (10) below refer to zone
locations on figure 3, TM 9 1430–257–20

(1) *Video alarm volume control variable
resistor R31.* The audio output from
transformer T1, located in the alarm
control of the director station group,
is applied across video alarm volume
control variable resistor R31 (A5)
and the video alarm speaker. The
amount of current shunted through
R31 determines the power output of
the video alarm speaker. An audible
tone from the video alarm speaker
alerts the battery control console op-
erator when a target is present in a
preset sector.

(2) *Foe, friend, battery relay K20.* Foe,
friend, battery relay K20 (C22) con-
sists of three individually operated re-
lays. The battery section of K20 is
operated during testing procedures or
during FUIF operation to allow the
PPI marker generator to produce a
defocus pulse on the PPI presentation.
The friend section of K20 is operated
during FUIF operation to allow the
PPI marker generator to produce a

semicircle concave down over the tar-
get video on the PPI presentation. The
foe section of K20 is operated during
FUIF operation to allow the PPI
marker generator to produce a circle
around the target video on the PPI
presentation. Varistors CR1, CR2,
and CR3 protect the coils of the sepa-
rate sections of K1 against arcing.

(3) *Interlock switches S21, S22, S23, S24,
and S25.* Interlock switches S22
(D23), S23, S24 (D20), and S25
(B11) all perform the same function.
Whenever any of the battery control
console doors are opened, one of the
switches opens the low-voltage supply
to the high-voltage circuits, thereby
interrupting high-voltage circuit op-
eration. This protects maintenance
personnel from possible injury due to
electric shock.

(4) *PPI blowers B1 and B2.* PPI blowers
B1 (B28) and B2 provide the proper
amount of forced air ventilation to the
equipment in the battery control con-
sole. Blowers B1 and B2 are operated
by 120 volts ac. Capacitors C2 and C3
provide the phase shift, between sta-
tor windings of blowers B1 and B2,
necessary for running the motors.

(5) *Filament transformer T1.* Filament
transformer T1 (A27) couples a regu-
lated 6.3 volts to filaments in the sweep
generator and PPI dc amplifiers. The
parallel circuit consisting of resistors
R32, R33, and R34 is connected in
parallel with the secondary of T1 and
is used to limit the current through
the filaments.

(6) *Status lamps I1, I2, I3, and I4.* Only
one of status lamps I1 (B6), I2, I3,
and I4, which are located above the
altitude plotting board of the battery
control console, can be illuminated at
a time. These status lamps are con-
trolled by alert status switch S3 lo-
cated on the tactical control-indica-
tor. Switch S3 provides a ground

for the −28-volt supply used for illuminating the status lamps.

(7) *Remote alarm buzzer I5.* Remote alarm buzzer I5 (A5), mounted on the cabinet behind the altitude plotting board, is sounded whenever a command is received from the anti-aircraft operation center (AAOC). At the same time that I5 operates, only one of the REMOTE, HOLD FIRE, and CEASE FIRE indicator lights on the tactical control-indicator of the battery control console will illuminate at a time. It is necessary to acknowledge the commands from the AAOC by closing ACKNOW switch S1 on the tactical control-indicator. When S1 is closed, I5 will cease to operate.

(8) *Resistors.* Two terminating resistors (B30), built into connectors, are provided for terminating the acquisition range mark and the sync pulse. The sync pulse is terminated through the resistor in connector P51 and the acquisition range mark through the resistor in connector P43.

(9) *Telephone circuitry.* TECH switch S11 (D24) switches the battery control console operator's telephone from the TECH loop to the command loop. Ring switches S12 (D21), S13, and S14 (D22) are telephone ringing switches for signalling the telephone operator.

(10) *Telephone set TA-272/G 8010134.* Telephone set TA-272/G (C22) with a handset-headset and a telephone connecting station comprise a console telephone station. Six console telephone stations are used throughout the radar course directing central to facilitate voice communication.

    Note. Refer to figure 60, TM 9-1400-251-12 for the circuits discussed in (*a*) and (*b*) below.

(*a*) *Transmit operation.*

    1. A −24-volt dc voltage from a telephone talking battery is applied through connector E301-G to winding 1-2 of filter choke L301.

The circuit continues through E301-E, connector J13-E in the telephone connecting station, connector P401-E and telephone push to-talk switch S401 on the handset-head-set to the telephone transmitter. The −24-volt dc circuit is completed through P401-C, J13-C, J13-A, E301-A, winding 3-4 of L301, and E301-BT to ground.

2. With S401 in the TELEPHONE TALK position, the −24-volt dc talking battery current is voice modulated. The voice frequency modulation is applied through connectors P401-D, J13-D, E301-D, and capacitor C301 to transmitter winding 4-5 of voice frequency transformer T301. Voice frequency voltage induced across winding 1-3 of T301 is applied through capacitor C303 to connector for E301-L2 and to connector E301-L1 for transmission by telephone line to the switchboard located in the recorder group in the trailer-mounted director station. Side tone voltage is induced in receiver winding 5-6 of T301 and applied through connectors E301-A, J13-A, P401-A, and connectors E301-B, J13-B, and P401-B to the telephone receiver.

3. With S401 in RADIO CONTROL position, a 24-volt dc radio control voltage is applied through E301-L1, holding coil L302, connectors E301-F, J13-E, P401-F, S401, P401-H, J13-H, and E301-L2. The 24-volt dc radio control voltage is blocked by capacitors C302 and C303. Voice frequency induced in winding 1-3 of T301 appears across L302 to modulate the 24-volt dc radio control voltage.

(*b*) *Receive operation*

1. Ringer I301 is operated by a 20-cycle ring voltage applied to E301-L1 and E301-L2. The ring voltage is coupled through C302 to I301

2. Voice frequencies transmitted by the telephone line are applied through E301-L1, E301-L2, and C303 to winding 1-3 of T301. Voice frequency voltage induced in winding 5-6 of T301 is applied through E301-A, J13-A, P401-A, E301-B, J13-B, and P401-B to the telephone receiver. Varistor CR302 suppresses receiver noises caused by ringing voltages and spurious line noises.

(11) *EJECT TRAINER switch S26.* EJECT TRAINER switch S26, when depressed, operates relays K1 and K2 (fig. 46, TM 9-1430-257-20) which disconnects radar signal simulator AN MPQ-36 from the trailer mounted director station and the trailer mounted tracking station.

(12) *EJECT TRAINER indicator light I6.* EJECT TRAINER indicator light I6, when illuminated, indicates that either one or both of the cables from the radar signal simulator are connected. When both cables are disconnected, indicator light I6 is extinguished.

c. Differences Among Models.

(1) *DA MWO 9-1430-251-30, 8.* Connector J60 (C31, fig. 3, TM 9-1430-257-20) is added to battery control console 8173147 of certain selected systems by DA MWO 9-1430-251-30/8. Connector J60 is provided so that a radar bomb scoring box may be connected to the battery control console and thus provide facilities for radar bomb scoring.

(2) *DA MWO 9-1400-263-30.* Auxiliary acquisition coaxial relay assembly 9985722 is added to battery control console 8173147 of certain selected systems by DA MWO 9-1400-263-30. Coaxial relays K1, K2, and K3 in the auxiliary acquisition coaxial relay assembly (A38, fig. 3.1, TM 9-1430-257-20) switch the acquisition preknock and sync pulses from the NAR (Nike acquisition radar) to the AAR (auxiliary acquisition radar) where the AAR is selected.

(3) *DA MWO 9-1400-268-50.* This MWO may be applied to 125 selected systems which may or may not have DA MWO 9-1400-263-30 applied. Acquisition control-indicator 9985604 is replaced by acquisition control-indicator 9988650. Miscellaneous wires, cables, and connectors are added. Refer to figure 3.2, TM 9-1430-257-20 for the schematic of systems without MWO 9-1400-263-30 applied and to figure 3.3, TM 9-1430-257-20 for the schematic of systems with MWO 9-1400-263-30 applied.

52.1 (U). Miscellaneous Cabinet-Mounted Components in Battery Control Console 9143989

a. General. The miscellaneous cabinet-mounted components in the battery control console are associated with various chassis in the director-computer group.

b. Detailed Theory. The theory of the miscellaneous cabinet-mounted components (fig. 71, TM 9-1430-257-20) is the same as that described in paragraph 52 except for the video alarm volume control variable resistor R31 which is no longer cabinet mounted.

c. Differences Among Models. Connector J60 (C31, fig. 71, TM 9-1430-257-20) is added to battery control console 9143989 of certain selected systems by DA MWO 9-1430-251-30 8. Connector J60 is provided so that a radar bomb scoring box may be connected to the battery control console and thus provide facilities for radar bomb scoring.

52.2 (U). Auxiliary Acquisition Relay Assembly 9985525

Auxiliary acquisition relay assembly 9985525 (fig. 24.1, TM 9-1430-257-20) contains 18 relays which are used to switch various functions from the NAR (Nike acquisition radar) to the AAR (auxiliary acquisition radar) when the AAR is selected. For functional theory of relay operation, refer to TM 9-1430-250-20

CHAPTER 4 (U)

ACQUISITION ANTENNA PEDESTAL

53 (U). Acquisition Antenna Pedestal 8513363, 9002671, 9156545

a. General.

(1) The main function of the acquisition antenna pedestal is to provide motive power for rotating the antenna in azimuth. Other functions include transfer of rf energy, transfer of control signals, and facilities for orientation of the acquisition antenna during emplacement.

(2) Motive power is furnished by an electric motor coupled to the antenna through the acquisition antenna drive In systems 1001 through 1020, acquisition antenna drive 8515267 and motor 8515037 are used. In systems 1021 through 1059, acquisition antenna drive 8513894 and motor 9010200 are used. Because of the change in acquisition antenna drives and motors, the acquisition antenna pedestal is modified to 9002761. The pedestals are not interchangeable. The difference between the two antenna drives is discussed in paragraph 54

(3) A positive means for transferring maximum rf energy and control signals, between stationary and rotating elements of the antenna, is accomplished by the rotary coupler and the acquisition slip-ring, respectively. Pressurization of the rotary coupler is performed by the compressor, and amplification of antenna position voltages is accomplished in the resolver amplifier. The acquisition resolver generates the antenna position voltages

(4) The acquisition orientation level is maintenance equipment used only during emplacement or periodic reorientation of the antenna

(5) Acquisition antenna pedestal 9156545 is modified for use with the antijam display receiver by MWO 9-1400-268-

50 and is incorporated in production at system 1363.

b. Detailed Theory.

(1) The main power to the acquisition antenna pedestal is applied from the external acquisition power control panel As shown schematically in figure 60, TM 9-1430-257-20, the 3-phase, 208-volt, 400-cps voltage is applied through AC POWER connector J1-1, 4, and 9 to the motor-speed control panel and to the compressor. The neutral for the supply voltage is returned through J1-16.

(2) A 4-kc excitation voltage is applied from the external 4-kc oscillator through J1-27 and 28 to acquisition azimuth resolver B2. This resolver is mechanically linked with acquisition drive motor B1 and rotates at the same rate as the acquisition antenna. The modulated 4-kc signal output from the rotor of B2 is connected through connector J6-1 and 2 to the input of the resolver amplifier. A 120-volt, 400-cps, phase A voltage is applied through J1-2, 7, and 12 to the resolver amplifier. The neutral is returned through J1-3, 8, and 13. These terminals on each leg are used to increase the current-carrying capacitor of the connection. The modulated 4-kc signal output from the resolver amplifier is applied through J6-5 and 9 and CONTROL connector J2-33 and 35 to the external target designate control-indicator. Interlock switch S3 is opened when the acquisition antenna pedestal cover is removed. This disconnects the +250-volt supply to the resolver amplifier.

(3) Antenna disable switch S1 is located under a protective cover on the side of the pedestal. The normally closed contacts are in series with −28 volts applied

through connector J3–21. When S1 is operated, the operating potential is removed from the relays of the motor-speed control panel, and the acquisition drive motor is immobilized so that maintenance may be performed in the acquisition antenna pedestal without danger to personnel. Motor-speed control panel interlock switch S4 is also in series with the −28-volt supply. When the motor-speed control panel is removed, S4 operates, and power to the acquisition drive motor is removed so that maintenance may be performed without danger to personnel.

(4) Three relays and associated wiring make up the motor-speed control panel. The −28 volts is applied to one side of each relay. When a given relay is operated, it applies the 3-phase, 208-volt, 400-cps power to the specific winding in the motor related to the relay. A varistor is connected across each of the relay coils to provide an effective short circuit for any pulse or voltage developed in the relay coils. This prevents arcing across the switch or relay contacts. A varistor decreases resistance with an increase in the applied voltage, and it is this characteristic which bypasses the transient surge voltages.

(5) The operation of the motor-speed control panel (fig. 49) is as follows. When ANTENNA AZIMUTH RPM switch S7 in the acquisition control-indicator is in the OFF position, all relays are de-energized. In this position, no power is applied to the motor windings and the antenna is not rotated. The main power to the acquisition antenna pedestal is applied through ACQ MOTORS switch S5 located on the acquisition power control panel. With S7 in the 5 position, the switch arm of S7A connects ground terminal 10 to terminal 7. The circuit is then completed through 5-rpm relay K1 and relay contacts 4 and 3 of 15-rpm relay K3, and 1 and 2 of 10-rpm relay K2 to the −28-volt supply. The 5-rpm relay

K1 closes and applies 208-volt, 3-phase, 400-cps power from the acquisition power control panel to the 5-rpm windings of the acquisition drive motor; the antenna now rotates in 5 rpm. When S7 is placed in the 10 position, K1 is deenergized and ground is connected to the coil of K2. The circuit is completed through contacts 2 and 1 of K3, and 3 and 4 of K1 to the −28-volt supply. The 10-rpm relay K2 closes and applies power to the 10-rpm windings of the motor; the antenna now rotates at 10 rpm. When S7 is placed in the 15 position, K2 is deenergized and ground is connected to the coil of 15-rpm relay K3. The circuit is completed through contacts 2 and 1 of K1, and 1 and 2 of K2 to the −28-volt supply. Relay K3 closes and applies power to the 15-rpm windings of the motor; the antenna now rotates at 15 rpm. At no time can more than one relay be energized, since energizing a given relay disables the other two relays. This prevents more than one set of windings in the drive motor from being energized at any one time.

(6) The acquisition drive motor contains three sets of fields, each set energized through its related relay in the motor-speed control panel. The three sets of fields produce three speeds of rotation through one common armature. The motor is a 3-phase, 3-speed, 208-volt, 400-cps, constant torque, 4-horsepower, ac induction motor of the squirrel-cage type. The motor is located beneath the turntable and gear reduction box in the acquisition antenna drive. The operating characteristics of drive motor 8515037 are listed in table IV. Beginning with system 1021, motor 9010200 replaces motor 8515037. The difference between the two is that motor 9010200 is faster than motor 8515037. The operating characteristics of motor 9010200 are listed in table V. The motors are not interchangeable.
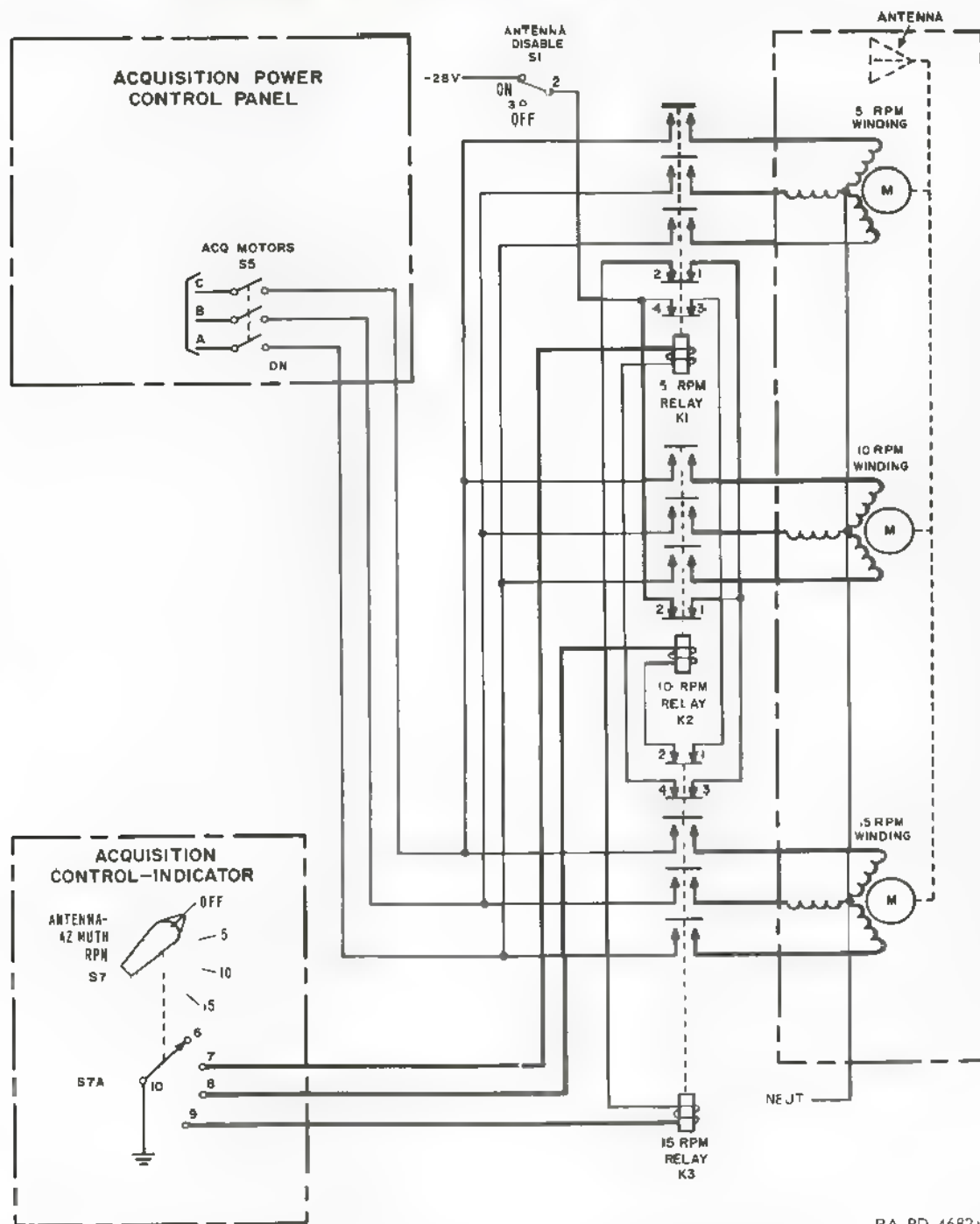
Figure 49 (U) Motor-speed control panel—simplified schematic diagram

RA PD 468210

CONFIDENTIAL

Table IV. *Motor 8515037 Characteristics*

Antenna speed	Motor speed	Horsepower	Current flow
5 rpm_____	1,650 rpm_____	0. 375	9 5 amp
10 rpm_____	3,600 rpm_____	0. 75	7.0 amp
15 rpm_____	5,600 rpm_____	1 2	7.0 amp

Table V   *Motor 9010200 Characteristics*

Antenna speed	Motor speed	Horsepower	Current flow
5 rpm_____	3,600 rpm_____	0. 75	6.0 amp
10 rpm_____	7,200 rpm	1. 5	8 0 amp
15 rpm_____	10,800 rpm_____	4. 0	19 0 amp

(7) The motor drives the acquisition antenna drive, which in turn drives the acquisition antenna, the rotary coupler, the acquisition slipring, and acquisition azimuth resolver B2.

54. Acquisition Antenna Drive 8515267, 8513894

a. General. The acquisition antenna drive is a mechanical linkage between the acquisition drive motor and the acquisition antenna. The linkage consists of gears which provide a 30 to 1 step-down ratio. Included in the linkage is a slip clutch which protects the motor from burnout in case the rotating mechanisms become jammed. The antenna drive is contained in an oil-filled gear reduction box, sealed to prevent entry of dust and to reduce noise level.

b. Detailed Theory.

(1) Power is applied to the acquisition drive motor through connector J1 (fig. 60, TM 9–1430–257 20). The motor converts electrical power to mechanical power which rotates the output drive sprocket.

(2) The motor armature pinion extends into the antenna drive assembly when the antenna drive assembly and the motor are joined together. Oil can be added to the interior of the housing or can be drained by removing a pipe plug threaded into the side of the housing. The level of oil within the housing can be ascertained through the window of the oil gage.

(3) The motor armature pinion (fig. 50) is extended into the antenna drive housing and meshes with the small gear. The shafts of the gears rotate in their respective ball bearings mounted in the orifices of the cover and housing. With the motor rotating at 1,650 rpm, the motor armature pinion drives the small gear. A smaller gear on the shaft of the small gear drives the large gear assembly which also has a small 15-tooth gear used to drive the 84-tooth gear. This 30 to 1 reduction gear linkage turns the drive sprocket at 120 rpm. The slip clutch is contained in the large gear assembly. Power is applied to the 60-tooth gear. As the gear rotates, it transmits the power through the spring to the collar. The spring offset fits into a slot on the collar to provide a positive connection. The spline of the 15 tooth gear fits into the collar, causing the 15-tooth gear to rotate at the same rate as the 60-tooth gear. In the event of overload or jamming, slippage occurs between the 60 tooth gear and spring, thus immobilizing the 15-tooth gear.

(4) The dotted line in figure 50 shows the power path from the acquisition drive motor to the drive sprocket. The power from the motor armature is coupled from the motor armature pinion to the small gear. After a speed reduction, the path continues from the small gear to the large gear. After another speed reduction, the path continued from the large gear to the 84-tooth gear and on to the drive sprocket.

(5) When the acquisition antenna drive (fig. 51) is placed in the acquisition antenna pedestal, the drive sprocket meshes with the idler gear. In turn, the idler gear meshes with the large ring gear which is bolted to the turntable. Since the antenna is also bolted to the turntable, its rotational motion is dependent upon motive power provided by the acquisition drive motor.

144

CONFIDENTIAL

IDLER GEAR

TO ANTENNA

DRIVE SPROCKET

LARGE RING GEAR

84-TOOTH GEAR

LARGE GEAR

SMALL GEAR

MOTOR ARMATURE PINION

FROM MOTOR
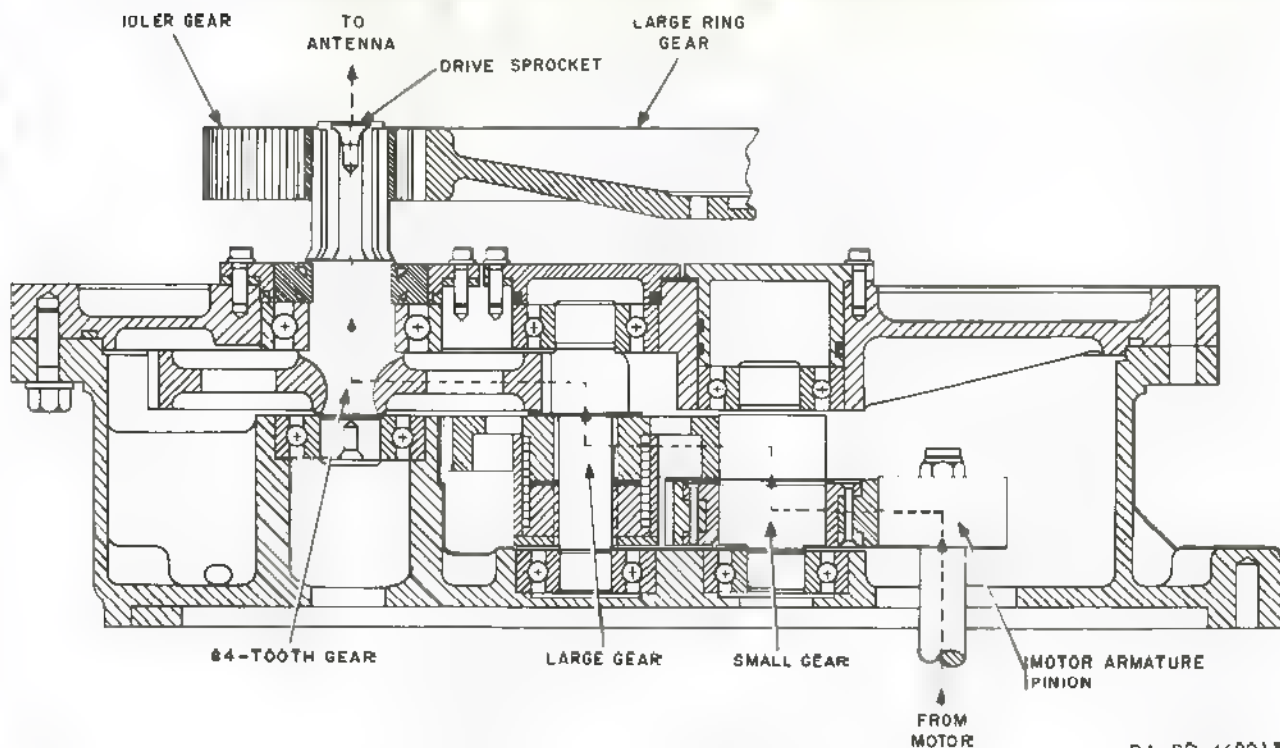
RA PD 468211

Figure 50 (U) Antenna drive—power path

c. *Antenna Drive 8513894.* Beginning with system 1021, antenna drive 8515267 is replaced by antenna drive 8513894. Because of the change in speed of the motor (par. 53*b*(6)), the following gear changes are incorporated in antenna drive 8513894. The large and 84-tooth gears (fig. 50) are replaced by speed-decrease gear assemblies 8513899 and 8513903, respectively. The purpose of the change between antenna drive 8515267 and antenna drive 8513894 is to provide an antenna drive which will operate satisfactorily in high winds. Antenna drives 8515267 and 8513894 are mechanically similar, but are not interchangeable.

55. Acquisition Slipring 7620498

a. *General.*

(1) The acquisition slipring (fig. 52) contains a series of continuous conducting rings compactly stacked to fit in a small space. The assembly serves as an electrical connector between components located in the stationary portion and components located in the rotating portion of the acquisition antenna pedestal.

(2) The brush contacts of the slipring are made from a precious metal alloy and the rings are made from fused gold, silver, and nickel. These metals are used because of their excellent conductive capabilities.

(3) The slipring consists of inner and outer subassemblies. The inner subassembly, which remains stationary, contains 24 continuous conducting rings. The outer subassembly, which rotates at antenna speed, contains brush contacts for each continuous conducting ring.

(4) The slipring transfers elevation drive data, IFF sync pulses, IFF power, IFF control data, and IFF video pulses between stationary and moving elements of the antenna pedestal.

b. *Detailed Theory.*

(1) Six groups of brush contacts are stacked

145

TURNTABLE

LARGE
RING
GEAR

ACQUISITION
ANTENNA
PEDESTAL

IDLER
GEAR

DRIVE
SPROCKET

DRIVE
SPROCKET

ACQUISITION
ANTENNA
DRIVE

ACQUISITION
DRIVE
MOTOR

INCHES
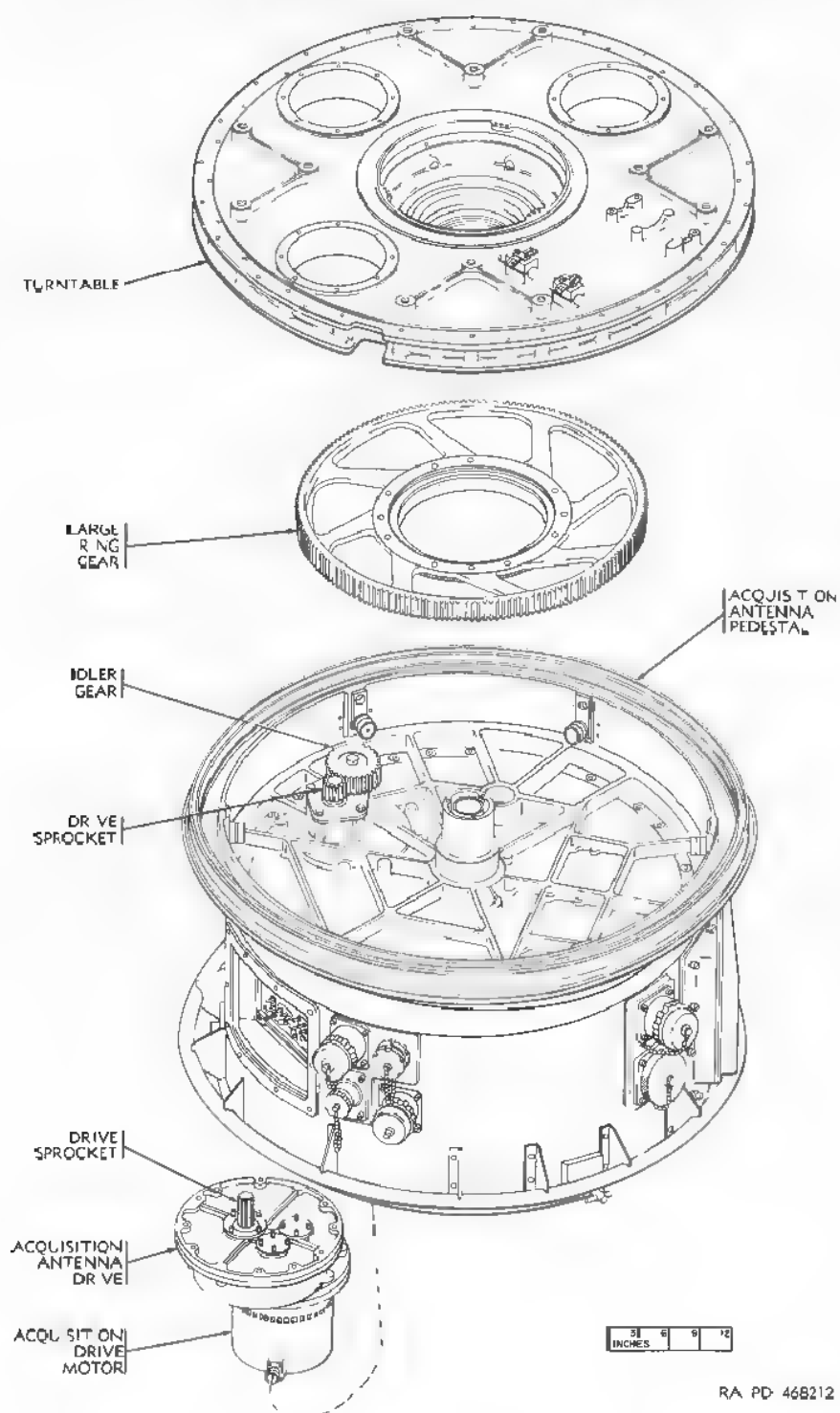
RA PD 468212

Figure 51. (U) Acquisition antenna pedestal—partial exploded view.

C
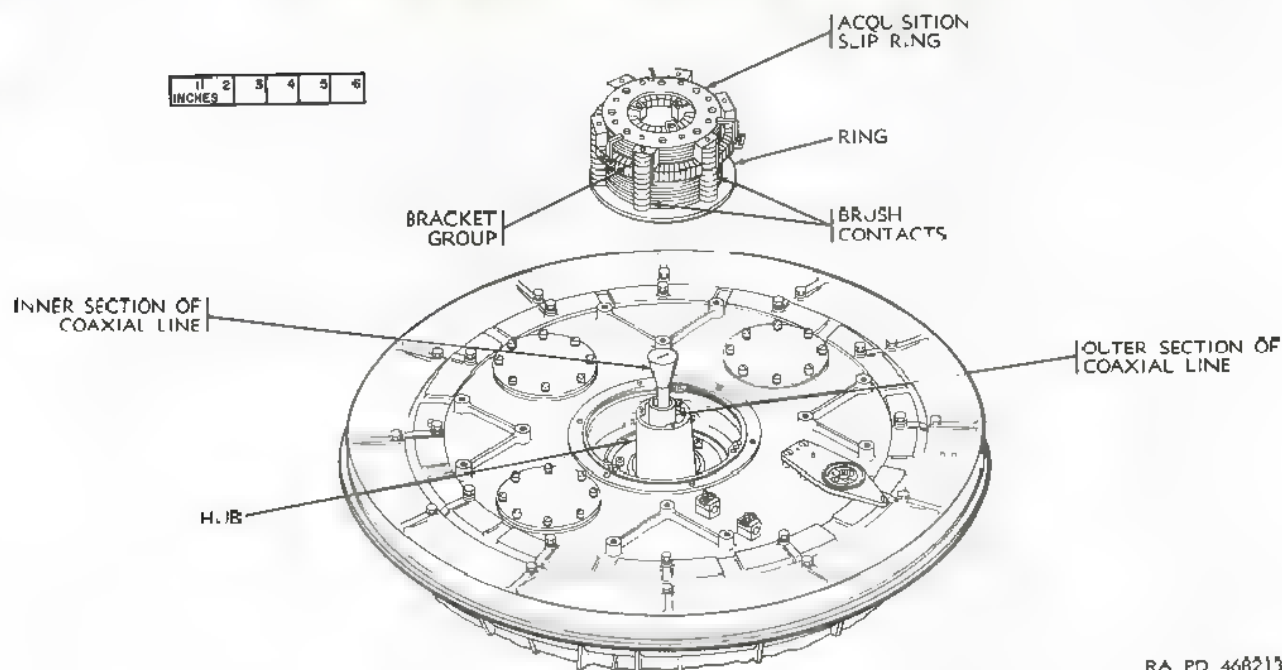
Figure 52. (U) Acquisition slipring—location.

RA PD 468213

to sit vertically on the ring and are held down by the bracket group. The bracket group contains the terminals of the brush contacts plus connectors of IFF sync and IFF video.

(2) The location of the slipring in the acquisition antenna pedestal is shown in figure 52. It is inserted into a cavity on top of the turntable. The inner section of the coaxial line, the outer section of the coaxial line, and the hub are extended upward through the center of the slipring.

(3) Figure 60, TM 9–1430 257–20 shows the manner in which the slipring inner circle TB5 and outer circle TB6 terminals are connected to connectors J2, J3, J4, P1, P11, P12, P13, P14, and P15 in the acquisition antenna pedestal.

56. Resolver Amplifier 7620653

a. *General.*

(1) The resolver amplifier provides sufficient power amplification of the acquisition azimuth resolver signal to drive resolvers in the acquisition and target tracking radar systems.

(2) The resolver amplifier contains two channels, a north-south (N–S) and an east-west (E–W) channel. Since both channels are identical, only the north-south (N–S) channel will be discussed.

b. *Detailed Theory.*

(1) The 4-kc signal at connector P1–1 (fig. 61, TM 9–1430 257–20) is coupled to the control grid of voltage amplifier V1 through the RC circuit of R1 and C6. The amplifier output from the plate of V1 is coupled through capacitor C3 to the control grid of power amplifier V2. The amplified output at the plate of V2 is coupled through transformer T2 to P1–5 and 7.

(2) A portion of the output signal is returned to the grid of V1 through RC network R2 and C7 from terminal 1 of T2 to provide degenerative feedback. Capacitor C6 shifts the phase of the input signal, and C7 shifts the phase of the

feedback voltage to maintain a constant 180° phase relationship between the two 4 kc signals.

(3) Voltage amplifier V1 is a conventional voltage amplifier. Cathode bias is provided by resistor R3 and cathode bypass capacitor C5. Screen voltage is dropped through resistor R5 with capacitor C2 acting as screen bypass. The amplified signal at the plate of V1 is developed across resistor R4 and coupled through C3 to V2.

(4) Amplifier V2 serves as a power amplifier. Cathode bias is developed across resistor R6 and cathode bypass is provided by capacitor C8. Screen voltage is dropped across resistor R8 with capacitor C1 acting as screen bypass. Plate voltage is supplied through R8, the primary of T2, and resistor R7 in series. Resistor R7 is a parasitic suppressor. The output of V2 is fed through T2 to P1-5 and 7.

(5) Transformer T2 is electrostatically shielded. Capacitor-resistor network C9 and R10 across the primary winding of

T2 compensates for the reactive effect of the winding. Capacitor-resistor network C4 and R21 across the secondary winding of T2 performs a similar function to prevent phase shift.

57. Rotary Coupler 8019245

a. General. The function of the rotary coupler (fig. 53) is to couple RF energy between the stationary portion of the acquisition antenna pedestal and the rotating antenna. If necessary, the rotary waveguide can be pressurized to prevent internal arcing.

b. Detailed Theory.

(1) A cross-sectional view of the rotary coupler is shown in figure 54. RF energy is coupled from the duplexer through a flexible waveguide to the lower choke joint shown in the figure.

(2) A choke joint used with rectangular waveguides has a slot (A–B) one-quarter wavelength (B–C) from the broad face of the waveguide. When energy attempts to leak out of the wave guide at the joint, standing waves are set up in
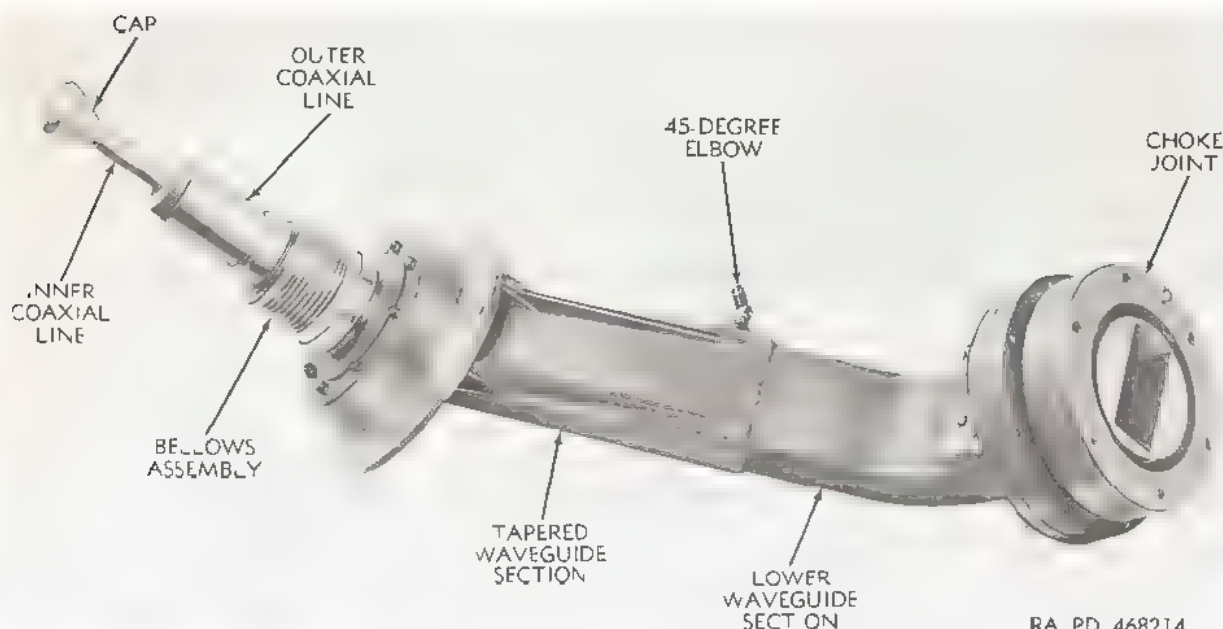
CAP
OUTER COAXIAL LINE
45-DEGREE ELBOW
CHOKE JOINT
INNER COAXIAL LINE
BELLOWS ASSEMBLY
TAPERED WAVEGUIDE SECTION
LOWER WAVEGUIDE SECTION
RA PD 468214

Figure 53. (U) Rotary coupler—lower section.

KNOB
JUNCTION

CAP

INNER SECTION
OF COAXIAL
LINE

RESONANT
CAVITY

LOWER SECTION
OF COAXIAL
LINE

"OIL CAN"
JUNCTION

LOWER WAVE-
GUIDE SECTION

UPPER
WAVEGUIDE
SECTION

UPPER SECTION
OF COAXIAL LINE

OUTER SECTION
OF COAXIAL LINE

HYDRAULIC
"O" RING

BELLOWS
ASSEMBLY

TAPERED
WAVEGUIDE
SECTION

45-DEGREE
ELBOW

WINDOW

RF TO
ANTENNA

UPPER
CHOKE
JOINT

LESS THAN $\frac{\lambda}{10}$ $\frac{\lambda}{4}$

B   A

$\frac{\lambda}{4}$

E   D

LOWER
CHOKE
JOINT

WINDOW

RF
FROM
DUPLEXER

VALVE

RA PD 468215

Figure 54 (U). Rotary coupler—cross section.

these quarter-wave sections The short circuit at (A) is reflected to (B) as a high impedance. The high impedance is transformed to a low impedance across the quarter-wave section (B-C). This occurs because the addition of the two quarter-wave standing wave sections effectively short-circuits points (D-E) in spite of the fact that there is no metallic connection between the points.

(3) The principle of the choke joint is especially useful when it becomes necessary to insert separators such as the windows shown in the lower and upper choke joint. The lower waveguide section is rectangular and contains an air pressure input 45 elbow. A valve in the lower choke joint provides a means for releasing the air pressure Energy from the duplexer is directed through the lower choke point, the window, and the tapered waveguide section to the lower section of the coaxial line. The tapered waveguide termination is called the "oil can" junction because of its shape. The inner conductor of the coaxial line is rigidly mounted on the "oil can" and extends through the lower section of the coaxial line. The tapered waveguide section is evenly split into two dissimilar paths at the "oil can" junction. The difference between the two paths is equivalent to one-half wavelength and provides the proper impedance match between the tapered waveguide section and the coaxial line. The RF energy is conducted through the coaxial line, around the cap, and is reflected by the knob junction in the upper waveguide section. An upper choke joint, similar to the lower choke joint, terminates the upper waveguide section and provides proper coupling to the antenna waveguide

(4) It is necessary that the connections between the stationary waveguide and the rotating antenna fit tightly at the point where they join. The connection portion of the joint consists of two cylindrical metallic sections placed so that the smaller section fits snugly inside the larger upper section. A third cylindrical section, called the bellows assembly, is placed around the lower section of the rotary joint at the lower end of the upper section. This flexible assembly contains two hydraulic O-rings which are provided to keep the joint airtight so that the entire RF conducting area, within the rotary coupler, may be pressurized. A window located in each of the choke joints is pressure tight for the same reason.

(5) The upper section of the rotary joint contains two small resonant cavities which are designed to prevent RF leakage through the seam where the upper and lower sections fit together. These cavities are one-quarter wavelength long and are placed so that they reflect an effective short circuit across the gap where the two sections of the joint meet. This is the same principle employed in the choke joints and thus causes the inner walls of the rotary joint to appear as an unbroken path for the RF energy conducted to the antenna.

57.1 (U). Rotary Coupler 9156621

a. *General.* The function of the rotary coupler is to couple RF energy between the stationary portion of the acquisition antenna pedestal and the rotating antenna. To accomplish this, the rotary coupler utilizes two isolated channels; one with high power and the other with low power handling capabilities. The high power channel provides a path for main antenna receiving and transmitting, while the low power channel provides a path for the auxiliary antenna received energy which is used in the JS receiver. High power channel insertion loss is a maximum of 0.1 db, while low power channel maximum loss is 0.3 db. Isolation between channels is a minimum of 90 db. If necessary, the rotary waveguide can be pressurized to prevent internal arcing.

b. *Detailed Theory.*

(1) A cross sectional view of the rotary coupler is shown in figure 54.1. RF

energy is coupled from the duplexer through a flexible waveguide to the lower choke joint shown in the figure. For theory of the choke joints and electrical theory of the rotary joint for the normal acquisition antenna refer to paragraph 57.

(2) The inner section of coaxial line in conjunction with the outer section of the rotary coupler together form a dual concentric coaxial transmission line. The outer section is used as the high power channel, while the inner section is used as the low power channel.

58 (U). Compressor 7605715 or Pressurization Unit 9138649

a. General. The compressor (fig. 55) is a compact pressurization unit used to maintain the rotary coupler under pressure to prevent arcing within the waveguides. Arcing within the waveguide may be caused by an increase in power output, by a decrease in atmospheric pressure within the waveguide, or by rough or dirty walls within the waveguide.

b. Detailed Theory.

(1) A —28-volt potential is applied through P1-H and power switch S1 (fig. 60, TM 9-1430-257-20). When S1 is operated to the ON position, the —28 volts is applied through normally closed operate pressure switch S2 and safety pressure switch S3 to start relay K1. Relay K1 and power indicator light I1 are returned to ground through connector P1-C.

RF FROM
AUXILIARY →
ANTENNA

RF TO
ANTENNA

RF TO
NOISE
GENERATOR

LESS THAN $\frac{\lambda}{10}$

$\frac{\lambda}{4}$

RF FROM
DUPLEXER

ORD G87647
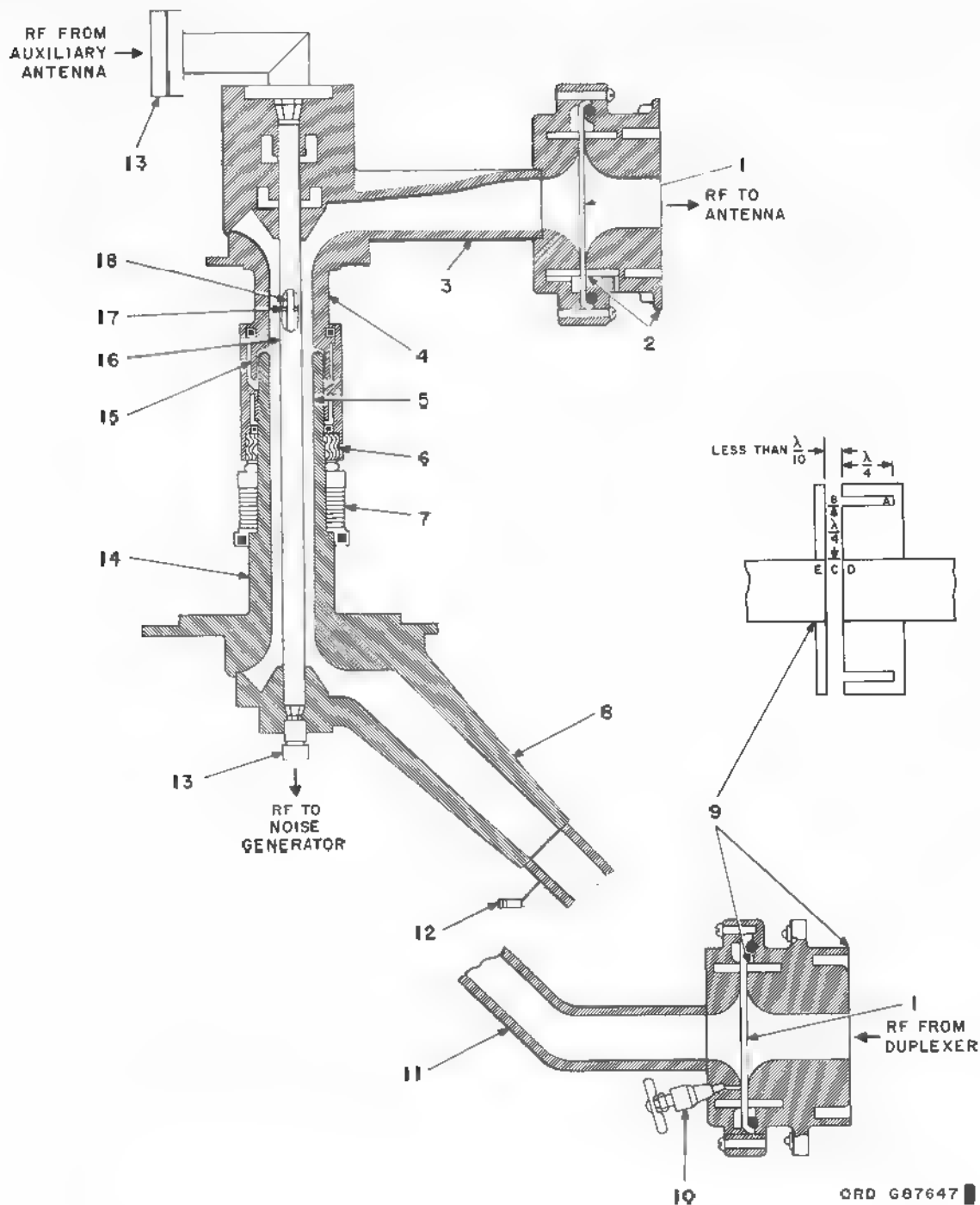
1—Window
2—Upper choke joint
3—Upper waveguide section
4—Upper section of coaxial line
5—Outer section of coaxial line
6—Hydraulic "O" ring
7—Bellows assembly
8—Tapered waveguide section
9—Lower choke joint

10—Valve
11—Lower waveguide section
12—45-degree elbow
13—Cap
14—Lower section of coaxial line
15—Resonant cavity
16—Inner section of coaxial line
17—Insulator
18—Inner coaxial conductor

Figure 54.1 (U). Rotary coupler - cross section—used with AAR.

FUSES
F1 F2 F3

IND CATOR
L GHT I

POWER
SWITCH S

PRESS
METER MI

CONNECTOR PI

PRESSURE
SWITCHES S2, S3

COMPRESSOR

START
RELAY K1

COMPRESSOR
MOTOR B1

INCHES
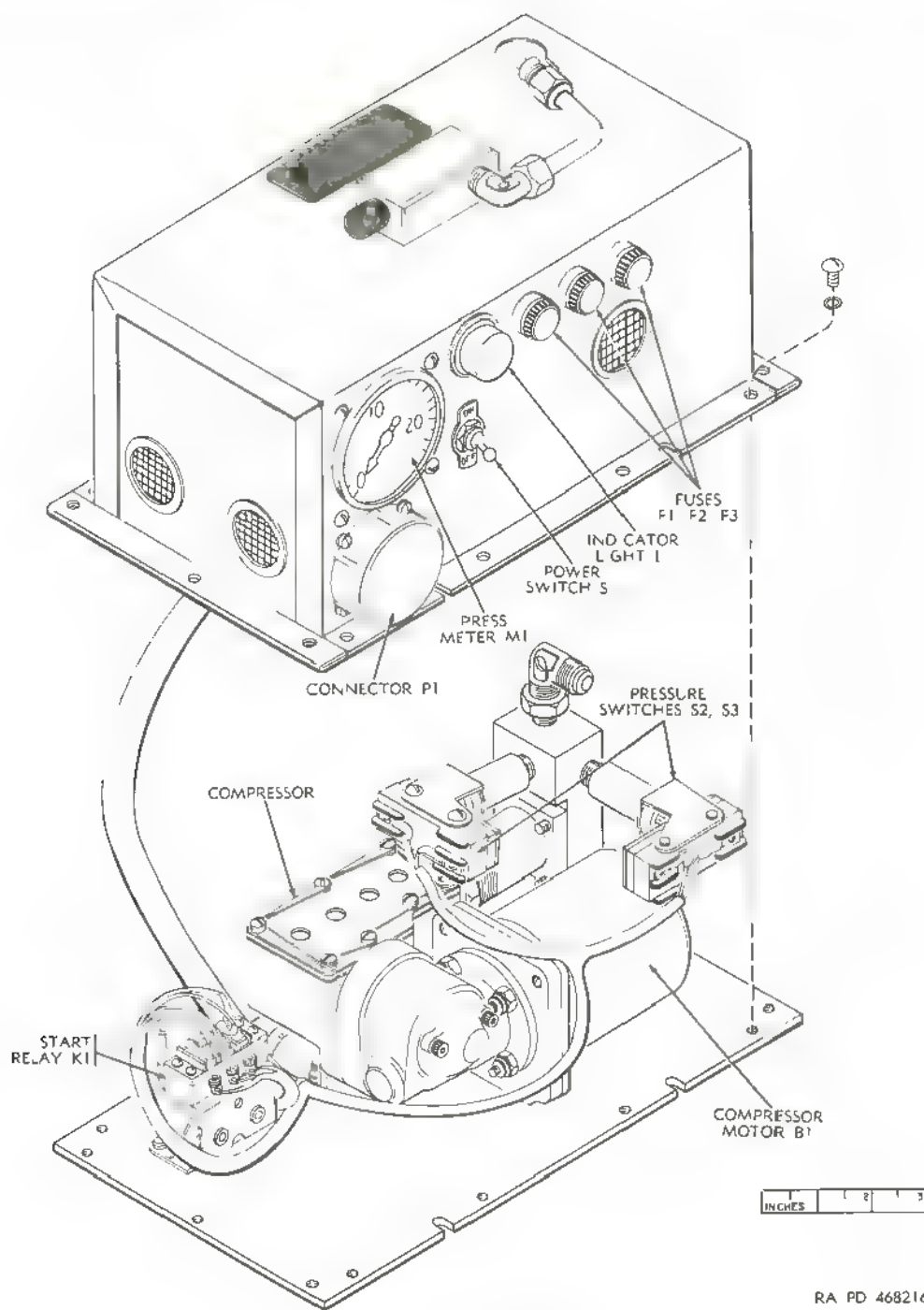
RA PD 468216

Figure 55. (U) Compressor

151

Light I1 illuminates to indicate that S1 is in the ON position.

(2) A 3-phase, 208-volt, 400-cps voltage is applied through connectors P1-A, B, and G, fuses F1, F2, and F3, and contacts of energized K1 to compressor motor B1. The motor is rated at 1/4 horsepower. It rotates at a speed of approximately 7,500 rpm with 5 to 1 speed reduction obtained in the mechanical gearing between the motor and the compressor.

(3) The compressor is a single cylinder, single action pump and has a capacity of 110 cubic inches of air per minute within the operating pressure range of 10 to 16 psi. The pump action builds up air pressure within the waveguide of the rotary coupler and when this pressure increases to 16 psi, operate pressure switch S2 is forced open. This releases start relay K1, which in turn opens the 3-phase supply circuit to motor B1, and the motor stops.

(4) Air pressure within the waveguide may be read on PRESS meter M1 located on the front of the compressor enclosure. This meter is graduated from 0 to 25 psi and is accurate within ±1 psi. When air leakage decreases the pressure to 10 psi, operate pressure switch S2 closes and energizes start relay K1, which in turn causes the compressor action to be resumed. In the event S2 fails to open, safety pressure switch S3 assumes the function of opening or reclosing the motor-pump circuit. Switch S3 opens at 23 psi and closes at 17 psi. If neither switch operates, a relief valve, located behind the air

pressure meter, opens to prevent the pressure from exceeding 30 psi.

58.1. (U) Dehumidifier – 9150659

a. General. The dehumidifier (fig. 55.1) is used on systems 1327 and up to eliminate moisture in the rotary coupler. The air from the compressor is passed through the dehumidifier before being applied to the rotary coupler.

b. Detailed Theory.

(1) The dehumidifier consists of two regenerative desiccant tanks, a heating element for each tank (HTR1 and HTR2), two solenoid-controlled air and steam valves, two capillary tubes, and a cycle timer. The cycle timer consists of a 400-cps synchronous motor, driving cams, and microswitches. The motor drives the cams which operate the microswitches. These switches control the operation of solenoids L1 and L2 which open and close the air and steam valves. The excitation of heating elements HTR1 and HTR2 is also controlled by the microswitches. The operation of the dehumidifier as described in (2) through (5) below is cycled so that one desiccant tanks is in use while the other tank is being dried.

(2) When 400 cycle ac and 28v dc power is applied to the dehumidifier, the synchronous motor on the cycle timer is energized and indicator lights I1 and I2 are illuminated. Contacts of the microswitches connected to terminals 6 and 12, 7 and 13, and 4 and 11 of the cycle timer are closed as shown in figure 55.1. Tank 1 solenoid L1 is deenergized. Tank 2 solenoid L2 is energized through

A

FLOW ARE DESIGNATED AS FOLLOWS

CYCLE OF THIS DEHUMIDIFIER IS

ACT VATED BY	T ME ACT VATED DURING 80 MINUTE CYCLE
CAM 3	90- 80 M NUTES
CAM 3	0- 90 MINUTES
CAM 2	90 135 M NUTES
CAM	0- 45 M NUTES

B 120V PH A A J2

NEUT B

AIR INLET FROM COMPRESSOR

-28V C J2

R GND D

AIR OUTLET TO ROTARY COUPLER

T SOL

ORD G27510
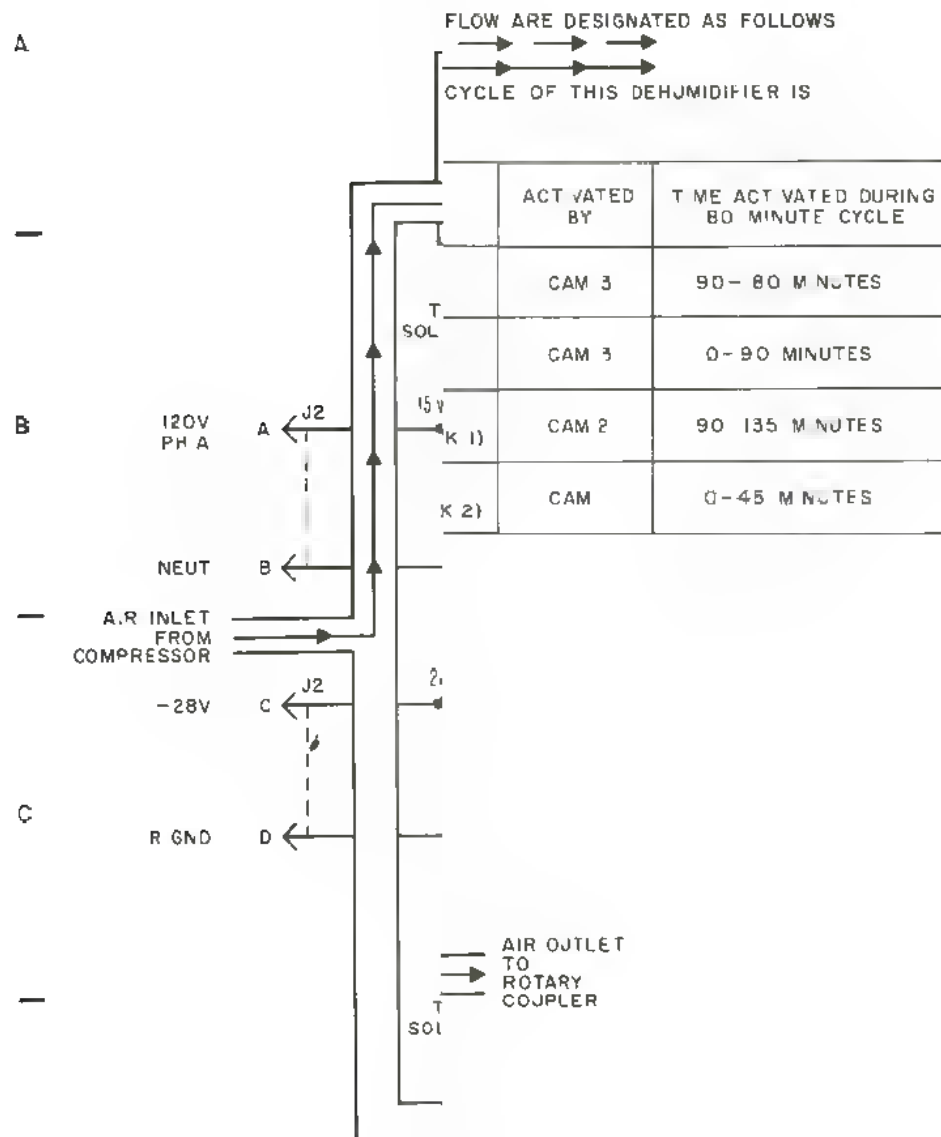
152.1

contacts of the microswitch connected to terminals 4 and 11 of the cycle timer. Heater HTR1 is deenergized. Heater HTR2 is energized through contacts of the microswitch connected to terminals 6 and 12 on the cycle timer. Deenergized tank 1 solenoid L1 opens the air valve and closes the steam valve associated with desiccant tank no. 1. Energized tank 2 solenoid L2 closes the air valve and opens the steam valve of desiccant tank no. 2. Air then flows into the air INLET from the compressor through the open air valve, desiccant tank no. 1 and the associated check valve. From the check valve the air flows through the HUMIDITY INDICATOR and then through the air outlet to the rotary coupler. The moisture in the air stream is absorbed by the desiccant tank no. 1. The desiccant in desiccant tank no. 2 is dried during the first 45 minutes of cycle. Heater HTR2 vaporized the moisture from the desiccant in the tank and discharges it as steam through the open steam valve. A small amount of air from the air flow supplies a pressure to desiccant tank no. 2 through the associated capillary tube to aid the steam discharge. At the end of the first 45 minutes of the cycle, cam 1 breaks the microswitch contacts connected to terminals 6 and 12 of the cycle timer and heater HTR2 is deenergized. For the next 45 minutes of the cycle, the desiccant in tank 2 cools down to the normal operating temperature.

(3) At the end of 90 minutes, cams 2 and 3 activate the associated microswitches. Heater HTR1 and tank 1 solenoid L1 are energized and tank 2 solenoid L2 is deenergized. This action closes the air valve and opens the steam valve associated with desiccant tank no. 1 and opens the air valve and closes the steam valve associated with desiccant tank no. 2. The air flow is now directed through desiccant tank no. 2 and heater HTR1 begins to dry desiccant tank no. 1. At the end of 135 minutes cam 2 breaks microswitch contacts connected to terminals 8 and 13 of the cycle timer and heater HTR1 is deenergized. For the next 45 minutes of the cycle, the desiccant in tank 2 cools down to the normal operating temperature.

(4) At the end of 180 minutes, cams 1 and 3 operate the associated microswitches. Heater HTR2 and tank 2 solenoid L2 are energized while tank 1 solenoid L1 is deenergized. This action closes the air valve and opens the steam valve associated with desiccant tank no. 2 and opens the air valve and closes the steam valve associated with desiccant tank no. 1. The air flow is now directed through desiccant tank no. 1 and heater HTR2 begins to dry desiccant tank no. 2 as explained in paragraph (2) above. The full cycle requiring 180 minutes is now completed. This cycling continues until power is removed from the dehumidifier.

(5) The air leaving the desiccant tanks passes through a small amount of desiccant which is visible through a window in the HUMIDITY INDICATOR. This desiccant is impregnated with

a substance which indicates moisture. This provides a check to determine if the unit is operating properly. This desiccant is normally blue and will turn pink if it absorbs moisture.

59. (U) Acquisition Orientation Level 7614258

a. General. The acquisition orientation level (fig. 56) is used when leveling and orienting the acquisition antenna.

b. Detailed Theory.

(1) The acquisition orientation level is contained in a metal case (fig. 57) having a hinged cover and a carrying handle. The bottom of the case has a machined, circular, flat surface with two dowel holes used as a reference. The center of the circular surface is a depression in the case material. The center is tapped to accommodate a lock screw.

(2) Two spirit levels (fig. 56) mounted at right angles to each other are used to establish a level horizontal position of the antenna. Two plan-table retractable peepsights are used for positioning the antenna to a known reference designation when orienting. A knurled knob is used to screw the level case to a reference surface on the antenna.

(3) The acquisition orientation level is placed on the acquisition antenna pedestal so that the dowel holes on the case fit over the dowel pins located on the rotating part of the pedestal. The three antenna mounting legs are provided with jack-type feet as a means of leveling the antenna. These jacks are set so that the spirit levels in the case are level within tolerance over the
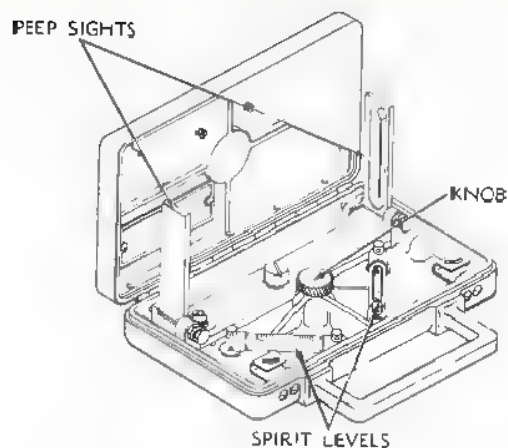
Figure 56. (U) Acquisition orientation level - inside view.

full 360° travel of the rotating portion of the acquisition antenna pedestal.

(4) Care must be taken to make certain that only the acquisition orientation level assigned to the antenna is used in sighting it, because the dowel pins on the particular antenna reference surfaces have been adjusted to the assigned serial number of the level case.
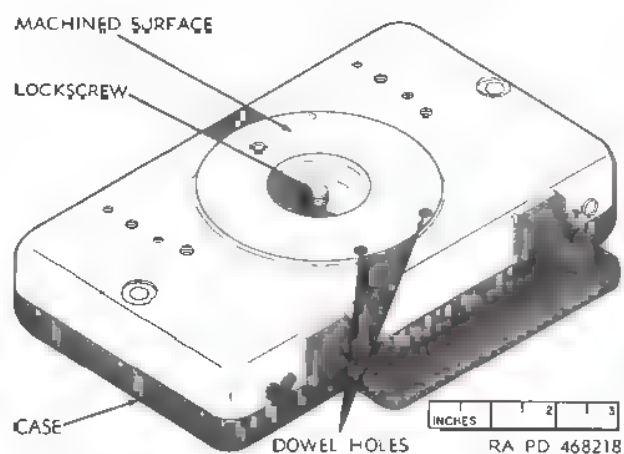
Figure 57. (U) Acquisition orientation level - bottom view.

CHAPTER 5

ACQUISITION RADAR MODULATOR

60. Acquisition Modulator 8512354

a. General. The acquisition modulator circuit develops a positive 800-volt, 2-microsecond pulse into a 4- to 8-kilovolt (kv), 1.3-microsecond pulse which is used to trigger the acquisition magnetron. The acquisition modulator contains two subchassis; the acquisition trigger amplifier (par. 61) and modulator control-indicator (par. 62).

b. Detailed Theory.

(1) *Thyratron switch V1.*

(a) With no input signal, hydrogen thyratron switch V1 (fig. 52, TM 9-1430-257-20) is cut off even through operating with 0-volt grid bias and 8 to 16 kv on its plate. No plate current flows because a hydrogen thyratron tube re quires a positive control grid for tube ionization. In the plate circuit, the capacitors in pulse-forming network Z1 charge 8 to 16 kv by means of resonant charging or charges almost twice the 4 to 8 kv at TRAILER HIGH VOLTAGE connector J1. (Resonant charging is described in par. 61.) The voltage at J1 can be varied from 4 to 8 kv by MAGNETRON HV supply knob T1 located on the acquisition control indicator. It is normally set for 6 to 7 kv, which produces the desired 30 milliamperes of magnetron current. Magnetron pulse transformer T1, located in the acquisition receiver-transmitter, is the load of Z1. The complete charge path of Z1 is from ground through externally located T1, through PULSE connector J5 to Z1, then through inductor L3 and J1 to the acquisition high-voltage power supply.

(b) The positive 800-volt, 2-microsecond trigger pulse is applied to grid resistor R1 of V1 through connector J4. The trigger pulse ionizes V1, allowing Z1 to discharge through magnetron pulse transformer T1 and the low resistance of V1. Pulse-forming network Z1 is completely discharged in 1.3 microseconds, producing a negative 4- to 8-kv, 1.3-microsecond pulse across T1. Simultaneously, with the trailing edge of the pulse, V1 deionizes and Z1 again charges (from ground through L3) to +8 to +16 kv. The charge-discharge cycle of Z1 is repeated at the 500 pps rate of the trigger pulse from the acquisition trigger amplifier.

1. The output circuit of V1 is matched to the impedance of the magnetron as closely as possible to obtain a maximum power transfer. In accomplishing maximum power transfer, the amplitude of the output pulse drops to one-half the 8 to 16 kv to which Z1 is charged.

2. At the instant of ionization, V1 draws grid current. The sudden change of voltage between the grid and ground of V1 initiates a voltage transient which is reflected toward the acquisition trigger amplifier. However, inductor L1 is in series with the voltage transient reflected to J4 and the high reactance of L1 to the initial surge of grid current limits the amplitude of the reflected voltage.

3. In the plate circuit of V1, the first surge of current initiates a half-cycle of oscillation in the LCR combination of inductor L2, resistor R2, and capacitor C1. This half-cycle of oscillation shapes the leading edge of

frequency of the transmitter sync pulse. Since polarity reversal occurs in T3 and since T3 has a step-up ratio of 1 to 1.4, the output pulse at connector J2 is a positive-going, 800-volt, 2-microsecond pulse. The pulse at winding 2-1 of T3 can be monitored at trigger pulse monitor test point connector TP2.

(4) *Reverse current diode V3.* At the termination of the output pulse and before Z1 is recharged, voltage reflections are received from the acquisition modulator. These reflections enter at connector J2 and are coupled from winding 2-1 of T3 to winding 3-4. The voltage reflections are of the same polarity as the outgoing trigger pulse. However, winding 2-1 of T3 is now the source, and Z1 is the load. The negative pulse induced in winding 3-4 of T3 is coupled through Z1 to the plate of V2, driving it negative with respect to ground. This also places the cathode of reverse current diode V3 below ground. Therefore, V3 conducts and shorts the reflected voltage to ground. This action insures a constant reference level for successive pulses and removes any damped oscillations in the trailing edge of the pulse which could cause random triggering of the magnetron.

62. Modulator Control-Indicator 8173006

a. General. The modulator control-indicator contains metering, power supply, and overload control circuits of the acquisition modulator.

b. Detailed Theory.

(1) *Overload circuit.*

(a) The input to the overload circuit is a dc current applied at connector P1-1 (fig. 54, TM 9-1430-257-20). This current is caused by voltage reflections from the magnetron to the acquisition modulator circuit and is referred to as inverse current. It flows through a circuit composed of resistors R3, R1, R2, overload relay K1, and capacitor C1. From this circuit, it then flows through common resistor R4 to ground.

Normally, the total current ranges from 30 to 55 milliamperes, which is not sufficient to energize K1. If the voltage reflections from the magnetron to the modulator circuit are excessive, the current increases sufficiently to energize K1. Contacts 5 and 6 of K1 open, breaking the high-voltage interlock circuit. This removes all high voltage from the acquisition transmitter system.

(b) Capacitor C1 is connected across R2 and K1 and bypasses any sudden current surges around K1. This insures that K1 energizes only when the current increase is continuous. Capacitor C1 also acts as a filter for continuous overload current and thus maintains a constant voltage drop across K1. Resistors R1 and R2 are in series with K1 and limit the current through the relay coil. The voltage developed across resistor R4 is applied to meter M1 as an indication of inverse current.

(2) *Thyratron-reservoir power supply.* The input to the thyratron-reservoir power supply is 120 volts ac. This voltage is applied through P1-14 and 15 to variable transformer T1. A variable tap, adjusted by means of the INCREASE knob, controls the output voltage from T1. The voltage range of T1 is 0 to 6 volts at 0 to 6 amperes; T1 is adjusted to the value stamped on thyratron switch V1 in the acquisition modulator circuit. The purpose of a variable ac voltage in T1 is to maintain optimum gas pressure within V1 in the acquisition modulator (par. 60b(1)(c)). This voltage is applied from terminal 3 of T1 directly to primary winding 1-2 of transformer T2. Parallel secondary windings are employed in T2 for current handling. The output from these windings is applied to P1-2 and 5.

(3) *Metering circuit.* Meter M1 is used for monitoring the inverse current and thyratron-reservoir voltage. The input to

meter M1 is controlled by switch S1, which has three positions: OFF, INVERSE CURRENT (FS 100 MA), and THY.-RES VOLTAGE FS 10 V. A reading of from 30- to 55-milliampere inverse current indicates normal operation of the acquisition modulator. With S1 in the THY.-RES VOLTAGE FS 10 V position, M1 indicates the voltage stamped on V1 in the acquisition modulator.

63. Miscellaneous Cabinet-Mounted Components in Acquisition Modulator

a. General. This paragraph describes the theory of operation of cabinet-mounted components in the acquisition modulator.

b. Detailed Theory.

(1) *Impedance networks.* Impedance networks Z2, Z3, Z4, and Z5 are low-pass filters connected in series with the − 250-volt, 120-volt neutral, 120-volt phase C, and + 320-volt power supplies, respectively (fig. 52, TM 9–1430–257 20). These filters pass the low-frequency power supply voltages, but isolate the power supplies from high-frequency voltage transients present in the acquisition modulator.

(2) *Interlock switch S1.* Interlock switch S1 is mounted on the acquisition modulator housing, flush with the outer cover. Switch S1 is normally closed, completing the ground path to relays controlling the low-voltage power supply. When the cover is removed, switch S1 opens this path. Low-voltage power is removed, and INTLK indicator light I30 on the acquisition power control panel is extinguished. At the same time, high voltage is also removed because the low- and high-voltage control circuits are interlocked.

(3) *Transformer T1.* Transformer T1 supplies 6.3 volts ac to the filaments of V1 in the acquisition modulator.

(4) *Blower motor B1.* Blower motor B1 is a 208-volt, three-phase motor provided to cool the acquisition modulator circuits.
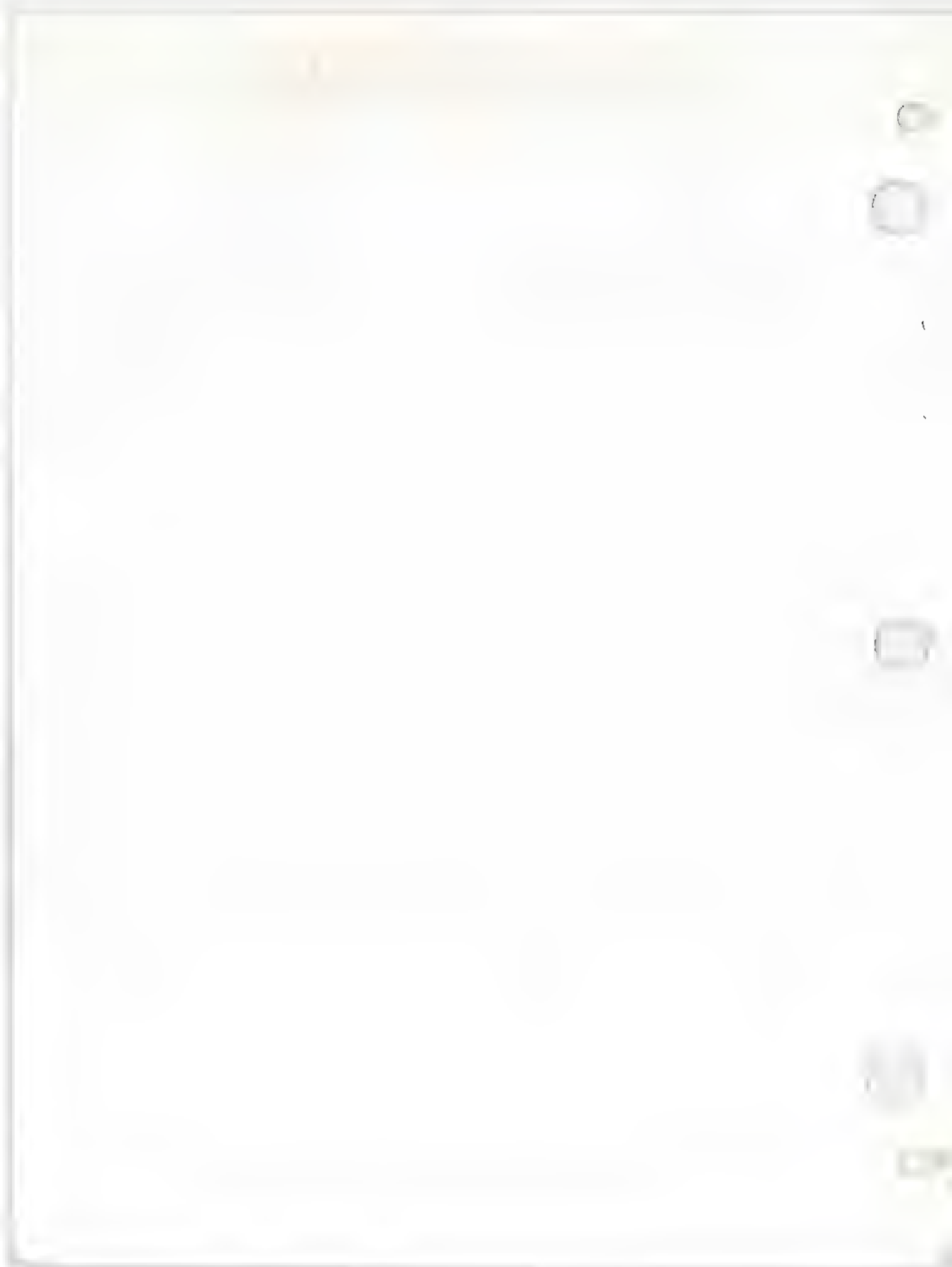
CHAPTER 6 (CMHA)

ACQUISITION RECEIVER-TRANSMITTER 8515397 OR 9156628

64 (U). General

a. Acquisition Receiver-Transmitter 8515397. The acquisition receiver-transmitter 8515397 consists of the magnetron and its associated circuits, frequency and power meter 8173652, acquisition duplexer 8512993, noise generator 8520785, magnetic circuit 8516184, acquisition preselector 7621790, receiver frequency-converter 7621829, acquisition local oscillator 7599343, acquisition IF preamplifier 7620695, AFC frequency-converter 7621830, acquisition AFC 9143030, low-power servo amplifier 7614253, AFC motor generator 7605334, acquisition RF power supply control 8158120 or 9000009, and miscellaneous cabinet-mounted components of the acquisition receiver-transmitter. Detailed theory of the units listed above is found in paragraphs 64.1 and in 65 through 78. For functional theory, refer to TM 9-1430-250-20/1.

b. Acquisition Receiver-Transmitter 9156628. The acquisition receiver-transmitter 9156628 is recoded from acquisition receiver-transmitter 8515397 when DA MWO 9-1400-268-50 is installed to add antijam display (AJD) capabilities to the Nike-Hercules system. New units which are added or recoded by this change are the acquisition RF power supply control 9156017, receiver-transmitter subassembly 9156632, auxiliary frequency converter 9990516, main frequency converter 9989320, acquisition AFC 9156541, auxiliary IF amplifier 9156573, IF amplifier 9156675, two acquisition preselector cavities 9990523 and 9990524, and miscellaneous cabinet-mounted components. Detailed theory of the units listed above is found in paragraphs 78.1 through 78.8. For functional theory, refer to TM 9-1430-250-20/1.

64.1 (CMHA). Magnetron and Associated Circuits

a. General. The acquisition magnetron generates 1.3-microsecond pulses of RF energy which are fed through a waveguide to the acquisition antenna for radiation. The magnetron operates over a frequency range of 3,100 to 3,500 megacycles.

b. Detailed Theory. The acquisition magnetron and associated circuits consist of magnetron cathode fan B1 (fig. 55, TM 9-1430-257-20); magnetron anode fan B4; filament transformer T2; magnetron cathode circuit, composed of pulse transformer T1 and associated circuit components; magnetron; arc suppressor circuit; magnetron current metering circuit, composed of voltage regulator V8, impedance network Z1, and associated circuit components; and the magnetron tuning drive.

(1) *Magnetron cathode fan B1 and magnetron anode fan B4.* Magnetron cathode fan motor B1 and anode fan motor B4 are conventional three-phase induction motors which supply an air stream to cool the magnetron. They are placed in operation when MAIN POWER switch S4, ACQUISITION POWER switch S6, and AQC MOTORS switch S5 on the acquisition power control panel of the director station group are activated. AIR FLOW switch S1 is mounted on B1 and is closed when B1 is supplying a sufficient amount of cooling air. An identical type switch is mounted on B4. If S1 on B1 is open, power is removed from filament transformer T2. If S1 on B4 is open, high voltage cannot be applied to the magnetron be-

161

cause the 15-minute delay timer located in the director station group will not be energized.

(2) *Filament transformer T2.*

(a) The 120-volt supply to T2 enters at connector J2-2 and is applied to terminal 1 of the primary of T2 through the normally closed contacts of hot box interlock switch S2, S1 of B1, and inductor L1 (fig. 58). Terminal 2 of T2 is returned directly to the 400-cycle neutral line. Switch S2 is located in the magnetron hot box and is closed by the hot box cover. The high series impedance of L1 isolates the 400-cps power supply from the high-frequency transient voltages initiated in the secondary of T2.

(b) From the junction of S1 and L1, the 120 volts is also applied through the normally closed contacts of AIR FLOW switch S1 of B4 as energizing voltage for start relay K1 in the 15-minute delay timer on the acquisition 5-minute delay timer. Relay K1 controls the application of high voltage to the acquisition modulator. Since the 120 volts is applied to K1 only when S1 of B4 is closed, the application of the high voltage is interlocked with the normal operation of S1 of B4.

(3) *Magnetron-cathode circuit.*

(a) The 120 volts from the primary of T2 is coupled to the secondary of T2, which is connected through bifilar secondary windings 3-4 and 5-6 of pulse transformer T1 to the directly heated cathode of the magnetron. The use of bifilar windings places terminals 3 and 5 of T1 at the same pulse potential. Since the

secondary of T2 is connected between these points, no difference of pulse potential exists across T2. Consequently, high-voltage insulation is not required for T2 to prevent arcing, as would be the case if a single secondary winding were used in T1. The primary purpose of T1 is to step-up the high-voltage pulse for application to the magnetron. Capacitor C6, connected across the secondary of T1, and capacitors C8 and C9, connected across the secondary of T1 and T2, keep each end of T1 at the same potential to prevent burning out the filaments of the magnetron. Winding 7-8 of T1 is a single turn loop which is shunted by the low resistance of parallel resistors R39 and R40. This network acts as a low resistance across the tuned circuit composed of the secondary of T1 and the distributed capacitance of the magnetron cathode circuit, and suppresses oscillations within T1 at the trailing edge of the modulator pulse. Oscillation of T1 could cause additional firing of the magnetron and would show up as objectionable range rings at the beginning of the PPI sweep.

(b) The normal current path for the magnetron is from the cathode to anode ground, resistor R36, and then through capacitors C2 and C7 where it divides between the bifilar windings of T1 back to the cathode of the magnetron. The capacitance of C2 and C7 presents zero reactance to the pulse current. A greatly attenuated pulse is developed across R36 and fed through connector J7 to the acquisition AFC.

(c) When there is an open circuit in the magnetron cathode circuit, the successive modulator high-voltage pulses quickly build up a large voltage across the bifilar secondary of T1. Spark gap capacitor C3 is connected across the secondary of T1 and shorts this voltage to ground, thus protecting the secondary winding of T1 from high-voltage arc-over.

(4) *Magnetron.*

(a) The magnetron is essentially a diode, with the cylindrical plate mounted concentric with the cathode. The plate, or anode, is split into a number of segments. These segments have apertures which are points of excitation for resonant cavities contained within the anode structure. A permanent magnet, which is part of the magnetron, produces a strong magnetic field perpendicular to the path of electrons from cathode to plate.

(b) Normally, there is no electron flow between cathode and anode because both electrodes are at ground potential. When the 40-kilovolt, 1.3-microsecond pulse is applied to the cathode of the magnetron, a strong electric field is set up between cathode and anode. Electrons are emit-

ted at a high velocity in this field toward the anode, but are bent in a spiral path by the magnetic field of the permanent magnet. As the electrons pass the cavity apertures, the cavities are excited and oscillate at the resonant frequency of the cavities. A probe is mounted in the cavities at a point for maximum transfer of energy, and couples the RF energy to the acquisition duplexer. The maximum peak power produced by the magnetron is 1 megawatt.

(5) *Arc suppressor circuit.*

(a) The arc suppressor circuit consists of arc suppressor relay K5, capacitors C1 and C14, and an insulated arc suppressor wire which is connected in the acquisition duplexer across the flared output coupling of the magnetron. The arc suppressor wire is open circuited. Each end of the open circuited wire is connected across C1.

(b) When transmitter operation is normal, C1 (which is smaller than C14) charges quickly. Since current ceases to flow when C1 is charged, only a small charge is accumulated in C14. The voltage drop across C14 is not sufficient to energize K5, and transmitter sync pulses

162.01

Figure 58. (U) Acquisition magnetron circuits – simplified schematic diagram.

ORD G177776

ACQUISITION RF POWER SUPPLY CONTROL

VOLTAGE REGULATOR V8 OC3

R34 26.1
R38 000

TO MAG CURRENT METERING CKTS

Z1

R36 0.5
C2 0.01
J7

C9 0.25
C8 0.0
FILAMENT TRANSFORMER T2
45 MH L
NEUT

MAG ANODE BLOWER B4
AIR FLOW S1
MAG CATHODE BLOWER B3
AIR FLOW S2
HOT BOX INTLK S2

START K1
NEU

ACQUISITION 5-MINUTE OR 15-MINUTE DELAY TIMER
(NOTE 2)

120V AC J2-2 PHASE A

NOTES:
1. ALL VALUES ARE IN OHMS OR MICROFARADS UNLESS OTHERWISE INDICATED
2. 15-MINUTE DELAY TIMER IS USED IN SYSTEMS 1001—1286. ACQUISITION 5-MINUTE DELAY TIMER IS USED IN SYSTEMS 1287—

R39 2
R40 2
PULSE TRANSFORMER T1

C3 75 UUF
C6 0.05

TUNABLE MAGNETRON V1 5795

ARC SUPPRESSOR K5 3,800
C14 1
C1 6600 UUF
+50V

ACQUISITION DUPLEXER
RF ENERGY TO ANTENNA

SYNC IN J29
TO ACQ TRIG AMP J30

B2
R1 000
FREQ MEASURE
R3 0.22 MEG
−250V

MAGNETRON TUNING DRIVE
J25 P11
NEUT

C4
C3A
C3
CONTROL VOLTAGES

MAG FREQ S2
120V AC PHASE A
RAISE
LOWER
MAG FREQ S3

ACQUISITION RF POWER SUPPLY CONTROL
CONTROL VOLTAGES

NEUT

FREQUENCY AND POWER METER

ACQUISITION CONTROL-INDICATOR
MAG FREQ & REC NOISE S9

TO NOISE GEN SW TCH S9 AND
MAG FREQ & REC NO SE METER M2

are allowed to pass through normally closed contacts 5 and 6 of K5 to the acquisition trigger amplifier.

(c) When there is excessive arcing in the acquisition duplexer, the open circuit of the arc suppressor wire becomes shorted and represents a closed switch. This removes C1 from the circuit, and C14 is allowed to charge. At some point, the voltage across C14 is sufficient to energize K5. Thus contacts 5 and 6 open, removing transmitter sync pulses from the acquisition trigger amplifier and deactivating the transmitter system. With no trigger pulse, the magnetron is not fired, and arcing ceases in the acquisition duplexer. The arc suppressor wire again represents an open circuit, allowing C14 to discharge through the resistance of K5. At some point, the voltage across C14 drops to the point where K5 deenergizes. Trigger pulses again pass through contacts 5 and 6 of K5 to the acquisition trigger amplifier, reactivating the transmitter system. If the arcing is of a transient nature, normal transmitter system operation is resumed. However, if the arcing continues, the energizing-deenergizing cycle of K5 is repeated until dc power is manually removed from the transmitter system.

(6) *Magnetron current metering circuit.* The magnetron current metering circuit is connected in parallel with C2, C7, and R35. It consists of impedance network Z1, voltage regulator V8, and resistor R34. Resistor R34 is located in the acquisition RF power supply control. Resistor R34 is in parallel with the magnetron current metering circuits in the acquisition RF power supply control and the acquisition control-indicator. Impedance network Z1 acts as a filter and provides an average voltage indicative of the magnetron current to R34. Magnetron current should be set to 30 milliamperes by MAGNETRON HV supply knob T1,

located on the acquisition control-indicator. If the normal ground path of C2, C7, and R36 opens, no current flows through the magnetron. Consequently, the negative 40-kilovolt trigger pulse potential at terminals 4 and 6 of T1 would be present instantaneously at all points of the magnetron cathode circuit. Since this potential would be present at the plate of V8, the inverse voltage would be sufficient to ionize V8. The instantaneous ionizing of V8 insures a low shunt resistance across the metering circuits. This provides adequate protection to the metering circuits, regardless of any additional current paths in these circuits.

(7) *Magnetron tuning drive.*

(a) The magnetron tuning drive permits the magnetron frequency to be varied from 3,100 to 3,500 megacycles. It consists of split-phase magnetron tuning drive motor B2, and an associated gear and shaft mechanism which is connected to tuning slugs within the resonant cavities of the magnetron. When the tuning slugs are inserted into the cavity, the size of the cavity is reduced and the frequency is increased. Conversely, when the tuning slugs are retracted from the cavities, the size of the cavities is increased and the frequency is decreased.

(b) Motor B2 can be controlled by either MAG FREQ switch S2 on the acquisition RF power supply control, MAG FREQ switch S3 on the frequency and power meter, or MAG FREQ & REC NOISE switch S9 on the acquisition control-indicator. These switches have two manual positions, and are spring-loaded to center position. The RAISE and LOWER positions are interconnected so that no two switches can control B2 at the same time. The operation of all three switches is similar to S2. If S2 is held in the RAISE position, one winding of B2 is returned through connector P11–3 and contacts

CONFIDENTIAL

4 and 5 of S2 to 120 volts, phase A. The second winding is returned through connector P11–3 and the parallel path of phase-shift capacitors C3A and C4, contacts 2 and 1 of S2, to 120 volts, phase A. The third winding is permanently connected to the 120-volt neutral line at connector P11–5. The phase shift across C3A and C4 places the 120 volts across the first and second windings in quadrature with the 120 volts across the first and third windings. The quadrature voltages produce a rotating magnetic field, which causes B2 to rotate in a direction so as to increase magnetron frequency.

(c) If S2 is held in the LOWER position, the first winding is returned through P11–3 and contacts 8 and 9 of S2 to 120 volts, phase A. The second winding is returned through P11–1, C3A and C4, and contacts 2, 3, 11, and 12 of S2 to the 120-volt neutral line. The phase-shift through C3A and C4 places the 120 volts across the first and second windings in quadrature with the 120 volts across the first and third windings. A rotating magnetic field is set up which causes B2 to rotate in a direction so as to lower the frequency.

(d) Frequency measure variable resistor R1 is part of a voltage divider composed of resistors R3 and R1 connected between −250 volts and ground. The brush arm of R1 is geared to the tuning drive mechanism of B2. Since the position of the brush arm of R1 is determined by the position of the tuning drive mechanism, the voltage at the brush arm is indicative of the magnetron frequency. This voltage is fed through connector P11–10 and NOISE GEN switch S19 to MAG FREQ & REC NOISE meter M2. Both S19 and M2 are located on the acquisition control-indicator.

65. Frequency and Power Meter 8173652

a. *General.* The frequency and power meter is a unit of built-in test equipment which is used to measure the frequency and power output of the acquisition transmitter.

b. *Detailed Theory.*

(1) *General.* Transmitter frequency and power output are monitored on meter M1 (fig. 59, TM 9–1430–257–20). The use of M1 is determined by TEST switch S2. This switch has two positions, BAL and MEAS. Although S2 is a 6-pole double-throw switch, it can be considered as a 3-pole double-throw switch since the lower three poles are in parallel with the upper three poles. It is so represented in figures 59 and 60, which are simplified schematics of those frequency and power meter circuit components used in conjunction with S2 and M1 for meter balancing and measurements.

(2) *TEST switch S2—BAL position.*

(a) With TEST switch S2 in the BAL position, meter M1 is connected across a conventional bridge circuit and the bridge potentials adjusted for a zero reading on M1. The circuit arrangement is shown in figure 59. Note that +150 volts is applied across a series voltage divider consisting of resistors R12, R11, and R8. Approximately 1/20 or +7 volts is dropped across R8. The +7 volts is also applied across the parallel circuit of BALANCE—FINE variable resistor R7, BALANCE—COARSE variable resistor R6, sensitivity variable resistor R4 shunted by resistor R5, and the bridge circuit.

(b) The bridge circuit arrangement is as follows: from point 1 through resistor R9 to point 2, and then through S2 contacts 2–3 and 11–12 and thermistor RT1 to point 3; also from point 1 through resistor R2 to point 4, and through resistor R3 to point 3. Meter M1 is connected across the bridge from points 2 to 4 as follows: from point 2

through resistor R1 shunted by GALV SENS switch S1, contacts 6–5 and 15–14 of S2, M1, contacts 8–9 and 17–18 of S2 to point 4.

(c) Meter M1 is balanced when the resistance of R2 and R3 are equal to that of R9 and RT1. At this time, no current flows through M1, since the voltage potentials at points 2 and 4 are equal. Balancing is accomplished by varying R6 and/or R7 to adjust the voltage potential applied between points 1 and 3 so that the current through RT1 pro-

duces a resistance of 100 ohms. Thermistor RT1 has a negative temperature coefficient; therefore its resistance is inversely proportional to the current through it. Switch S1 is provided so that R1 can be bypassed in order to obtain a more accurate zero adjustment. At all other times, R1 serves as a current-limiting resistor in series with M1.

(3) *TEST switch S2—MEAS position.*

(a) *Calibration.* With S2 in the MEAS position (fig. 60), resistors R12, R11,
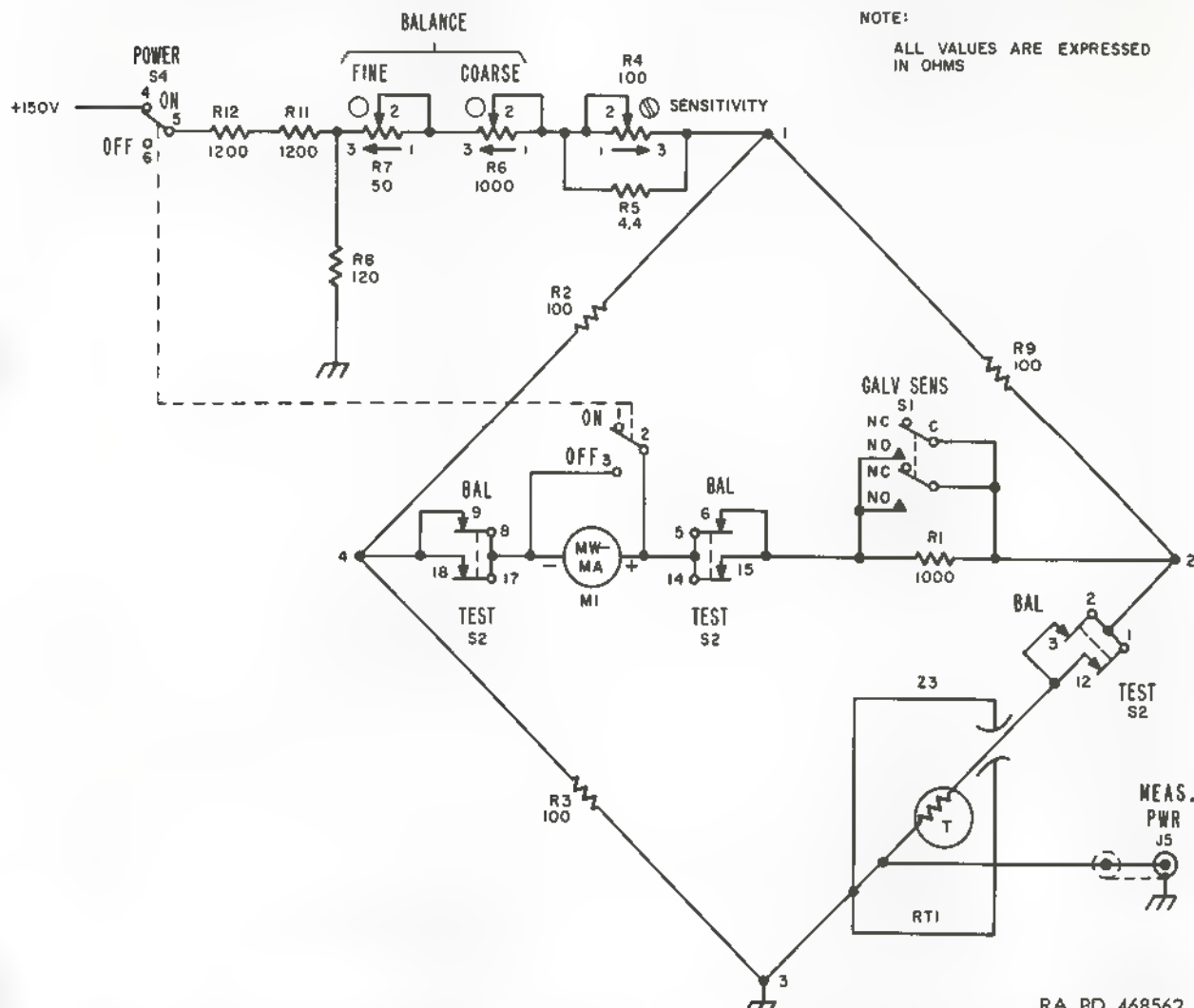
Figure 59 (U) Frequency and power meter—test switch S2 in BAL position—simplified schematic diagram.

RA PD 468562

CONFIDENTIAL

and R8 are again connected in a voltage divider across +150 volts, producing +7 volts across R8. However, the +7 volts is now applied across a series-parallel circuit consisting of R7 and R6; a shunt divider consisting of R4, R5, and M1; and a series parallel divider consisting of R2 and R3 shunted by R9 and R10. Resistors R9 and R10 are connected by contacts 1-2 and 10-11 of S2. Meter M1 is connected across R4 and R5 by contacts 4-5 and 13-14 at point 1 and contacts 7-8 and 16-17 at point 2. Sensitivity variable resistor R4 is used during calibration of M1 and is adjusted for a maximum reading of 22.5 milliamperes. A standard level signal is used during this calibration, and R4 is locked after the desired reading is obtained. Since M1 is connected across a voltage potential, there is a normal current through it with no signal applied. This current causes a deflection on M1 whenever S2 is placed in the MEAS position.

(b) *Power measurements.*

1. Prior to measuring transmitter power, S2 is placed in the BAL position (fig. 59) and resistors R7 and/or R6 are adjusted for a zero reading on M1. Switch S2 is then placed in the MEAS position (fig. 60), and the quiescent current reading on M1 is recorded.

2. With S2 in the BAL position, the transmitter output is applied at MEAS. PWR. connector J5 to RT1 (fig. 59, TM 9-1430-257-20). With the RF power affecting the resistance of RT1, M1 is zeroed by using R7 and/or R6. Switch S2 is then placed in the MEAS position and the new quiescent current reading on M1 is compared with the value recorded in *1* above. The difference in reading is indicative of the transmitter power.

(c) *Frequency measurements.* The transmitter output enters at FREQ METER IN connector J2 and is applied to tunable cavity Z1, which acts as a series-tuned circuit. The output energy from Z1 is probe-coupled to FREQ METER-OUT connector J6 and then passed through a connecting coaxial cable to J5. From J5, the energy is applied to RT1. The temperature rise caused by the RF energy decreases the resistance of RT1. With S2 in the BAL position, the bridge unbalance produced by the change in resistance of RT1 is indicated by a meter deflection. As the cavity is tuned throughout its frequency range using the MEAS FREQ knob, the indication of M1 rises sharply when the cavity is tuned to the transmitter frequency. The rise occurs because the cavity is at
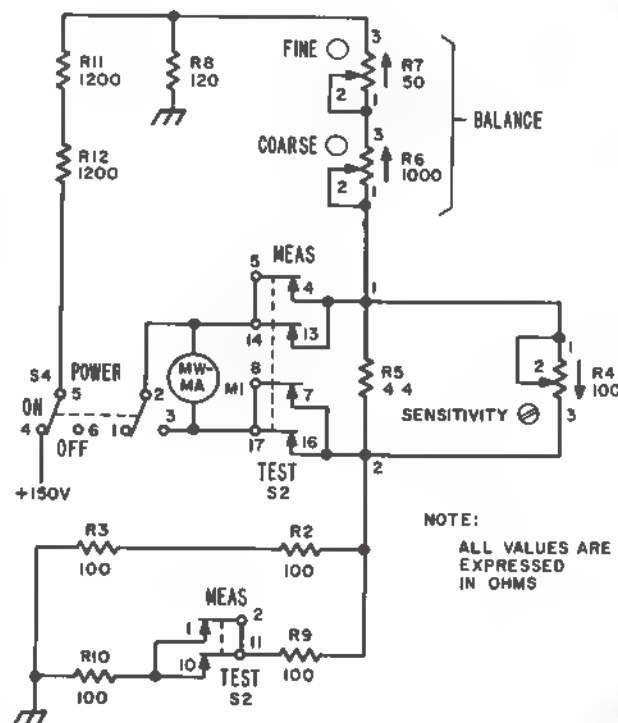
RA PD 468563

Figure 60 (U) Frequency and power meter—test switch S2 in MEAS position—simplified schematic diagram.

CONFIDENTIAL

series resonance, and its impedance is minimum. At this point, maximum energy is coupled to RT1, producing a maximum unbalance in the bridge circuit. Peaking is accomplished by activating S1, and readjusting Z1 for a maximum meter indication.

(4) *Demodulator circuit Z2.* Demodulator circuit Z2 provides a means for analyzing the transmitter pulse which enters at CRYSTAL IN connector J3 and is applied directly to Z2. Demodulator circuit Z2 contains crystal detector CR1 which detects the RF pulse and passes the video envelope to VIDEO connector J4. A capacitor is connected across CR1 to bypass any RF energy from the output line.

(5) *MAG FREQ switch S3.* MAG FREQ switch S3 is a double-throw (RAISE LOWER) 4-pole switch. Its contacts are normally in the position shown in figure 59, TM 9–1430–257–20. MAG FREQ switch S3, MAG FREQ & REC NOISE switch S9 located on the acquisition control-indicator, or MAG FREQ switch S2 located on the acquisition RF power supply control can be operated to vary the magnetron frequency. When any of these switches is operated, control voltages are applied to magnetron tuning drive motor B2 located in the acquisition receiver-transmitter.

66. Acquisition Duplexer 8512993

a. General. The acquisition duplexer is an electronic waveguide switch which enables a single antenna to be used for transmission and reception. When the magnetron fires, the acquisition duplexer matches the transmitter to the antenna and protects the receiver system from the injurious effects of the high-voltage RF pulse. Between transmitter pulses, the acquisition duplexer channels the low-level RF return pulses to the receiver system and prevents dissipation of this energy in the transmitter system. It also contains a pickup probe for transfer of attenuated transmitter RF energy to the AFC system and a

directional coupler which is used in measuring transmitter power and frequency.

b. Detailed Theory.

(1) The acquisition duplexer (fig. 61) consists of a Y-shaped section of waveguide to which are mounted a transmit-receive (TR) tube, two antitransmit-receive (ATR) tubes, a directional coupler, and an AFC coupling probe. Energy is coupled to the TR and ATR tubes through rectangular waveguide windows and to the directional coupler through three circular irises.

(2) The TR tube forms an H-plane parallel junction with the main waveguide. It contains three spark gap electrodes, each separated by a quarter wavelength. Spark gap SG 1 (A, fig. 62) is one wavelength from the center of the waveguide. A keep-alive potential of 800 volts is applied through a keep-alive probe to the center of the TR tube to insure quick ionization of the gas within the tube.

(3) The ATR tubes (fig. 61) form an E-junction series with the main waveguide. They are electrically one-quarter wavelength in depth, thus normally reflecting a high series impedance to the window E-junction with the main waveguide. The window of ATR 1 (A, fig. 62) is one quarter wavelength from the Y-junction at the lower portion of the magnetron frequency band, and the window of ATR 2 is one-quarter wavelength from the Y-junction at the upper portion of the frequency band. Their combined effect over the magnetron operating frequency range is equivalent to one ATR tube at one-quarter wavelength from the Y-junction.

(4) When the magnetron fires, the 1-megawatt pulse of RF energy travels down the duplexer toward the Y-junction (B, fig. 62). A high voltage is impressed across the high impedance of the ATR tube windows, and this potential ionizes the gas at the tube windows. Instantaneous ionization of the entire ATR tubes

CONFIDENTIAL
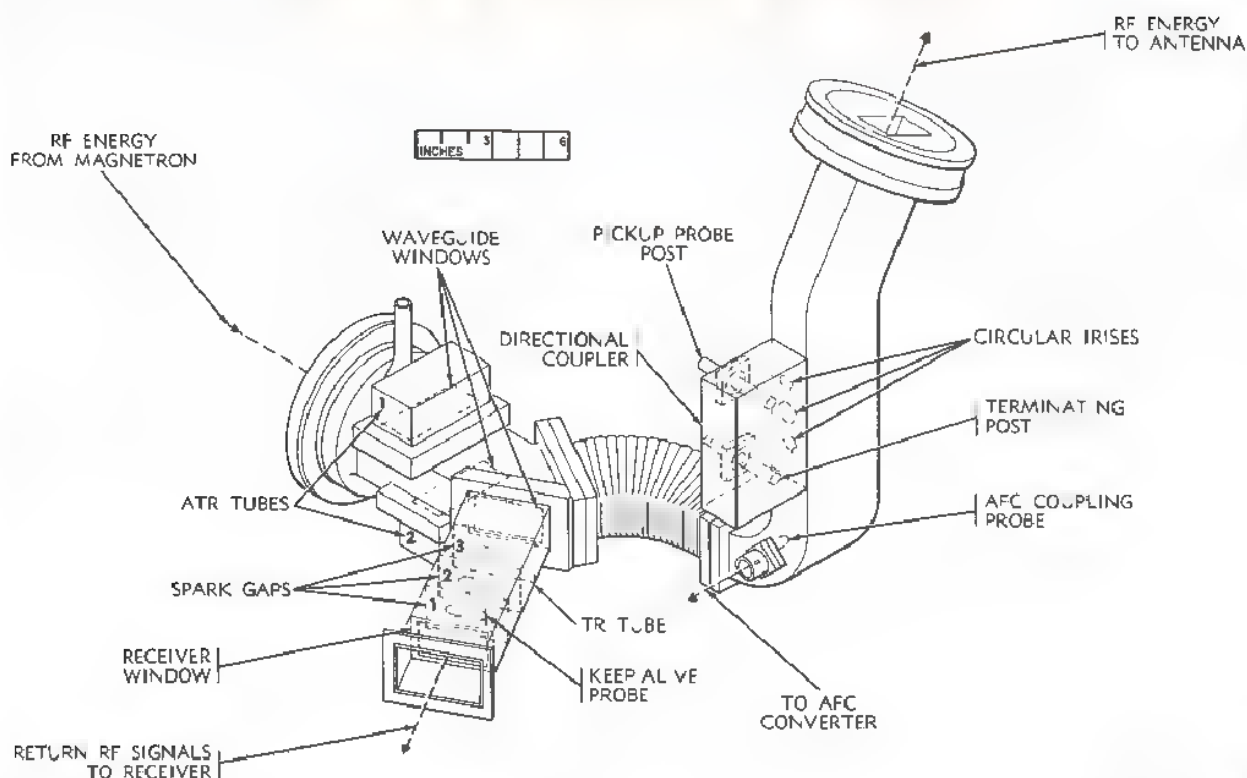
Figure 61. (U) Acquisition duplexer.

RA PD 468564

follows, causing the impedance at the ATR tube windows to drop sharply. As a result, the waveguide section from the magnetron to the Y-junction appears to the RF energy as a continuous section of waveguide. When the RF wave reaches the Y-junction, it sees a parallel path through the TR tube windows to the receiver and to the antenna. Since the three spark gaps within the TR tube are spaced one-quarter wavelength apart and SG 1 is a full wavelength from the center of the waveguide, one of the spark gaps will be at a high impedance point. Thus, a large RF voltage potential appearing across this spark gap ionizes the gas between the spark gap electrodes. The adjacent spark gaps also break down

since they are at a high impedance point one-quarter wavelength from the shorted spark gap. Three spark gaps are used to insure instantaneous ionization of the TR tube, thus preventing a large voltage spike from passing into the receiver frequency-converter and burning out the crystal mixer. Ionization of the entire TR tube follows, presenting a shorted wall at the TR tube window facing the Y-junction. This causes the waveguide to appear continuous to the RF energy as the energy travels toward the antenna.

(5) The low-level return RF signals are channeled down the antenna waveguide to the Y-junction (C, fig. 62). At the Y-junction, the RF signals see a parallel path to the transmitter and to the re-

168

PART OF
DUPLEXER

ELECTRICAL CENTER
OF WAVEGUIDE

NOTE 1

Y JUNCTION

FROM MAGNETRON

ATR 1

TR TUBE
WINDOW

A

TO ANTENNA

ATR 2

NOTE 2

SG 3
(NOTE 3)

TR TUBE

SG 2

1 WAVELENGTH

SG 1

RECEIVER WINDOW

A ELECTRICAL CHARACTERISTICS

PART OF DUPLEXER

Y JUNCTION

RF ENERGY
FROM MAGNETRON

ATR 1

ATR 2

TR TUBE
WINDOW – SHORTED

RF ENERGY
TO ANTENNA

ATR TUBE
WINDOWS –
SHORTED

SG 3

TR TUBE IONIZED

SG 2

B. TRANSMISSION

SG 1

RECEIVER
WINDOW –
SHORTED

PART OF DUPLEXER

Y JUNCTION

NOTE 4

TO MAGNETRON

ATR 1

RF ENERGY
FROM ANTENNA

ATR 2

TR TUBE
WINDOW OPEN

SG 3

TR TUBE DEIONIZED

SG 2

RECEIVER
WINDOW –
OPEN

SG 1

TO RECEIVER

C. RECEPTION

NOTES

1. DISTANCE IS 1/4 WAVELENGTH AT LOWER END OF MAGNETRON FREQUENCY BAND
2. DISTANCE IS 1/4 WAVELENGTH AT UPPER END OF MAGNETRON FREQUENCY BAND
3. THE SPARK GAPS (SG) ARE SPACED 1/4 WAVELENGTH
4. ATR TUBES ARE A HIGH IMPEDANCE AND REFLECT SHORT CIRCUIT BACK TO Y JUNCTION

RA PD 468565

Figure 62. (U) Duplexer operation

CONFIDENTIAL

ceiver. Since the ATR tubes normally present a high-series impedance one-quarter wavelength from the Y-junction over the operating range of magnetron frequency, this high impedance is reflected as a short at the Y-junction facing the transmitter system. This short causes the Y-junction leading to the transmitter to appear as a continuous wall. This isolates the transmitter from the waveguide and prevents any dissipation of energy across the transmitter impedance. In the receiver branch of the Y-junction, the amplitude of the received RF signal is insufficient to fire the spark gaps within the TR tube; the RF signal passes through the TR tube coupling windows to the receiver system.

(6) A 3-iris directional coupler (fig. 63) is used in the acquisition duplexer. In the 3-iris directional coupler, irises 1 and 3 are of equal size, but are one-half the size of iris 2. Therefore, the RF energy coupled through iris 2 is equal to the sum

of the RF energy coupled through irises 1 and 3. The irises are spaced one-quarter wavelength apart. A terminating post is mounted opposite iris 1, and a pickup probe post is mounted opposite iris 3. Each post is one-quarter wavelength from the main waveguide wall. When the directional coupler is used for transmitter power and/or frequency measurements, a coaxial cable is connected from the pickup probe post to the frequency and power meter located in the acquisition receiver-transmitter.

(a) The RF energy traveling in the main waveguide (fig. 63) from the magnetron to the antenna is coupled into the directional coupler through the three irises (points A, B, and C). The RF energy entering the directional coupler at point A travels one-quarter wavelength from point A to the terminating post (point D). The RF energy entering the directional coupler at point B travels one quarter wavelength from
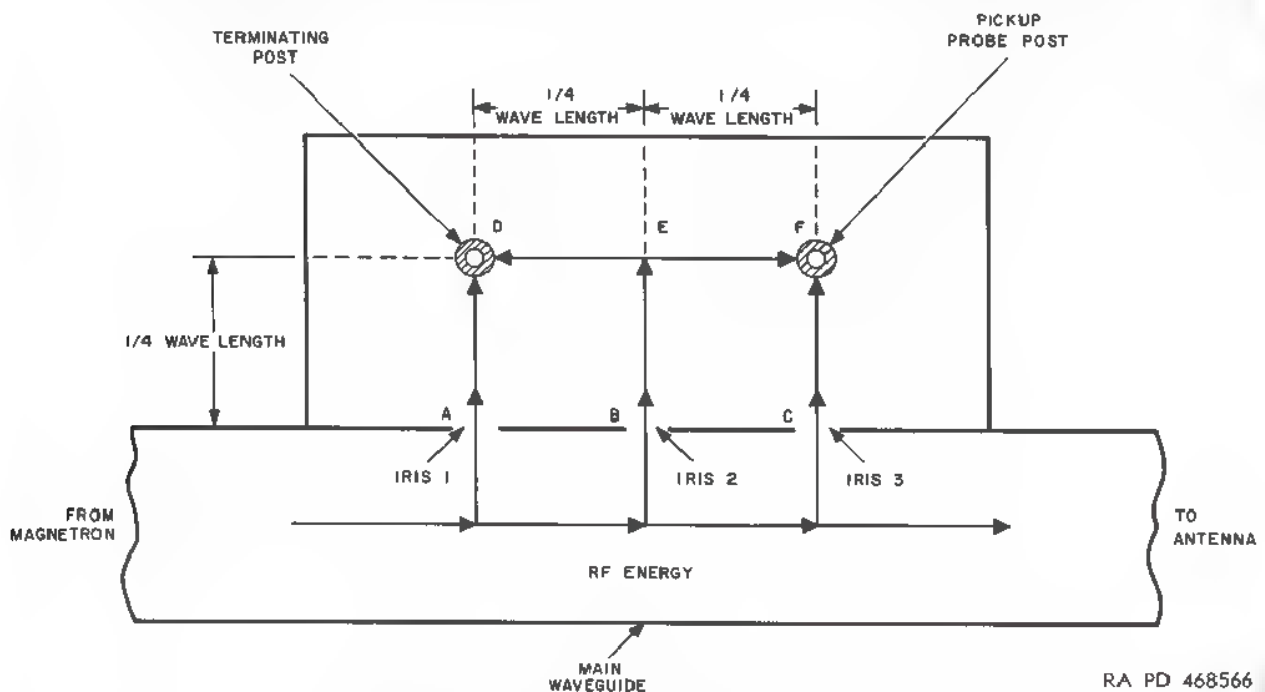
Figure 63 (U) Acquisition directional coupler—electrical characteristics and operation.

point B to point E. At point E, the RF energy divides, with one-half the RF energy traveling one-quarter wavelength to point D and one-half the RF energy traveling one-quarter wavelength to the pickup probe (point F). Using point A as the time reference point, one-half the RF energy entering at point B travels the distance ABED, which is equal to three-quarters of a wavelength. The RF energy traveling the distance ABED arrives at point D one-half wavelength after the RF energy traveling the distance AD. Since the RF energy traveling the paths AD and ABED is equal in magnitude but 180 degrees out of phase, the summation of the RF energy at point D is zero.

(b) The RF energy entering the directional coupler at point C travels one-quarter wavelength from point C to point F. One-half the RF energy entering at point B travels the distance ABEF, which is equal to three-quarters of a wavelength. The energy entering at point C travels the distance ABCF, which is also equal to three-quarters of a wavelength. The RF energy traveling the distance ABEF arrives at point F at the same time as the RF energy traveling the distance ABCF. Since the RF energy traveling the paths ABEF and ABCF is equal in magnitude and in phase, the summation of the RF energy at point F equals twice the RF energy entering the directional coupler at point C.

(7) The AFC coupling probe is mounted in the section of the duplexer waveguide between the TR tube and directional coupler (fig. 61). The probe is U-shaped and forms the center conductor of the coaxial cable at connector J10 (fig. 55, TM 9–1430–257 20). A greatly attenuated RF pulse is coupled from the probe to the AFC system for monitoring the magnetron frequency.

67. Noise Generator 8520785

a. *General.* The noise generator (A9, fig. 55, TM 9–1430–257–20) is a unit of built-in test equipment which is activated only during receiver system performance testing. It generates a continuous-wave noise voltage, the level of which is approximately 15 db. This voltage passes through the normal receiver system channel to monitoring circuitry, where the receiver system performance figure is derived by determining the ratio of normal receiver noise to generated noise.

b. *Detailed Theory.*

(1) The noise generator (fig. 64) consists of argon gas tubes V7 1 through V7–4, which are mounted within a cavity section of the receiver system waveguide. These tubes are mounted in the H-plane of the waveguide and resemble miniature fluorescent tubes. Tubes V7–1 through V7 4 are connected in series across the center-tapped secondary of transformer T3. Tube V7–1 is returned to terminal 6 of T3 through terminal boards TB6–2 and TB2–8. Tube V7–4 is returned to terminal 5 of T3 through terminal boards TB6–3 and TB2–7. Terminal 4 of T3 is returned to the acquisition RF power supply control through terminal board TB2–1. The 120 volts ac is applied to TB2–1 if NOISE GEN—EXC switch S1 on the acquisition RF power supply control is depressed, or NOISE GEN switch S19 on the acquisition control-indicator is placed in the ADJ position. Terminal 1 of T3 is connected directly to the 120-volt neutral line through terminal board TB2–6.

(2) Capacitors C4 and C5 are connected across the primary of T3 and provide power factor correction. The voltage across terminals 2 and 1 in the primary of T3 is also applied through terminal board TB2–4 as excitation for NOISE GEN—GEN ON indicator light I2 on the acquisition RF power supply control and NOISE GEN–ON indicator light I7 on the acquisition control-indicator.

CONFIDENTIAL
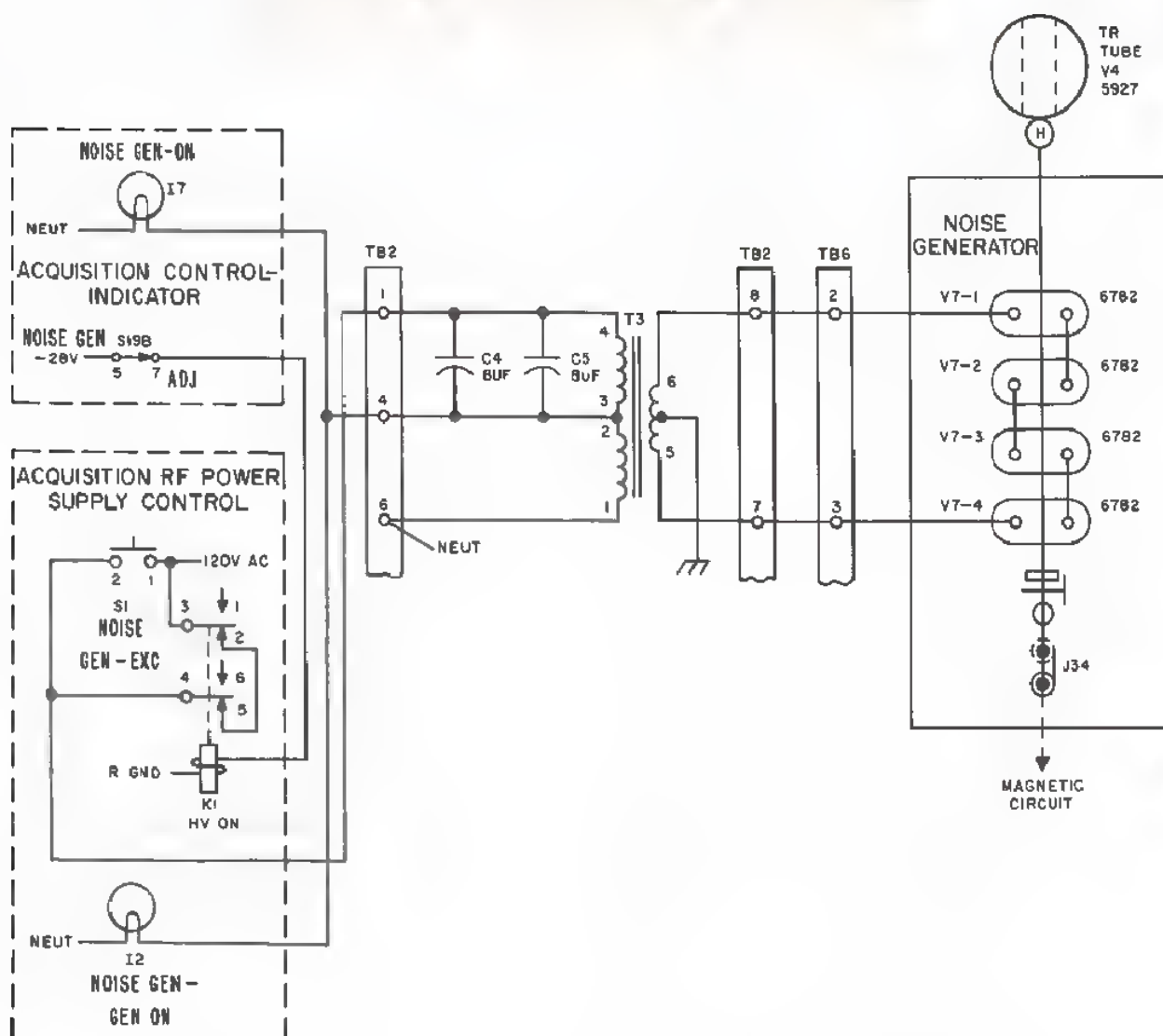
RA PD 468567

Figure 64 (U) Noise generator and power control circuitry simplified schematic diagram.

The turns ratio of T3 steps up the 120 volts in the primary to 2,500 volts in the secondary, and 625 volts is applied across each tube. By center tapping the secondary of T3 to ground, insulation requirements are considerably reduced.

(3) When the noise generator is activated, 625 volts ac from T3 is applied across each tube. This potential insures optimum operation of V7, a tube type 6782.

A tube type 6782 is a particularly stable gas tube, and the noise level of each tube is practically the same. This provides a constant reference level for successive measurements, thus insuring that any change in the receiver performance figure is due to deterioration of the receiver system. Generators V7-1 through V7-4 conduct on both halves of the ac cycle since the electrodes are not polarity sensitive

tive. Consequently, the noise level is constant for as long as the noise generator is energized. Four tubes are required to generate the desired noise level of 15 db.

(4) The continuous wave noise voltage is generated by the random clashing of ions during the ionization and deionization of the argon gas. This noise voltage is radiated into the noise generator cavity and is coupled from the cavity by a U-shaped probe at connector J34. From here, the noise voltage passes through a coaxial cable to the magnetic circuit. An amplified noise voltage from the magnetic circuit is further amplified in the rest of the receiver system. The noise generator level is monitored on the acquisition RF power supply control (fig. 58, TM 9–1430–257–20) on TEST 2 meter M4 in REC NOISE TEST—F.S. 100 position 11 of TEST switch S7; or on the acquisition control-indicator (fig. 21, TM 9–1430 257–20) on MAG FREQ & REC NOISE meter M2 in the ADJ position of NOISE GEN switch S19.

68. Magnetic Circuit 8516184

a. *General.* The magnetic circuit is the first stage of the acquisition receiver. It provides a voltage gain of approximately 20 db to the RF wave received by the acquisition antenna.

b. *Detailed Theory.*

(1) *Physical description.* The magnetic circuit (fig. 55, TM 9 1430–257–20) is composed of traveling wave tube V6, which is mounted within a permanent magnet. Tube V6 is a medium gain, low noise, RF amplifier particularly suitable for amplifying radio frequencies of 1,000 megacycles and above. The main components of V6 (fig. 65) are the electron gun, helix, and collector. The electron gun is composed of the cathode, beam-forming electrode, and three accelerator anodes. Micrometer screws suport the electron gun housing (fig. 66) and enable the electron beam to be positioned horizontally and/or vertically over a small arc. Input

transducer J1 and output transducer J2 are magnetically coupled to the helix for applying the RF wave to V6 and obtaining the amplified RF wave from V6, respectively.

(2) *Circuit operation.*

(a) Electrons are emitted in a wide beam by the cathode of V6 (fig. 65). The electron beam is slightly decelerated and shaped into a narrow beam by the variable negative potential on the beam-forming electrode. The electron beam is accelerated toward the collector by the relative positive potentials at the three accelerator anodes, the helix, and the collector.

(b) The permanent magnet, which encloses the helix, produces an axial magnetic field around the helix that compresses the electron beam.

(c) The helix is a long, loosely-wound coil. Since the coil inductance is shunted by stray coil capacitance, the helix can be considered a transmission line. The RF wave from the acquisition antenna is coupled to the helix through input transducer J1 (fig. 66) and propagated along the axis of the helix. As the RF wave travels along the axis of the helix, it induces an electric field at the center of the helix, which is along the path of the electron beam. This axial electric field alternates in intensity and polarity at the frequency of the RF wave. Although the RF wave travels along the axis of the helix at approximately the speed of light, the axial electric field travels slower than the RF wave by the ratio of the helix pitch to the helix circumference. There is an interaction between the axial electric field and the electron beam, resulting in velocity modulation of the electron beam. The resultant helix wave taken from the magnetic circuit at J2 has an amplitude representing approximately 20-db voltage gain relative to the RF

CONFIDENTIAL

OUTPUT
TRANSDUCER J2

COLLECTOR

PERMANENT
MAGNET

INPUT
TRANSDUCER J1

BEAM FORMING
ELECTRODE (G1)

CATHODE

HEL X

ACCELERATOR
ANODE 3 (G4)

ACCELERATOR
ANODE 2 (G3)

ACCELERATOR
ANODE 1 (G2)
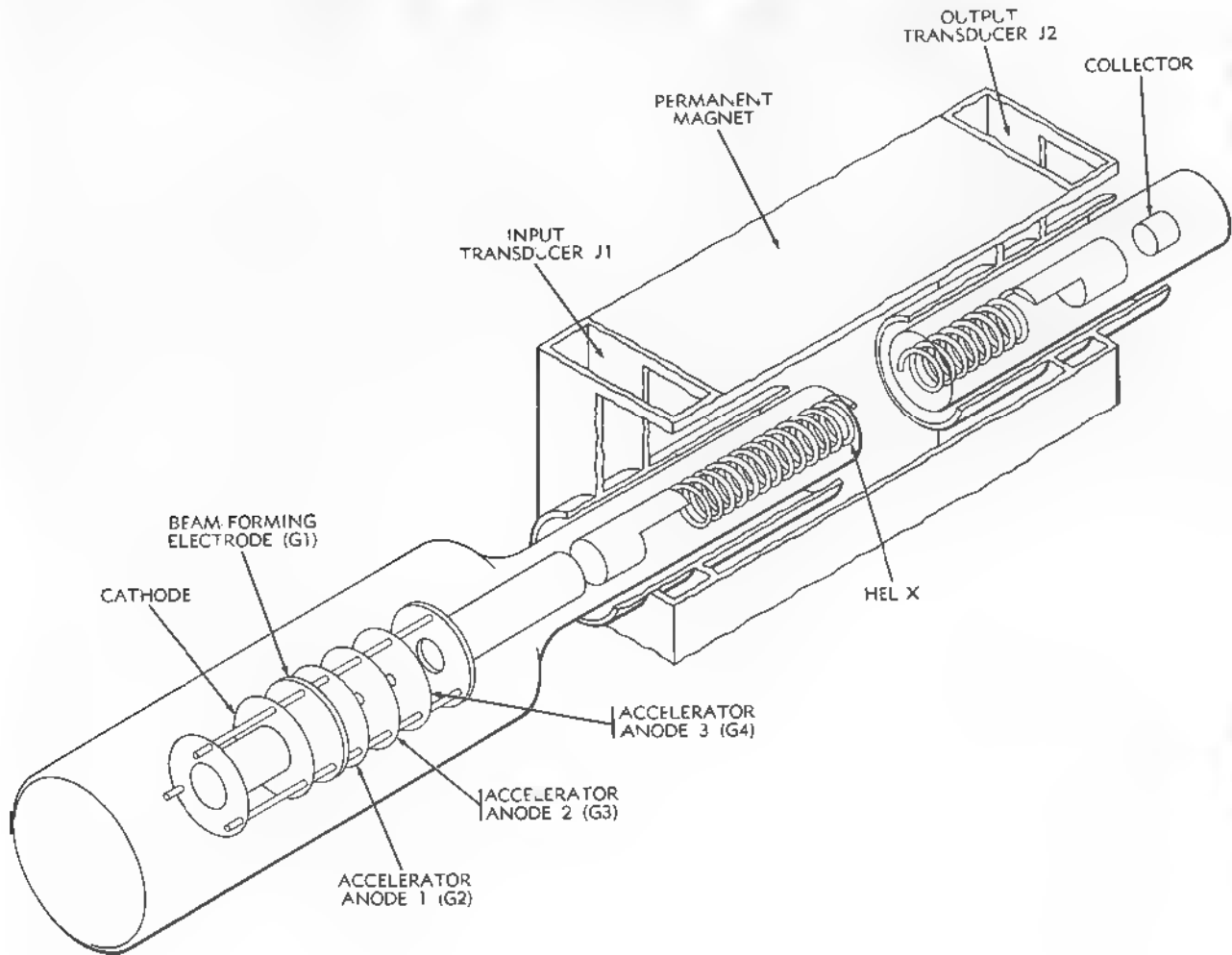
RA PD 468568

Figure 65. (U) Traveling wave tube V6—cutaway view.

wave applied to the magnetic circuit at J1.

(3) *Regenerative feedback.* To achieve stable amplification from V6, it is necessary to prevent reflected energy from J2 from returning to J1. These reflections, resulting from an inherent impedance mismatch between J1 and J2, could cause oscillations within V6. These oscillations could be compared to positive voltage feedback from plate to grid in a conventional vacuum-tube amplifier. In order to prevent oscillations in V6, the forward gain must be less than the backward loss. To accomplish this, the ceramic rod supporting the helix at the input end of the helix is sprayed with an aquadag coating. This coating absorbs RF wave reflections from the output end of the helix which could initiate oscillations within V6.

CONFIDENTIAL

MICROMETER SCREW
(ONLY I OF 2 SCREWS
SHOWN)

ELECTRON GUN
HOUSING

INPUT
TRANSDUCER JI

CERAMIC
SUPPORT
ROD

OUTPUT
TRANSDUCER J2

ELECTRON
GUN

HELIX

PERMANENT
MAGNET

COLLECTOR

MAGNETIC COUPLING
OF TRANSDUCERS TO
HELIX

MAGNETIC COUPLING
OF TRANSDUCERS TO
HELIX
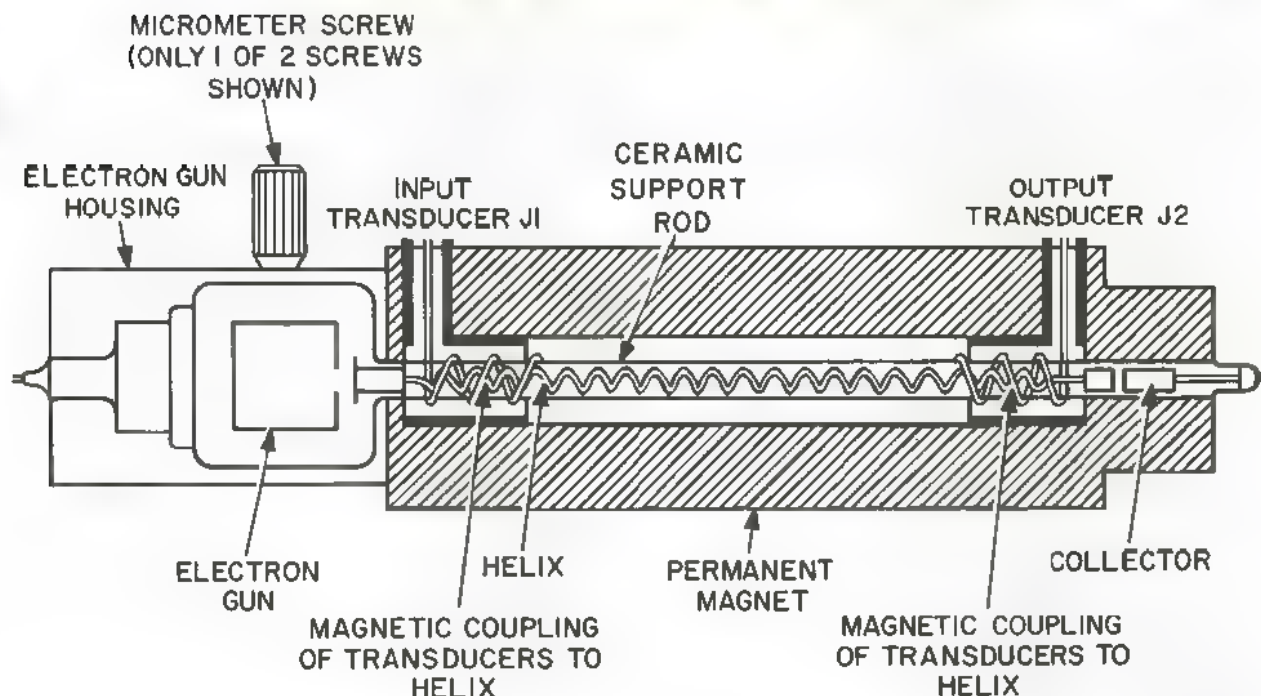
RA PD 468569

Figure 66. (U) Magnetic circuit—cutaway

(4) *Operating voltages and magnetic circuit adjustments.* All dc potentials for the operation of V6 are obtained from the acquisition RF power supply control (fig. 67). Although the dc output from the rectifier in the acquisition RF power supply control is − 800 volts with respect to ground, the potentials at the other electrodes of V6 are measured with respect to cathode potential as a reference. Since the beam-forming electrode (G1) potential is the only one lower than cathode potential, the potentials at the other electrodes of V6 will be positive with respect to cathode potential. By taking potentials as positive with respect to the cathode potential, the potentials indicated on TEST 2 meter M4 will be a more realistic indication of the operation of V6.

(a) The cathode of V6 is connected through terminal board TB3–3 to a fixed potential of − 725 volts with respect to

ground and is taken as the reference potential. No provision is made for indicating cathode potential on M4.

(b) The beam-forming electrode (G1) is connected through TB3–4 to R. F. AMPLIFIER V O L T A G E CONTROLS—G1 variable resistor R11. Variable resistor R11 varies the potential at G1 from 0 to −75 volts; the potential at G1 is indicated on M4 with TEST 2 switch S7 at G1 VOLTS— F. S. 100V position 1. The potential applied to the beam-forming electrode is adjusted to form the electrons emitted from the cathode into a narrow beam.

(c) The micrometer screws on the electron gun housing (fig. 66) are adjusted until a zero current reading is obtained on R. F. AMPLIFIER HELIX CURRENT meter M2 (fig. 67). A zero current reading on M2 indicates that no dc current is being induced in the
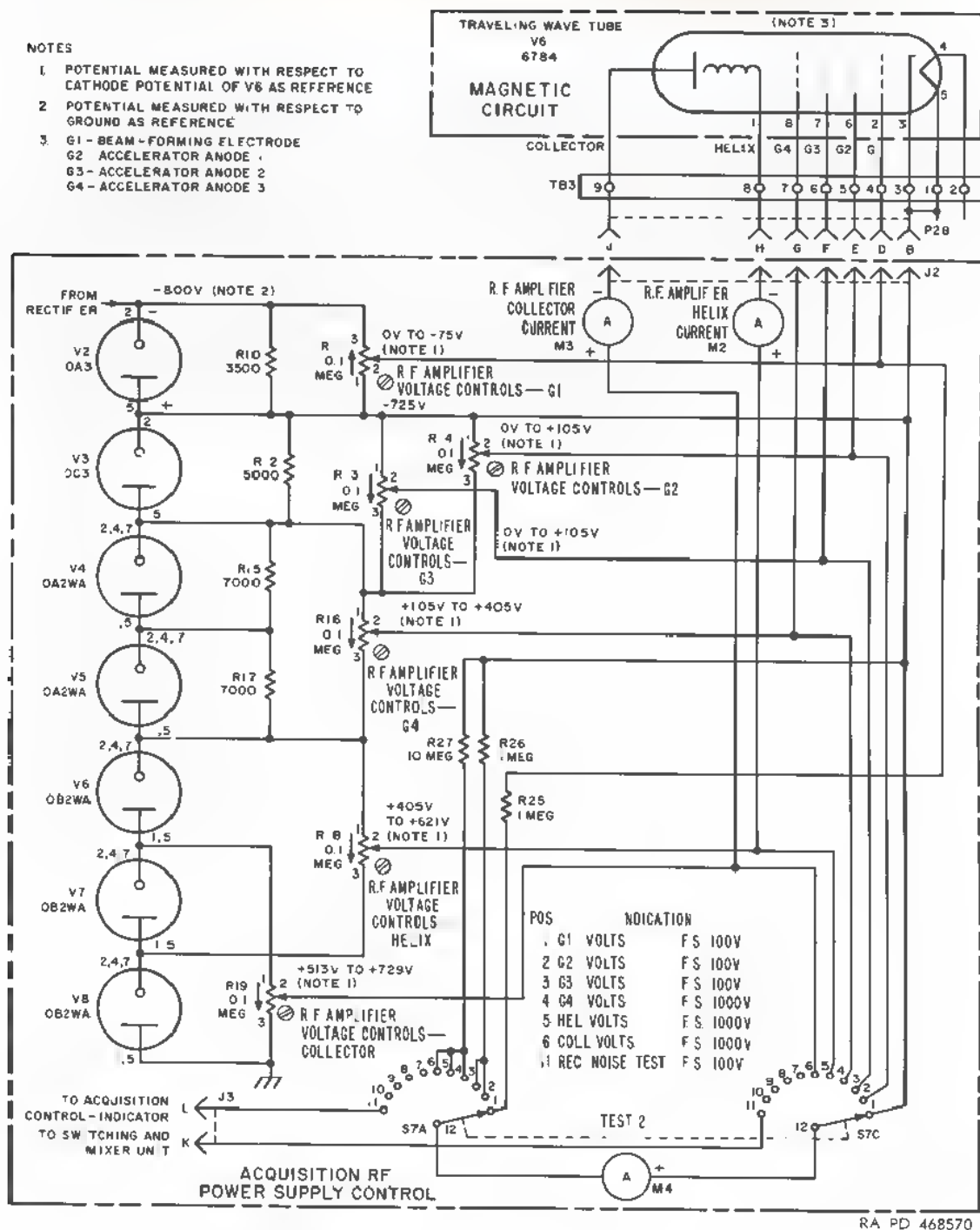
Figure 67 (U) Traveling wave tube V6 electrode potentials schematic diagram

RA PD 468570

helix by the electron beam. This means that the electron beam is exactly centered on the axis of the helix.

(d) Accelerator anode 1 (G2) is connected through TB3-5 to R. F. AMPLIFIER VOLTAGE CONTROLS—G2 variable resistor R14. Variable resistor R14 varies the potential at G2 from 0 to +105 volts; the potential at G2 is indicated on M4 with S7 at G2 VOLTS—F. S. 100V position 2. Accelerator anode 1 provides initial acceleration to the electron beam. With the proper operating potential at the helix, R14 and the micrometer screws are alternately adjusted until a maximum potential is applied to G2 without exceeding a current reading of 1 microampere on M2, or 0.5 milliampere on R. F. AMPLIFIER COLLECTOR CURRENT meter M3.

(e) Accelerator anode 2 (G3) is connected through TB3-6 to R. F. AMPLIFIER VOLTAGE CONTROLS—G3 variable resistor R13. Variable resistor R13 varies the potential at G3 from 0 to +105 volts; the potential at G3 is indicated on meter M4 with S7 at G3 VOLTS—F. S. 100V position 3. Accelerator anode 2 provides additional acceleration to the electron beam initially accelerated by G2. With the proper operating potential at the helix, R13 is adjusted to obtain a minimum indication on M4 with S7 at REC NOISE TEST—F. S. 100 position 11.

(f) Accelerator anode 3 (G4) is connected through TB3-7 to R. F. AMPLIFIER VOLTAGE CONTROLS—G4 variable resistor R16. Variable resistor R16 varies the potential at G4 from +105 to +405 volts; the potential at G4 is indicated on M4 with S7 at G4 VOLTS—F. S. 1000V position 4. Accelerator anode 3 provides additional acceleration to the electron beam initially accelerated by G2 and G3. With the

proper operating potential at the helix, R16 is adjusted to obtain a minimum indication on M4 with S7 at REC NOISE TEST—F. S. 100 position 11. The adjustment of the potentials applied to G3 and G4 to obtain a minimum noise indication on M4 is important, since the noise generated in V6 determines the signal-to-noise ratio of the acquisition receiver.

(g) The helix is connected through TB3-8 to R. F. AMPLIFIER VOLTAGE CONTROLS—HELIX variable resistor R18. Variable resistor R18 varies the potential at the helix from +405 to +621 volts; the potential at the helix is indicated on M4 with S7 at HEL VOLTS—F. S. 1000V position 5. Variable resistor R18 is adjusted to obtain a maximum indication on M4 with S7 in REC NOISE TEST—F. S. 100 position 11. A maximum noise indication on M4 indicates that the noise in V6 is at the highest point, meaning that the gain of V6 is maximum.

(h) The collector is connected through TB3-9 to R. F. AMPLIFIER VOLTAGE CONTROLS—COLLECTOR variable resistor R19. Variable resistor R19 varies the potential at the collector from +513 to +729 volts; the potential at the collector is indicated on M4 with S7 at COLL VOLTS—F. S. 1000V position 6. The collector is normally operated at a maximum +729 volts as indicated on M4, which is actually zero potential with respect to ground. Since the collector is the most positive electrode in V6, the electron beam is attracted to V6 and returned through the acquisition RF power supply control to the cathode of V6.

69. Acquisition Preselector 7621790

a. General. The acquisition preselector is a tunable, high-Q cavity. Its tuning controls are geared to the AFC motor-generator to insure that the preselector follows any changes in magnetron

CONFIDENTIAL

frequency. The preselector passes the return RF pulses but greatly attenuates all signals whose frequency differs from the magnetron frequency. This protects the receiver system from jamming signals, nearby radar interference signals, and the image frequency signal.

b. *Detailed Theory.*

(1) *Preselector operation.*

(a) The preselector cavity (fig. 68) consists of two concentric cylinders, with the smaller cylinder forming the inner wall of the cavity, and the larger cylinder forming the outer wall of the cavity. The cavity is partially inserted into the receiver system waveguide. The received RF signals are coupled to the preselector cavity from the acquisition duplexer through the front coupling windows in the outer wall.

(b) The preselector cavity acts as a parallel resonant circuit. Since the impedance of a parallel circuit is high at resonance, a maximum amplitude output signal is devleoped at the magnetron frequency (fig. 69). Off resonance, the response of the cavity drops sharply; therefore, it presents a low-shunting impedance to interference signals. The RF signals are coupled from the preselector to the main receiver waveguide by the rear coupling windows (fig. 68) in the outer wall.

(c) The outer cavity wall is also pierced by two vertical slots, which are electrically 90° apart for those frequencies other than the desired frequency to which the cavity can resonate. Polyiron damping slugs are mounted in line with these slots against the waveguide wall and absorb the energy which would cause the preselector to resonate at an undesired frequency.

(d) The RF signals from the acquisition duplexer also pass through the crosssectional area of the waveguide not occupied by the preselector cavity. This area is divided into two partitions by a metal post. The post acts as a shunt inductor in the guide, producing a phase lag between the RF signals coupled through the partitions and the output RF signal from the preselector cavity. The output to the receiver frequency-converter is a resultant RF signal produced by the addition of these out-of-phase signals from the partitions and the preselector cavity. At the image frequency, which is 120 megacycles higher than the magnetron frequency, the addition of the out-of-phase signals results in complete cancellation of output signal to the receiver frequency-converter (fig. 69). The sharp dip in the preselector response curve at the image frequency represents a 45-db attenuation of output versus input signal amplitude; the attenuation is constant throughout the tuning range of the preselector cavity.

(2) *Preselector tuning.* Tuning of the preselector cavity is effected by double-cup noncontact tuning plungers (fig. 68) which are positioned by the tuning shaft. The tuning shaft is geared to the AFC motor-generator. The tuning plungers move in the space between the inner and outer walls of the cavity, changing the size of the cavity. Since the volume of the cavity is approximately proportional to the inductance of the tuned circuit formed by the cavity, reducing the size of the cavity increases its frequency and increasing the size of the cavity decreases its frequency. Spurious oscillations in the position of the cavity below the tuning plungers is prevented by a polyiron damping ring mounted on the tuning shaft.

70. Receiver Frequency-Converter 7621829

a. *General.* The receiver frequency-converter is a resonant waveguide cavity which provides a means for mixing the continuous-wave local oscillator signal with the return RF signals to gen-

CONFIDENTIAL

POLYIRON
DAMPING SLUG

FRONT COUPLING
WINDOW

VERTICAL
SLOT

OUTER
CONDUCTOR

SIGNAL FROM
DUPLEXER

INNER
CONDUCTOR

POLYIRON
DAMPING
RING

PRESELECTOR
CAVITY

REAR
COUPLING
WINDOW

METAL POST

SIGNAL TO RECEIVER
FREQUENCY-CONVERTER

PARTITIONS

TUNING
PLUNGERS

POLYIRON
DAMPING
RING

TUNING SHAFT

INCHES
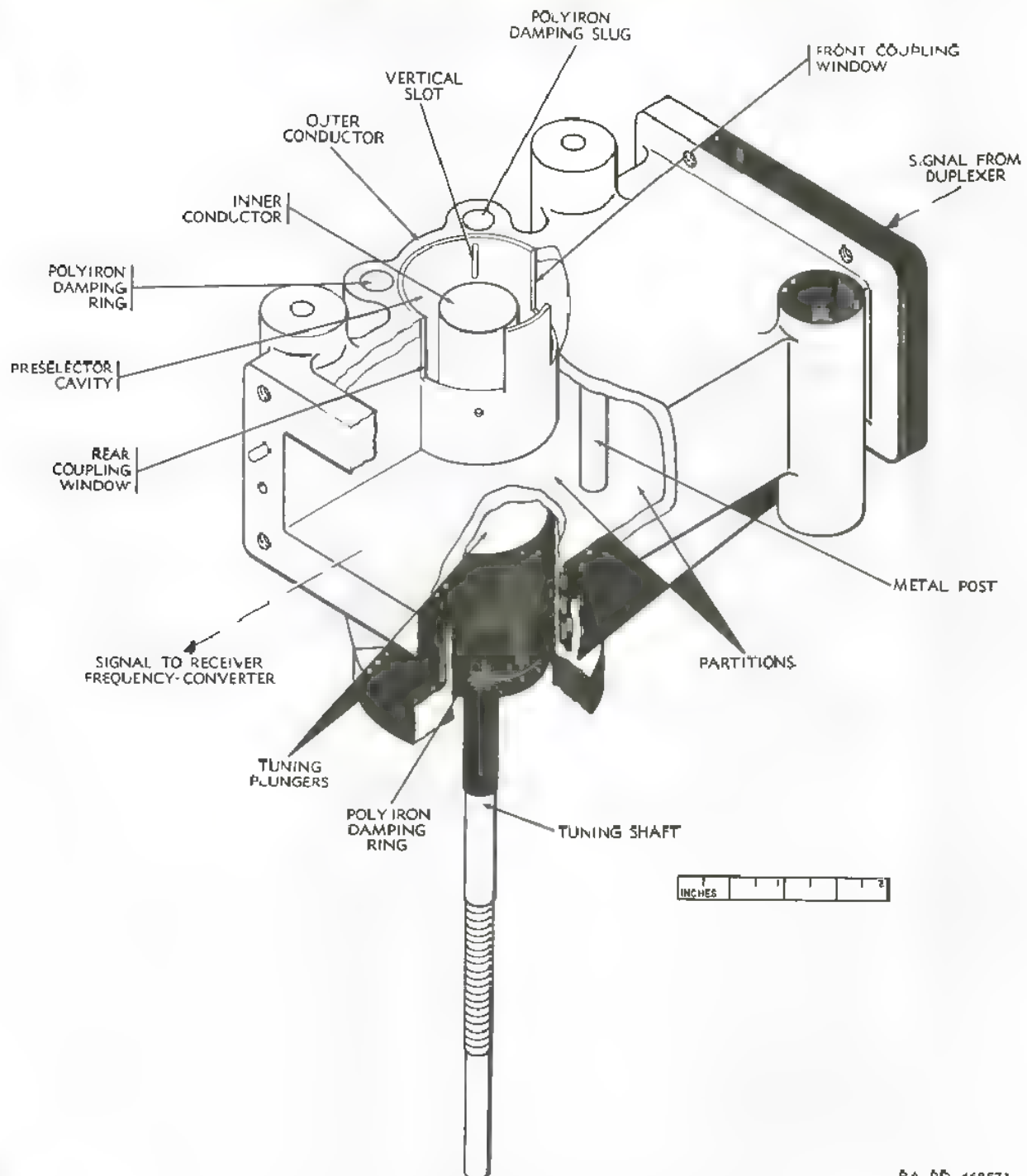
RA PD 468571

Figure 68. (U) Acquisition preselector—cutaway view.

RESPONSE CURVE FOR
ONE SIGNAL FREQUENCY
VALUES SHOWN ARE
REPRESENTATIVE ONLY
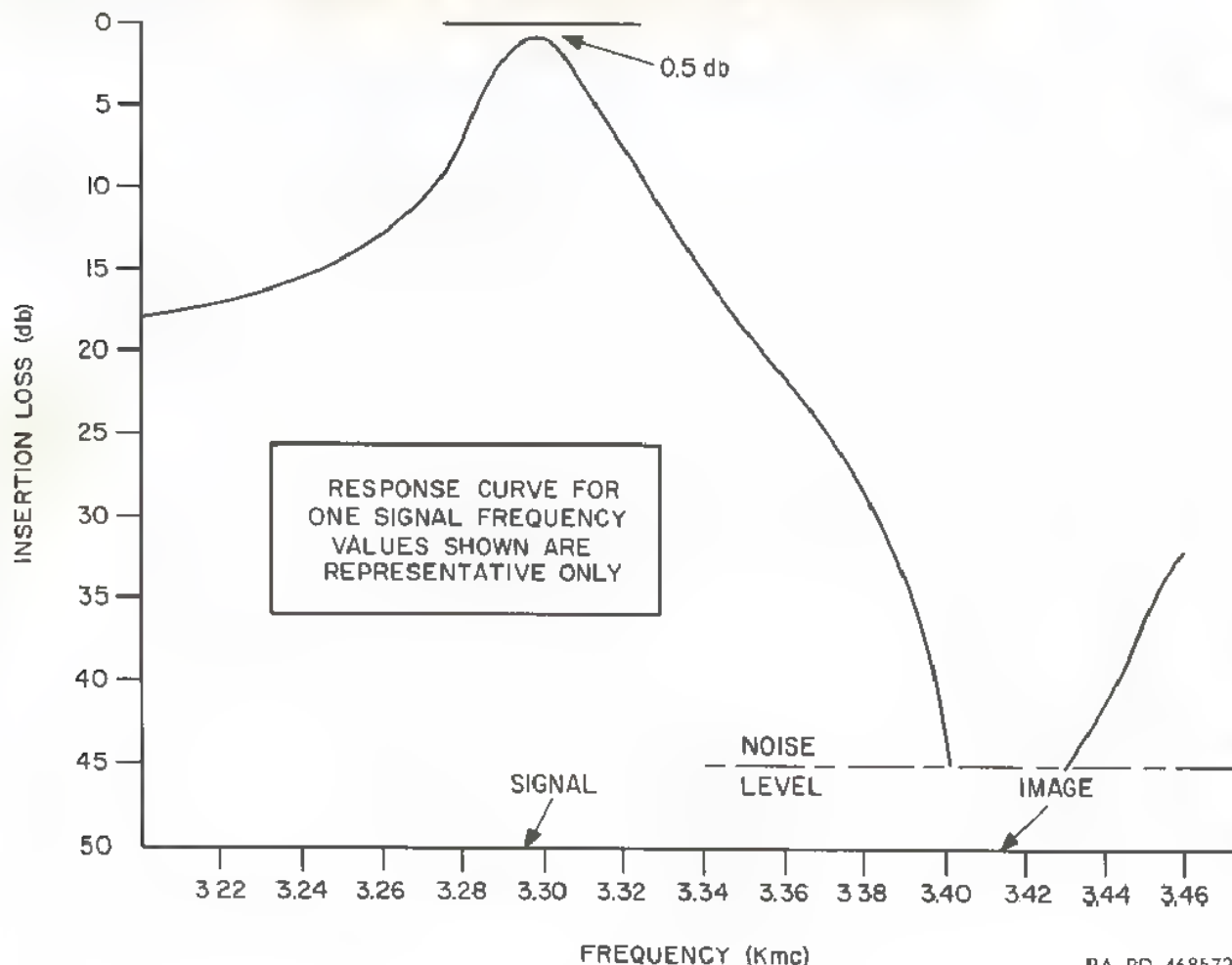
Figure 69 (U) Preselector response curves.

RA PD 468572

erate a 60-megacycle IF signal. The 60-megacycle IF signal is sent to the acquisition IF preamplifier.

b. *Detailed Theory.*

　(1) *Local oscillator signal injection.*

　　(a) A 10-milliwatt continuous-wave local oscillator signal is introduced into the receiver frequency-converter by a U-shaped oscillator coupling loop at connector J21 (fig. 70). This loop is a continuation of the center conductor of the coaxial cable from the acquisition local oscillator; the loop is electrically one-quarter wavelength to assure proper excitation of the cavity. The loop is properly matched to the receiver frequency-converter by a capacitive ring mounted concentric with the loop termination at J21. This ring also serves to mechanically center the conductor. The coupling loop is terminated by a powdered iron core, which attenuates the local oscillator signal to the 1-milliwatt level desired for proper mixing action.

　　(b) Some local oscillator energy is reflected from the mixer loop toward the antenna system. However, the highly selective preselector presents a low impedance to the local oscillator fre-

110
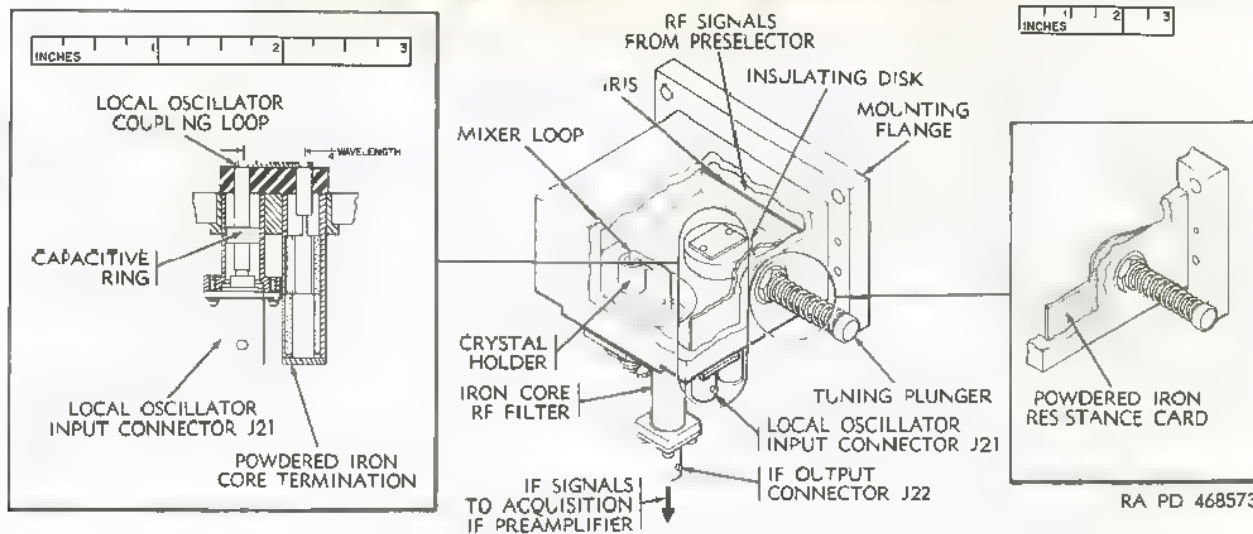
Figure 70. (U) Receiver frequency—converter

quency, thus shunting the oscillator signal to ground. This action prevents any local oscillator radiation from the antenna.

(2) *RF signal injection.* The return RF signals are channeled through the receiver waveguide to the receiver frequency converter, which is flange-mounted to the waveguide. The return RF signals are coupled from the waveguide to the receiver frequency-converter by a capacitive-type window, which also provides proper impedance matching of the receiver frequency-converter to the waveguide.

(3) *Signal conversion.* A 1N28 crystal diode detector is mounted in the crystal holder within the receiver frequency-converter. The detector is properly matched to the cavity by the capacitance of the crystal holder and the inductance of the crystal. A U-shaped mixer loop is terminated at the crystal detector and forms the center conductor of the output IF coaxial cable at IF output connector J22. The mixer loop is mounted in a transverse position to assure maximum pickup of the local oscillator signals and the return RF signals. Since the crystal detector is a nonlinear device, the original, sum, and dif-

ference frequency signals are produced across the mixer loop. These signals are superimposed on the dc voltage level produced by the rectification of these signals. A powdered iron core RF filter is mounted concentric with J22. It blocks the RF signals but passes the IF difference frequency signal to the acquisition IF preamplifier.

(4) *Acquisition preselector output check.*

(a) A spring-back tuning plunger is mounted on the side wall of the receiver frequency-converter and is connected to a resistance card mounted within the cavity. The side of the card facing the cavity wall is coated with powdered iron. The card is tapered at the end facing the acquisition preselector to assure a proper impedance match to the waveguide. Normally, the tuning plunger positions the resistive side of the card flush with the side wall of the cavity, and the card does not absorb any energy from the receiver frequency-converter.

(b) The tuning plunger is depressed when it is desired to check the acquisition preselector for maximum output at the magnetron frequency throughout the preselector tuning range. Depressing

CONFIDENTIAL

the plunger inserts the resistive card into the cavity. Since the card is in line with the acquisition preselector, the card and the capacitive mixer loop are the load of the preselector. However, the resistive card absorbs most of the energy from the acquisition preselector, making the load essentially a resistive load. A resistive load does not change when the acquisition preselector cavity is tuned, as would be the case if the preselector load were the capacitive mixer loop. With a constant load on the acquisition preselector, it can be checked for maximum output throughout its tuning range.

71. Acquisition Local Oscillator 7599343

a. General. The acquisition local oscillator (C10, fig. 55, TM 9–1430–257–20) generates a continuous wave signal, the frequency of which can be varied from 3,160 to 3,560 megacycles. This signal is mixed with the magnetron output in the AFC frequency-converter and with the return RF signals in the receiver frequency-converter to generate 60-megacycle IF signals for use in the acquisition receiver.

b. Detailed Theory.

(1) *Physical description.* Local oscillator V5 is mounted upside down within a coaxial cavity (fig. 71). The first resonator grid makes contact with the outer wall of the cavity; the second resonator grid makes contact with the inner wall of of the cavity. The grids and the cavity form a tuned circuit which resonates at a frequency dependent on the size of the cavity. Cavity size is varied by sliding a noncontact-cup tuning plunger into the space between the inner and outer walls. Since the volume of the cavity is approximately proportional to the inductance of the resonant circuit, reducing the size of the cavity increases the frequency; increasing the size of the cavity decreases the frequency. A polyiron damping ring is mounted on the tuning shaft. It

dampens any spurious oscillations in the portion of the cavity below the shaft.

(2) *Operating voltages.*

(*a*) All dc voltages required by the acquisition local oscillator are obtained from the acquisition RF power supply control. The cathode and control grid are returned to 325 volts (fig. 72), and the resonator grids are at dc ground potential The repeller plate voltage is obtained from the brush arm of repeller plate variable resistor R32. The voltage applied to R32 is controlled by LOCAL OSC CONTROLS—LEVEL variable resistor R21 and LOCAL OSC CONTROLS—SPREAD variable resistor R24 located in the acquisition RF power supply control. These variable resistors adjust the voltage impressed across R32 from −420 volts at terminal 1 to 570 volts at terminal 2. Thus, the voltage available to the repeller plate is −420 volts to 570 volts as determined by the setting of R21 and R24.

(*b*) With the brush arm of R32 at terminal 1 and 420 volts at terminal 1, the repeller plate is still approximately 100 volts negative with respect to the cathode. This makes the repeller plate the most negative electrode in the tube, which is a prerequisite for obtaining oscillations within V5, or any reflex klystron.

(3) *Circuit operation.*

(*a*) Since the resonator grids are highly positive with respect to the cathode, electrons emitted by the cathode are accelerated to a high velocity. As the steady stream of electrons pass through the resonator grids, some electrons leak off into the cavity and initiate weak RF oscillations. The resultant alternating electric field modifies the velocity of the electrons to cause bunching. The bunching action of electrons is velocity modulation. The intensity of

162

CONFIDENTIAL

LOCAL
OSCILLATOR
V5
6BL6

PICKUP
LOOP

PICKUP
LOOP

COAX
CONNECTOR

COAX
CONNECTOR

UPPER DISK
(1ST RESONATOR GRID)

LOWER DISK
(2ND RESONATOR GRID)

TUNING
PLUNGER

REPELLER
CONTACT

COAX CAVITY
OUTER CONDUCTOR

POLYIRON
DAMPING RING

COAX CAVITY
INNER CONDUCTOR

FLEXIBLE REPELLER
VOLTAGE LEAD

TUNING
SHAFT

RA PD 468574

Figure 71 (U) Acquisition local oscillator—cross-sectional view

CONFIDENTIAL

NOTE
ALL VALUES ARE EXPRESSED IN OHMS
UNLESS OTHERWISE INDICATED

RA PD 468575

Figure 72 (U) Acquisition local oscillator—functional schematic diagram

the modulation of the electron stream is determined by the frequency of the RF oscillations in the cavity. The electron bunches return to the resonator grids at the same instant.

(*b*) If the repeller plate voltage is properly adjusted, the bunches of electrons are returned to the cavity when the electric field is positive. The positive electric field tends to repel and thereby decelerates the electron bunches returning from repeller plate to the cavity. When the electron bunches are decelerated, they give up energy to the electric field of the cavity. The transfer of energy reinforces the oscillations, just as regenerative feedback reinforces oscillations within a conventional vacuum tube.

(*c*) Oscillations within V5 can be sustained at several voltage settings of the repeller plate. Oscillations at these points are called modes of operation. One of these modes will yield optimum stability and power. This mode is selected during field adjustments by means of LOCAL OSC CONTROLS—LEVEL variable resistor R21 and LOCAL

OSC CONTROLS—SPREAD variable resistor R24 (fig. 72). Variable resistor R21 is adjusted to obtain the desired modes, and then variable resistor R24 is adjusted to sustain oscillations throughout the frequency range from 3,160 to 3,560 megacycles.

72. Acquisition IF Preamplifier 7620695

a. General.

(1) The acquisition IF preamplifier raises the level of the 60-megacycle IF signal. This amplification more than compensates for any deterioration of the signal-to-noise ratio in the 300-foot cable from the acquisition antenna-receiver-transmitter group to the director-computer group.

(2) The acquisition IF preamplifier also maintains a high signal-to-noise ratio in the acquisition receiver through low noise amplifiers. An overall band pass of 2.5 megacycles insures accurate IF signal reproduction.

b. Detailed Theory.

(1) *Tuned IF amplifier V1.*

(*a*) The input signal at connector P1 (fig. 56, TM 9-1430-257-20) is a 60-megacycle IF signal superimposed on the dc

CONFIDENTIAL

level produced by the crystal detector current in the receiver frequency con verter. This signal is applied across a low pass filter composed of inductors L1 through L3 and capacitors C1 through C3. The filter removes the 60 megacycle component, but passes a dc crystal current to connector P2-3 and connector J2-3. The 60 megacycle IF signal is coupled through capacitor C4 to the cathode of tuned IF amplifier V1, which is a grounded-grid triode.

(b) In the cathode circuit of V1, the IF signal is developed across inductor Z1, which resonates with the input circuit capacitances at 60 megacycles. Inductor Z1 is factory-tuned to obtain an optimum signal-to-noise ratio. An amplified output IF signal is developed across the primary of transformer T1, which resonates with the shunt circuit capacitances at 60 megacycles. Transformer T1 is sharply peaked to the center IF of 60 ± 1.5 megacycles. Since the signal to noise ratio is high at the center frequency, a minimum of noise is applied to tuned IF amplifier V2. The control grid of V1 is grounded to provide a better signal-to-noise ratio and prevent oscillations. The plate voltage of V1 is dropped to a lower value than the +150 volts at connector J2-2 and connector P2-2 by the paral lel resistor network composed of resistors R18, R19, and R20. This insures that tube noise does not receive sufficient amplification to override the IF signal, whose amplitude is in microvolts.

(2) *Tuned IF amplifier V2.* The input circuit of V2 is composed of the secondary winding of T1, input circuit capacitances, and capacitor C7. This network forms a series-tuned circuit, which is shunted by fixed inductor L4 to insure an optimum input impedance. An amplified output IF signal is developed across a

tuned circuit composed of inductor L5 and the shunt circuit capacitances. The Q, or figure of merit, of this tuned circuit is sufficiently lowered by resistor R4 to pass the desired band of frequencies. A grounded-grid amplifier is used as V2 for the reasons described in (1) above.

(3) *Tuned IF amplifier V3.*

(a) The 60-megacycle IF signal from V2 is coupled through capacitor C9 to the grid of medium gain tuned IF amplifier V3. In the input of V3, the IF signal is developed across a tuned circuit consisting of fixed inductor Z2 and the input circuit capacitances. Inductor Z2 is factory-tuned to peak the signal to the center frequency. An amplified output IF signal is developed across a tuned circuit composed of the primary of double-tuned transformer T2 and output circuit capacitances.

(b) Double-tuned transformer T2 provides a steep-sided response curve, through overcoupling of the primary and secondary windings. These windings are factory-set for the desired response curve by physically positioning the windings, and cannot be readjusted in the field. The primary and secondary windings of T2 are loaded by resistors R7 and R8, respectively. These resistors lower the Q, or figure of merit, of the tuned circuits to pass the desired band of frequencies.

(4) *Tuned IF amplifier V4.* The 60-megacycle IF signal is developed across the secondary of T2 and the input circuit capacitances. An amplified output IF signal is developed across a tuned circuit composed of the primary of double-tuned transformer T3 and output circuit capacitances. This tuned circuit is loaded by resistor R12 to obtain the desired bandpass.

(5) *Tuned IF amplifier V5.* The 60-megacycle IF signal is developed across the secondary of T3 and the input circuit capacitances. This tuned circuit is loaded

CONFIDENTIAL

by resistor R13 to obtain the desired bandpass. An amplified output IF signal is developed across a tuned circuit composed of the primary of transformer T4 (secondary not used) and output circuit capacitances. This tuned circuit is loaded by resistor R21 to obtain the desired bandpass. The output signal is properly matched to the 300-foot coaxial cable at connector J1 by fixed capacitors C31, C19, and factory-adjusted variable capacitor C20.

(6) *IF preamplifier gain control circuit.* The gain of V3, V4, and V5 is determined by RECEIVER-GAIN variable resistor R3, located on the acquisition control-indicator, which applies a variable dc level of from 0 to −20 volts to the control grids from connector J2–1 and connector P2–1. Additional grid bias is provided for the first portion of the acquisition radar range by a negative 130-microsecond sensitivity time control (STC) gate, which is superimposed on the variable dc level.

(7) *Decoupling networks.* Since continuous-wave oscillations in a cascaded amplifier can be caused by interstage coupling through the common impedances of power supplies, special care is taken to decouple all signal lines from power sources. In the plate circuits, the decoupling capacitors and resistors are C6, R2, C8, R16, C22, C12, R11, C15, R15, C18, R17, and C21. In the grid circuits, the decoupling capacitors and resistors are C10, R5, C13, R10, and C16. In the filament circuits, the decoupling capacitors and inductors are C23, L7, C24, C25, L8, C26, L6, L9, C27, L10, C28, L11, C29, L12, and C30.

73. AFC Frequency-Converter 7621830

a. General. The AFC frequency-converter mixes acquisition local oscillator signals with attenuated RF signals from the magnetron to produce an AFC IF signal. This IF signal is sent to the acquisition AFC for use in correcting IF deviations from 60 megacycles.

b. Detailed Theory.

(1) *Local oscillator injection.* A 10-milliwatt continuous-wave local oscillator signal is introduced into the AFC frequency-converter by a U-shaped directional coupling loop mounted at connector J20 (fig. 73). This loop forms the continuation of the center conductor of the coaxial cable from the acquisition local oscillator. The loop is electrically one-quarter wavelength for proper signal injection. The loop is terminated by a powdered iron core, which is mounted concentric with the loop at the termination point. The powdered iron core attenuates the acquisition local oscillator signal to the 1-milliwatt level desired for proper signal mixing action. Impedance matching to the AFC frequency-converter is accomplished by mounting a capacitive ring concentric with the coupling loop at J20. This ring also serves to mechanically center the conductor. The acquisition local oscillator signal radiates into the AFC frequency converter toward the mixing line.

(2) *Magnetron signal injection.* A greatly attenuated RF signal from the magnetron is fed through a coaxial cable to connector J19. An exciting probe is connected to J19, and it is mounted within a short circular section of waveguide within the AFC frequency-converter. The probe excites the waveguide, and the RF signal travels down the waveguide to the mixing line. Since a wide frequency response is required for proper AFC system operation, the waveguide is shunted at the coupling point to the mixing line by a low impedance quarter-wave line formed by an impedance post. The impedance post also serves as a housing for the RF filter in the mixing line output at connector J18.

(3) *Signal detection.* A 1N28 crystal detector is mounted on the side wall of the

CONFIDENTIAL

CRYSTAL DETECTOR
1N28

CRYSTAL
MOUNTING

CONTACT
FINGERS

ACQUISITION LOCAL
OSCILLATOR SIGNALS

MIXING
LINE

IRON CORE
RF FILTER

IMPEDANCE
POST

CONNECTOR J20

CAPACITIVE
RING

AFC IF SIGNALS

POWDERED IRON
CORE TERMINATION

CONNECTOR J18

U SHAPED
COUPLING LOOP

CIRCULAR
WAVEGUIDE

EXCITING
PROBE

INCHES

CONNECTOR J19

ATTENUATED RF
SIGNALS FROM MAGNETRON
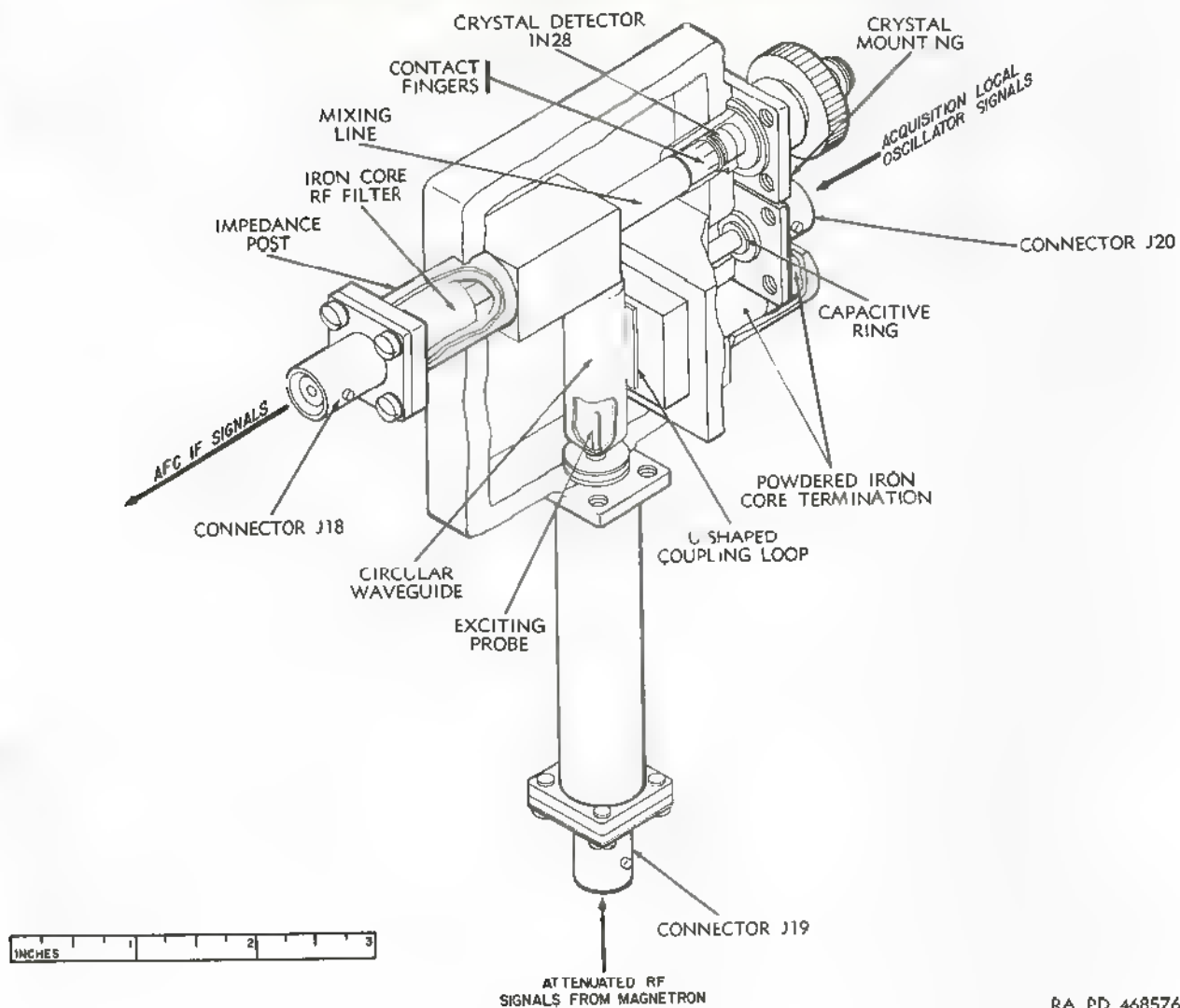
RA PD 468576

Figure 73. (U) AFC frequency-converter—cutaway view.

AFC frequency-converter and is properly matched by the capacitance of the crystal mounting and the inductance of the crystal. The crystal is connected to the probe end of the mixing line by contact fingers. The acquisition local oscillator and attenuated magnetron RF signals flow in the mixing line and are applied across the crystal detector. Since the crystal detector is a nonlinear device, it mixes these signals and produces the original, sum, and difference frequency sig-

nals in the mixing line. A powdered iron core RF filter is mounted concentric with the mixing line at J18. The filter blocks the RF signals, but passes the IF signal to the acquisition AFC for use in correcting IF deviations from 60 megacycles.

74. Acquisition AFC 9143030 ~~8176949~~

a. General. The acquisition AFC maintains the 60-megacycle IF necessary for proper acquisition receiver operation. The acquisition AFC detects

any IF deviation from 60-megacycles and controls the AFC motor-generator which retunes the acquisition local oscillator to restore the 60-megacycle IF. The acquisition AFC also searches for a new frequency lock-on point for the acquisition local oscillator when there is a shift in the acquisition magnetron frequency.

b. Detailed Theory. The acquisition AFC (fig. 57, TM 9–1430–257–20) consists of IF amplifiers V1 through V3; limiter V4; detectors V5A and V5B; video amplifier V6A; cathode follower V6B; pulse stretchers V7A and V7B; modulators V8A, V8B, V9A, and V9B; converters V10A and V10B; and relay amplifiers V11A and V11B.

   (1) *IF amplifier V1.*

      (*a*) IF signals are applied from the AFC frequency-converter through connector J1 and developed across the primary of transformer T1. The IF signals are in the form of 1-microsecond pulses, having a repetition rate of 500 pps. The IF signals are superimposed on a dc voltage level resulting from the rectification of the acquisition local oscillator signals and acquisition magnetron signals in the AFC frequency-converter. The primary of T1 is fixed-tuned with circuit capacitances to resonate at 60 megacycles. The primary is loaded by resistor R28, which broadens the response of T1 to obtain the desired 10-megacycle bandwidth centered at 60 megacycles. The IF signals developed across the primary of T1 are also developed across the low-pass filter composed of capacitors C45 and C1 connected in series with the primary of T1. The low-pass filter bypasses the IF signals to ground. The resultant dc crystal current is applied through connector P1–6 to the acquisition RF power supply control for monitoring on TEST 2 meter M4.

      (*b*) IF amplifier V1 is a conventional medium-gain, wideband IF amplifier. The IF signals induced in the secondary of T1 are applied to the control grid of V1. The secondary of T1 is fixed-tuned with circuit capacitances to resonate at 60 megacycles and loaded by resistor R5 to obtain the desired 10-megacycle bandwidth. Amplified IF signals at the plate of V1 are developed across the primary of transformer T2. IF signals at the plate and screen grid of V1 are decoupled from the +150-volt supply by resistor R17 and capacitor C10.

   (2) *IF amplifiers V2 and V3.* Amplifiers V2 and V3 are identical with V1 in purpose and component operation. The IF signals from V1 are amplified by V2 and V3 and coupled through transformer T4 to the control grid of limiter V4.

   (3) *Limiter V4.* Limiter V4 eliminates variations in amplitude of the IF signals. This amplitude limiting permits detectors V5A and V5B to respond only to frequency variations above or below 60 megacycles.

      (*a*) The control grid of V4 is biased slightly above cutoff by a combination of cathode bias voltage developed across cathode resistor R4 and limiter (grid-leak) bias voltage. The limiter bias voltage is developed by resistor R22 and capacitor C4 during the positive-going half-cycles of the IF signals. The limiter bias voltage level is maintained between signals by the long time constant of R22 and capacitor C37. The IF signals induced in the secondary of T4 are applied to the control grid of V4. The secondary of T4 is fixed tuned with circuit capacitances to resonate at 60 megacycles and loaded by resistor R8 to obtain the desired 10-megacycle bandpass. During the positive-going half-cycles of the IF signals, V4 is driven into saturation. During the negative-going half-cycles of the IF signals, the combination of the negative-going grid voltage and limiter bias voltage quickly drives V4 to cutoff. As a result, all amplitude variations in the IF signals are removed by

a combination of cutoff and saturation limiting. Thus, the IF signals developed across the primary of zero discriminator transformer T5 in the plate circuit of V4 have constant amplitude but retain any frequency variations from 60 megacycles.

(b) The primary of T5 is broad tuned to resonate at 60 megacycles by response discriminator variable capacitor C40 and loaded by resistor R12 to obtain the desired 10-megacycle bandwidth. The voltage applied to the plate of V4 is reduced from +150 volts to a low value by resistor R26. IF signals at the plate and screen grid of V4 are decoupled from the +150-volt supply by capacitor C13. An additional decoupling network composed of resistor R20 and capacitor C3 is connected between the plate of V4 and the +150-volt supply.

(c) The limiter bias voltage developed at the control grid of V4 is applied through connector P1 4 to TEST 2 meter M4 in the acquisition RF power supply control for monitoring purposes. A limiter current of 3 to 6 microamperes indicates normal operation of all AFC system circuits up to and including the control grid circuit of V4. However, absence of limiter bias voltage does not necessarily indicate a component malfunction, since limiter bias voltage is developed only when the IF signal falls within the 10-megacycle bandpass of V1, V2, and V3. Limiter bias voltage is also applied from V4 to the grid of relay amplifier V11A.

(4) *Detectors V5A and V5B.*

(a) The IF signals developed across the primary of T5 are induced in the secondary of T5. The plate of V4 is also directly coupled to the junction of capacitors C14 and C15, which are connected across the secondary of T5. The secondary of T5, C14, and C15 comprise a series-resonant circuit, the bandwidth of which is broadened by

resistor R13 to obtain the desired 10 megacycle bandwidth. The amplitude-frequency response of detectors V5A and V5B is affected by the frequency response of T5. The frequency response of T5 is adjusted by varying C40 in the primary circuit, and by slug-tuning the secondary circuit. The frequency response of T5 is properly adjusted when equal frequency deviations above and below 60 megacycles produce error pulses of equal amplitude and opposite polarity from V5A and V5B.

(b) Detectors V5A and V5B, inductors L1 and L2, capacitors C18 and C19, and resistors R14 and R15 comprise a shunt detector. Resistor R67 dampens any parasitic oscillations originating in the control grid circuit of video amplifier V6A, which is connected to the output of V5A and V5B. The impedance of a shunt detector is low, and therefore does not change appreciably when a new V5 (tube type 6AL5) is inserted. Thus, a constant impedance driving source to V6A is obtained, thereby eliminating the necessity of returning T5 after each tube change. Inductors L1 and L2 present a high series impedance to the IF frequency, thus isolating the remaining stages from IF signal interference. Inductors L1 and L2 also provide a low-resistance path for the diode currents. Although C19 is a smaller size capacitor than C18, the circuit is balanced since the additive effect of the tube capacitances are in parallel with C19. The output voltage from V5A and V5B is developed across R14 and R15 and can be monitored at test point TP1. The error pulse voltage is the algebraic addition of the opposite polarity voltage drops across R14 and R15.

(c) The voltage applied to the plate of V5A is the primary voltage plus the voltage developed across C14. The voltage ap-

CONFIDENTIAL

plied to the plate of V5B is the primary voltage plus the voltage across C15. The resultant plate voltages determine the currents through V5A and V5B. These currents determine the amplitude of the voltage drops across R14 and R15. The operation of V5A and V5B is explained in *1* through *3* below for the following three conditions: IF signal at 60 megacycles, IF signal lower than 60 megacycles, and IF signal higher than 60 megacycles. For each of these three conditions, different phase relationships exist between voltages across C14, C15, and the primary of T5.

1. IF signal at 60 megacycles. The 60-megacycle IF signal is applied across the series circuit composed of C14, C15, and the secondary of T5. The resonant frequency of the series circuit is 60 megacycles. At 60 megacycles, the inductive reactance (X_L) equals the capacitive reactances (X_C). Consequently, X_C cancels X_L, and the tuned circuit appears purely resistive. Voltage and current in the secondary of T5 are in phase with the voltage in the primary of T5. The current leads the voltage through C14 and C15 by 90°. Measured from terminals 3 to 4 on the secondary of T5, the voltages across C14 and C15 are in phase. However, they are 180° out of phase with each other as applied to the plates of V5A and V5B. The summation of the primary voltage and the voltage across C14 produces V5A plate voltage, which is equal in amplitude to V5B plate voltage, produced by the summation of the primary voltage and the voltage across C15. Equal amplitude plate voltages result in equal conduction in V5A and V5B. This causes equal and opposite voltage drops across R14 and R15, producing a 0-volt

error pulse output with respect to ground.

2. IF signal lower than 60 megacycles. When the IF signal is lower than 60 megacycles, the series circuit composed of C14, C15, and the secondary of T5 is no longer resonant. Below resonance, X_C is greater than X_L. This causes secondary current to lead secondary voltage by a phase angle proportional to the frequency deviation. However, in-phase voltages across C14 and C15 still lag secondary current by 90°, and are 180° out of phase with each other as applied to the plates of V5A and V5B. The voltage across C14 is now less than 90° out of phase with the primary voltage, and the voltage across C15 is more than 90° out of phase with the primary voltage. The summation of the primary voltage and the voltage across C14 produces V5A plate voltage, which is larger in amplitude than V5B plate voltage, the summation of the primary voltage, and the voltage across C15. The unequal plate voltages cause more current through V5A than through V5B, resulting in a larger voltage drop across R15 than across R14. The addition of the oppositive polarity voltages across R14 and R15 produces a resultant error pulse having a duration of 1-microsecond, a repetition rate of 500 pps, and a positive polarity with respect to ground.

3. IF signal higher than 60 megacycles. When the IF signal applied to the series circuit composed of C14, C15, and the secondary of T5 is higher than 60 megacycles, the converse of the condition in *2* above occurs. In this case, X_L is greater than X_C, causing the series circuit to act inductively. Secondary current lags secondary voltage by a phase angle dependent on the frequency devia-

CONFIDENTIAL

tion. In-phase voltages across C14 and C15 lag secondary current by 90°, and are 180° out of phase with each other as applied to V5A and V5B. The voltage across C15 is now less than 90° out of phase with the primary voltage, and the voltage across C14 is more than 90° out of phase with the primary voltage. The summation of the voltage across C15 and primary voltage produces V5B plate voltage, which is larger in amplitude than V5A plate voltage, produced by the summation of the primary voltage and the voltage across C14. The unequal plate voltages cause more current through V5B than through V5A, resulting in a larger voltage drop across R14 than across R15. The addition of the opposite polarity voltages across R14 and R15 produces a resultant error pulse having a duration of 1-microsecond, a repetition rate of 500 pps, and a negative polarity with respect to ground.

(5) *Video amplifier V6A.* The error pulses produced by V5A and V5B when the IF deviates from 60 megacycles are directly coupled to the grid of V6A (fig. 57, TM 9–1430–257 20). The amplified and inverted error pulses at the plate of V6A are coupled through capacitor C20 to the center tap of the secondary winding of pulse stretching transformer T6. If the output of modulators V8A, V8B, V9A, and V9B is to be proportional to the amplitude and polarity of the error pulses produced by V5A and V5B, then the gain of V6A cannot be allowed to vary. The degenerative feedback voltage developed across unbypassed cathode resistor R16 controls the gain of V6A. Thus, the stability of V6A is improved by making the stage gain less dependent upon tube characteristics and component aging. Error pulse frequencies at the plate of V6A are decoupled from the +150-volt supply by capacitor C2.

(6) *Cathode follower V6B.*

(a) Gate pulses having a duration of 1 microsecond, an amplitude of +30 volts, and a repetition rate of 500 pps are applied from the acquisition magnetron pulsing circuits to connector J2. These gate pulses occur simultaneously with the application of the IF signals at J1. From J2, the gate pulses are developed across cable terminating resistor R25 and applied through resistor R24 to the grid of V6B. Crystal diode CR1 in the grid circuit of V6B clips the peaks from the gate pulses. A bias voltage of +25 volts is applied to the cathode of CR1 through the voltage divider composed of resistors R60 and R62 connected from ground to the +150-volt supply. The bias voltage developed across R62 is stabilized by capacitors C39 and C24 connected in parallel with R62. The portion of each gate pulse which exceeds +25 volts causes CR1 to conduct. When CR1 conducts, the voltage of the gate pulse in excess of +25 volts is developed across resistor R24, thus clamping the grid of V6B at +25 volts.

(b) During quiescence, V6B is conducting near cutoff due to the small positive bias voltage applied to the cathode through the voltage divider composed of resistor R61 and cathode resistor R27 connected from ground to the +150-volt supply. The gate pulses applied to the grid of V6B cause increased conduction, resulting in positive-going pulses at the cathode. The gate pulses across cathode resistor R27 are coupled through capacitor C36 and developed across primary winding 1–2 of T6 and resistor R30 connected in parallel.

(7) *Pulse stretchers V7A and V7B.* Pulse stretchers V7A and V7B convert the positive or negative error pulses from V6A

CONFIDENTIAL

into pulsating dc control voltages having a dc level and polarity equal to the amplitude and polarity of the error pulses. The dc control voltages are applied as grid bias voltages to operate modulators V8A, V8B, V9A, and V9B.

(*a*) When the IF is 60 megacycles, the only input to V7A and V7B is the gate pulses applied from V6B to the primary of T6. The gate pulses induced into the secondary windings of T6 result in equal amplitude, opposite polarity gate pulses at T6–3 and T6–6. The gate pulses applied to the plate of V7A from T6–3 are positive, and the gate pulses applied to the cathode of V7B from T6–6 are negative. Capacitor C43 insures that the secondary of T6 is balanced. The gate pulses applied to the plate of V7A and the cathode of V7B cause equal conduction in V7A and V7B. Since the resulting currents through capacitor C23 are of equal amplitude and opposite phase, C23 is uncharged. Capacitor C21 in the cathode circuit of V7B and capacitor C22 in the plate circuit of V7A charge to the peak voltage of the gate pulses. Between pulses, the large resistance of resistor R29A in the cathode circuit of V7B and resistor R29B in the plate circuit of V7A hold C21 and C22 charged to approximately the peak gate pulse voltage. Capacitor C21 and R29A place a positive bias voltage at the cathode of V7B; C22 and R29B place a negative bias voltage at the plate of V7A. Thus, V7A and V7B are cut off during the period between gate pulses. This insures that the pulsating dc control voltages developed across C23 are functions of only the polarity and amplitude of the error pulses from V6A.

(*b*) If the IF deviates from 60 megacycles, the positive or negative error pulses at the plate of V6A are coupled through capacitor C20 to the center tap of the secondary of T6. From the center tap, the error pulses are developed across resistor R32, which is in parallel with each secondary winding of T6. Coincident with the error pulses, gate pulses are applied from V6B to the primary of T6. The induced gate pulse voltage in winding 5–6 is negative at the cathode of V7B. The induced pulse voltage in winding 3–4 is positive at the plate of V7A. The algebraic addition of the error pulses to the gate pulses produces unequal conduction in V7A and V7B. Since unequal currents of opposite phase flow through C23, a resultant charge is developed across C23.

1. If the error pulses from V6A are positive, the positive error pulses developed across R32 aid the positive gate pulses at the plate of V7A and oppose the negative gate pulses at the cathode of V7B. Pulse stretcher V7A conducts more than V7B, and the larger current through V7A produces a resultant positive charge on C23.

2. If the error pulses from V6A are negative, the negative error pulses developed across R32 aid the negative gate pulses at the cathode of V7B and oppose the positive gate pulses at the plate of V7A. Pulse stretcher V7B conducts more than V7A, and the larger current through V7B produces a resultant negative charge on C23.

3. Between gate pulses, C23 is held charged to the peak voltage appearing between ground and the output of V7A and V7B, since the only discharge path for C23 is through the long time-constant circuit composed of resistor R31 and capacitor C41. The dc control voltage developed across C23 causes an unbalance in modulators V8A, V8B, V9A, and

CONFIDENTIAL

V9B. The unbalanced modulators produce a voltage which causes the AFC motor-generator to retune the acquisition local oscillator. As the IF is being corrected to 60 megacycles, error pulses having a decreasing amplitude are coupled from V6A to V7A and V7B. Unequal currents flow through V7A and V7B, producing a charge on C23 of the same polarity but decreasing in amplitude. The decrease in error pulse amplitude, and hence the decrease in dc control voltage amplitude, is directly proportional to the amount of correction of the IF. This action is repeated during each succeeding gate pulse until the IF is corrected to 60 megacycles.

(8) *Modulators V8A, V8B, V9A, and V9B.*

(*a*) *General.* Modulators V8A, V8B, V9A, and V9B constitute a 400-cps bridge. A 400-cps signal is applied from the secondary winding of transformer T7 through resistor R35 to the cathodes of V8A and V8B, and through resistor R36 to the cathodes of V9A and V9B. The amplification of this 400-cps signal is determined by conduction in V8A, V8B, V9A, and V9B. Conduction in V8A, V8B, V9A, and V9B is determined by the dc control voltage from V7A and V7B. The control voltage is applied to the grids of V8A and V9B, and is compared to the steady reference voltage applied to the grids of V8B and V9A. When the IF is 60 megacycles, the dc control voltage from V7A and V7B is zero and the bridge is balanced. Equal amplification of the 400-cps signal within the balanced bridge produces a zero 400-cps signal at the plates of V8A and V9A, and V8B and V9B. If the IF deviates from 60 megacycles, a dc control voltage is applied from V7A and V7B to the grids of V8A and V9B. This dc control voltage unbal-

ances the bridge, producing a 400-cps signal at the plates of V8A and V9A, and V8B and V9B. The phase of the 400-cps signal at the plates is determined by the polarity of the dc control voltage. The amplitude of the 400-cps signal at the plates is controlled by the level of the dc control voltage.

(*b*) *Quiescent operation.*

1. When the IF is 60 megacycles, the dc control voltage applied from V7A and V7B to the grids of V8A and V9B is zero. The grids of V8B and V9A are connected to the potential at the brush arm of MOD BAL variable resistor R43. The brush arm of R43 is normally set at a point of zero potential through the voltage divider composed of resistor R42, resistor R43 in parallel with resistors R45 and R44, and resistor R41 connected between the +250 and −250-volt supplies. Voltage is applied to the plates of V8A and V9A through common load resistor R40 connected to the +250-volt supply, and to the plates of V8B and V9B through common load resistor R39 connected to the +250-volt supply. Voltage is applied to the common cathodes of V8A and V8B through resistor R35 and winding 1-2 of T7 connected to the −250-volt supply, and to the common cathodes of V9A and V9B through resistor R36 and winding 2-3 of T7 connected to the 250-volt supply. Since R39 and R40 are of equal resistance, R35 and R36 are of equal resistance, and the potential applied to the grids of V8B and V9A equals the potential applied to the grids of V8A and V9B, the bridge is balanced. The result is equal conduction in V8A, V8B, V9A, and V9B.

2. Simultaneously, 400-cps signals are induced in secondary winding 1-2-3 of T7 by primary winding 5–6.

CONFIDENTIAL

Since the cathodes of V8A, V8B, V9A, and V9B are at opposite ends of the center-tapped secondary of T7, the 400-cps signals applied to the cathodes of V8A and V8B are 180 degrees out of phase with respect to the 400-cps signals applied to the cathodes of V9A and V9B. Since conduction in V8A, V8B, V9A, and V9B is equal, the 400-cps signals receive equal amplification in each section of the bridge. The 400-cps signals at the plates of V8A and V9A are developed across R40. Since these 400-cps signals are 180 degrees out of phase and of equal amplitude,

the addition of the signals produces a zero 400-cps signal at the plates of V8A and V9A (A, fig. 74). The 400-cps signals at the plates of V8B and V9B are developed across R39. Since these 400-cps signals are 180 degrees out of phase and of equal amplitude, the addition of the 400-cps signals produces a zero 400-cps signal at the plates of V8B and V9B (A, fig. 74).

3. During quiescence, the 400-cps bridge should be balanced. However, 400-cps signals could be produced at the plates of V8A and V9A, and V8B and V9B, since no two tubes have ex-
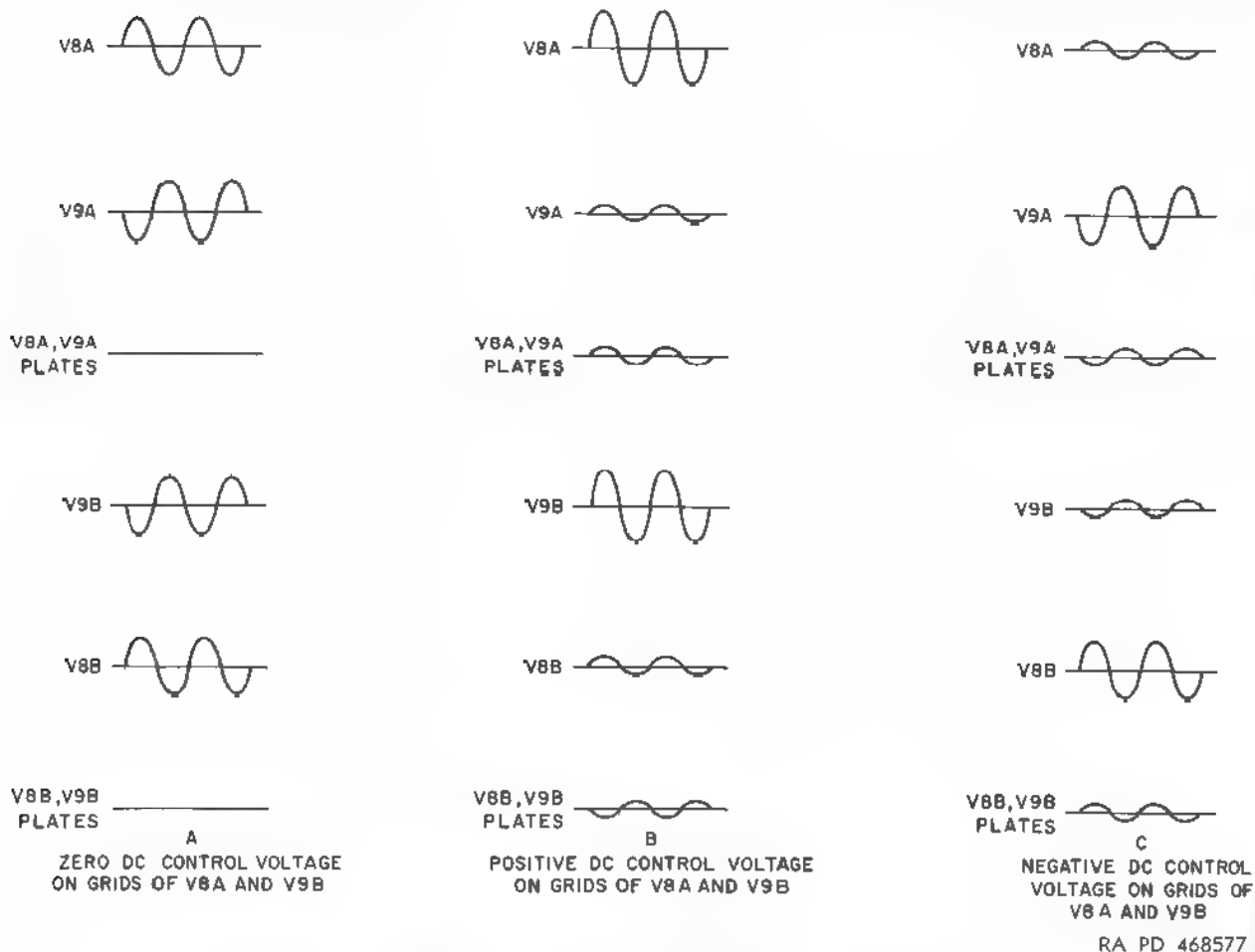
Figure 74. (U) Modulators V8A, V8B, V9A, and V9B—phase relationships.

CONFIDENTIAL

actly the same amplification factor. This is prevented by connecting the grids of V8B and V9A to the brush arm of R43. The voltage at the brush arm of R43 can be varied from 0.5 volt to +0.5 volt. Variable resistor R43 is adjusted for a zero 400-cps signal at the plates of V8A and V9A, and V8B and V9B. During this adjustment, MOD BAL switch S1 (fig. 57, TM 9-1430-257-20) is closed. If the acquisition AFC is in autosearch operation as decribed in (10)(b) below, autosearch signals applied through connector P2-11 are grounded through S1. This assures that no signal is applied to the secondary of T6 when the 400-cps bridge is being balanced.

(c) *Dynamic operation—positive dc control voltage.*

1. A positive dc control voltage applied from V7A and V7B to the grids of V8A and V9B causes increased conduction in V8A and V9B. The increased current in V8A and V9B produces a larger voltage drop across R35 and R36. Since the voltage drop across R35 and R36 determines the bias voltage at the grids of V8B and V9A, grid bias voltage is increased. This reduces conduction in V8B and V9A. Consequently, 400-cps signals at the cathodes of V8A, V8B, V9A, and V9B receive unequal amplification in the bridge.

2. Consider the operation of the bridge with a positive-going, half-cycle, 400-cps signal at the cathodes of V8A and V8B and a negative-going, half-cycle, 400-cps signal at the cathodes of V9A and V9B. Since the amplification obtained from V8A is higher than the amplification obtained from V9A, the positive-going, half-cycle, 400-cps signal at the cathode of V8A is amplified more than the negative-going, half-cycle, 400-cps signal at

the cathode of V9A. The half-cycle 400-cps signals developed across R40 are 180° out of phase and have unequal amplitude. The result is a positive going, half cycle, 400-cps signal at the plates of V8A and V9A (B, fig. 74). Simultaneously, the negative going, half-cycle, 400-cps signal at the cathode of V9B is amplified more than the positive-going, half-cycle, 400 cps signal at the cathode of V8B because of the higher amplification in V9B. The half-cycle, 400-cps signals developed across R39 are 180° out of phase and have unequal amplitudes. The result is a negative going, half-cycle, 400 cps signal at the plates of V8B and V9B (B, fig. 74).

3. During the next half-cycle, a negative going, half-cycle, 400-cps signal is applied to the cathodes of V8A and V8B, and a positive-going, half-cycle, 400 cps signal is applied to the cathodes of V9A and V9B. The 400-cps signals again receive unequal amplification. The result is a negative-going, half-cycle, 400-cps signal at the plates of V8A and V9A, and a positive going, half-cycle, 400-cps signal at the plates of V8B and V9B.

(d) *Dynamic operation—negative dc control voltage.*

1. A negative dc control voltage applied from V7A and V7B to the grids of V8A and V9B causes reduced conduction in V8A and V9B. The reduced current in V8A and V9B produces a smaller voltage drop across R35 and R36. This decreases the bias voltage at the grids of V8B and V9A, increasing conduction in V8B and V9A.

2. Consider the operation of the bridge with the same phase 400-cps signals applied to their common cathodes as in (c)1 above. Because of the higher amplification in V9A, the negative-

going, half-cycle, 400 cps signal at the cathode of V9A receives higher amplification then the positive-going, half-cycle, 400-cps signal at the cathode of V8A. The half-cycle 400-cps signals developed across R40 result in a negative-going, half-cycle, 400-cps signal appearing at the plates of V8A and V9A (C, fig. 74). Simultaneously, the positive-going, half cycle, 400 cps signal at the cathode of V8B receives higher amplification than the negative-going, half-cycle, 400-cps signal at the cathode of V9B because of the higher amplification in V8B. The half-cycle, 400-cps signals developed across R39 result in a positive going, half-cycle, 400-cps signal appearing at the plates of V8B and V9B (C, fig. 74).

3. On the next half-cycle, a negative-going, half-cycle, 400-cps signal is applied to the cathodes of V8A and V8B and a positive-going, half-cycle, 400-cps signal is applied to the cathodes of V9A and V9B. The 400-cps signals again receive unequal amplification. This results in a positive-going, half-cycle, 400-cps signal at the plates of V8A and V9A, and a negative-going, half cycle, 400-cps signal at the plates of V8B and V9B.

(9) *Converters V10A and V10B.*

(a) The 400-cps signals at the plates of V8A and V9A are coupled through capacitor C30 (fig. 57, TM 9-1430-257-20), developed across resistor R58, and applied to the grid of V10A. The 400-cps signals at the plates of V8B and V9B are coupled through capacitor C31, developed across resistor R59, and applied to the grid of V10B. Since the 400-cps signals at the grid of V10A are 180° out of phase with respect to the 400-cps signals at the grid of V10B, the 400-cps signals represent a push-pull input to V10A and V10B. Converters V10A and V10B produce a single-ended 400-cps signal output, the phase of which is determined by the phase of the 400-cps signal input to the grid of V10A. The amplitude of the 400-cps signal output is proportional to the amplitude of the push-pull 400-cps signal input. Push-pull to single-ended conversion is necessary in order to obtain a usable control voltage for operating the AFC motor-generator.

(b) Consider the operation of V10A and V10B when a positive-going, half-cycle, 400-cps signal is applied to the grid of V10A and a negative-going, half-cycle, 400-cps signal is applied to the grid of V10B. The positive-going 400-cps signal at the grid of V10A causes increased conduction, resulting in an increased voltage across common cathode resistor R63. The increased voltage across R63 plus the negative-going 400-cps signal at the grid of V10B cause reduced conduction, resulting in an increased voltage at the plate of V10B. During the next half-cycle, the negative-going 400 cps signal at the grid of V10A causes reduced conduction in V10A, resulting in a decreased voltage across R63. The decreased voltage across R63, and the positive-going 400-cps signal at the grid of V10B cause increased conduction, resulting in a decreased voltage at the plate of V10B. The output signal at the plate of V10B is a single-ended, 400 cps AFC motor-control voltage, having the same phase as the 400-cps signal applied to the grid of V10A. Even though the output is taken from the plate of V10B, V10A is necessary to balance the circuit. The phase shift in V10A and V10B is compensated for by capacitor C33 connected from the plate of V10B to a point of zero potential at the junction of R45 and R44.

(c) The 400-cps AFC motor-control voltage at the plate of V10B is coupled

through capacitor C32 and voltage-dropping resistor R47 to connector P1–1. The AFC motor control voltage is developed across resistors R48 and R49 connected between connectors P1–1 and P1–3 (circuit ground). The junction of R48 and R49 is connected to P1–5. A feedback voltage from the AFC motor-generator is applied through P1–5, and developed across R49. The feedback voltage is 180° out of phase with the AFC motor-control voltage. Therefore, the output voltage applied through P1–1 to the low-power servo amplifier is the resultant voltage produced by the algebraic summation of the AFC motor-control voltage across R48 and R49 and the feedback voltage across R49.

(d) Converters V10A and V10B are designed to give harmonic suppression. If harmonics of the 400-cps signals are present, the signals at the grids of V10A and V10B due to these harmonics may be in phase. The 800-cps second harmonic of the 400-cps signal is the harmonic having the largest amplitude. Therefore, suppression of an 800-cps signal is of primary importance. Since 800-cps signals are an even harmonic output of a push-pull amplifier, the 800-cps signals at the grids of V10A and V10B are in phase. For the purpose of explanation, the 800-cps signals are considered as positive-going at the grids of both V10A and V10B. The positive-going grid of V10A causes increased conduction. The resulting increased voltage across R63 attempts to cause reduced conduction in V10B. However, the positive-going grid of V10B prevents reduced conduction in V10B. Therefore, the net current change in V10B is zero, and no 800-cps signal appears at the plate of V10B. Thus, the 800-cps harmonics have been suppressed.

(10) *Relay amplifiers V11A and V11B.*
  (a) *Normal operation.* When the acquisition local oscillator frequency is 60 ± 5 megacycles above the acquisition magnetron frequency, the 60 ± 5 megacycle IF signals passed by V1, V2, and V3 develop limiter bias voltage at the grid of V4. The limiter bias voltage is applied from V4 through the low pass filter composed of resistor R23 and capacitors C35 and C5 to the grid of V11A, biasing V11A to cutoff. A positive bias voltage is applied to the grid of V11B through the voltage divider composed of plate resistor R53 and resistors R65 and R64 connected between the -250- and $+250$-volt supplies. The positive bias voltage causes V11B to draw grid current, which immediately reduces the grid voltage to zero. The resultant conduction in V11B causes current to flow in the solenoid winding of hunt relay K1. Relay K1 energizes, closing contacts 2 and 3. The center tap of the secondary of T6 is connected through R32 and contacts 3 and 2 of K1 to ground. The AFC motor-generator is controlled by the error pulse output of V5, which operates modulators V8A, V8B, V9A, and V9B.

  (b) *Auto-search operation—general.*
    1. If the acquisition local oscillator frequency is more than 65 megacycles above the acquisition magnetron frequency, the IF signals are outside of the 10-megacycle bandpass centered at 60 megacycles. Therefore, the IF signals are not passed by V1, V2, and V3. Limiter bias voltage is no longer developed at the grid of V4 and applied to the grid of V11A. The absence of limiter bias voltage at the grid causes V11A to conduct, resulting in a reduced voltage at the plate. The reduced voltage at the plate of V11A is applied through the voltage divider composed of R53,

CONFIDENTIAL

R65, and R64 to the grid of V11B, causing V11B to cut off. Current through the winding of K1 stops, causing K1 to deenergize. Contacts 1 and 3 of K1 close, connecting the center tap of T6 through R32 to connector P2–11. A dc auto search signal, which can be either positive or negative, is applied as an artificial detector signal from P2–11 through contacts 1 and 3 of K1 and R32 to the center tap of T6. Modulators V8A, V8B, V9A, and V9B are operated by the auto-search signal applied to T6. This causes the AFC motor-generator to retune the acquistion local oscillator to restore the 60-megacycle IF.

2. Capacitor C34, connected from contact 3 of K1 to ground, is in the circuit only when the acquistion AFC is in auto-search operation (contacts 1 and 3 of K1 closed). Capacitor C34 stabilizes the dc auto search signals applied to the center tap of T6. RELAY AMP ADJ variable resistor R66 in the cathode circuit of V11A controls the operation of K1 by limiting current in V11A. Variable resistor R66 is adjusted to assure that the plate voltage of V11A does not drop enough to cut-off V11B until limiter bias voltage is removed from the grid of V11A.

3. In order to explain auto-search operation, the following three relationships between acquisition local oscillator frequency and acquisition magnetron frequency are presented: local oscillator frequency more than 65 megacycles above the magnetron frequency; local oscillator frequency more than 65 megacycles below the magnetron frequency; and local oscillator frequency less than 55 megacycles above magnetron frequency. In each of these conditions, it is assumed that limiter bias voltage is

removed from the grid of V11A and that K1 is deenergized.

(c) *Local oscillator frequency more than 65 megacycles above magnetron frequency.*

1. The acquisition local oscillator is operating at the high end of its frequency range, more than 65 megacycles above acquisition magnetron frequency (A, fig. 75). Limit switch S13 (fig. 76) mechanically operated by the AFC motor-generator, is normally in the closed position. A potential of −28 volts is applied through S13 to AFC motor reversing relay K3 located in the acquisition RF power supply control. Relay K3 energizes, causing contacts 2 and 3 to close. A +5-volt auto-search signal is developed in the acquisition AFC across the voltage divider composed of resistors R56 and R9 in parallel and resistor R54 connected from ground to the +250-volt supply. Resistor R9 located in the acquisition RF power supply control, is connected from the junction of R54 and R56, through connector P2–9 and contacts 6 and 4 of normally deenergized AFC release relay K2 to ground.

2. The +5-volt auto-search signal is applied through P2–9, contacts 2 and 3 of K3, P2–11, contacts 1 and 3 of K1, and R32 to the center tap of T6. The +5-volt auto-search signal operates V8A, V8B, V9A, and V9B, causing the AFC motor-generator to retune the acquisition local oscillator to a lower frequency, resulting in a lowered IF. When the acquisition local oscillator frequency is 60+5 megacycles above the acquisition magnetron frequency, the IF signals can be passed by V1, V2, and V3. As a result, limiter bias voltage is again developed at the grid of V4 and applied to the grid of V11A. Amplifier

CONFIDENTIAL
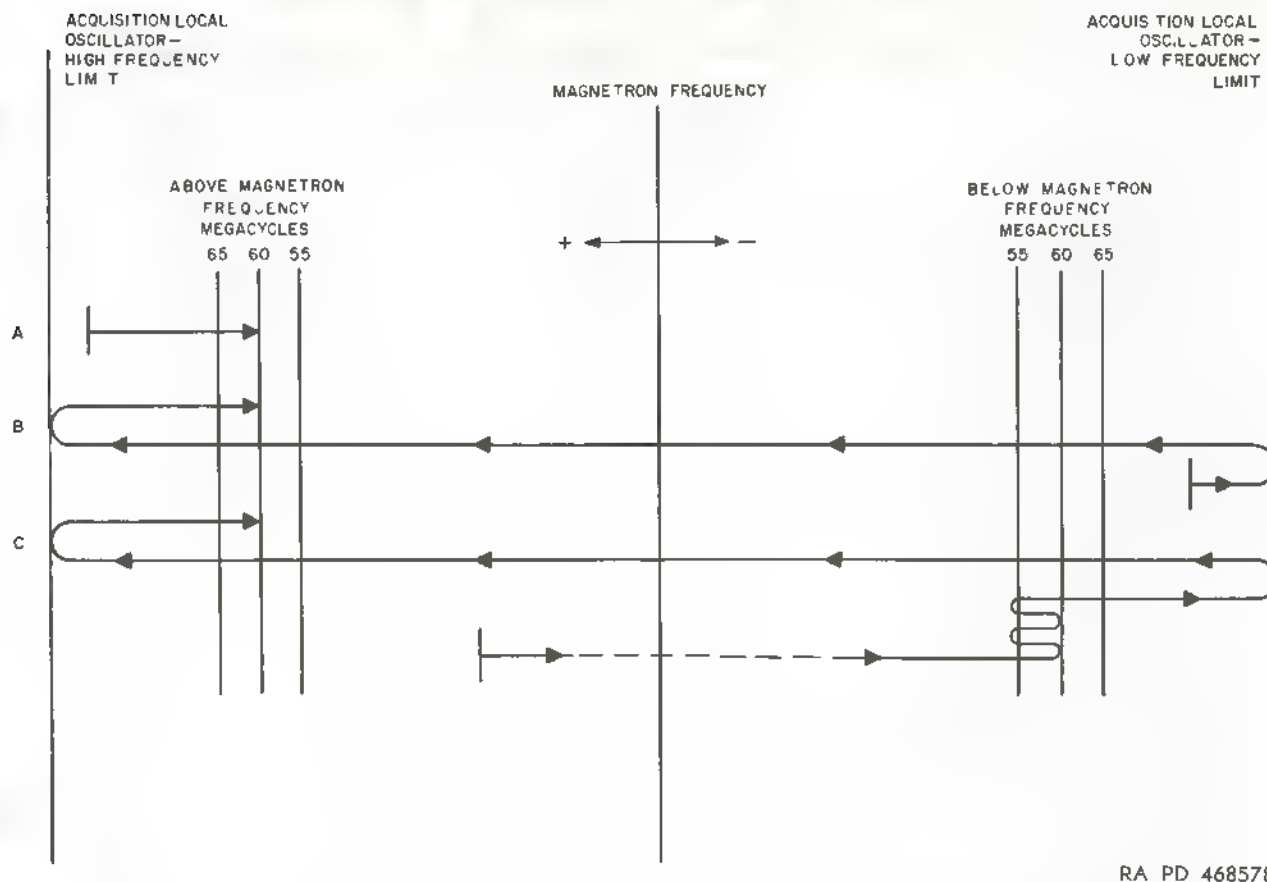
Figure 75. (U) Acquisition AFC auto-search operation.

RA PD 468578

V11A is cut off, causing V11B to conduct and energize K1. Contacts 2 and 3 of K1 close, grounding the center tap of T6. The error pulse output of V5 operates V8A, V8B, V9A, and V9B. Thus, normal AFC operation is resumed.

(d) *Local oscillator frequency more than 65 megacycles below magnetron frequency.*

1. The acquisition local oscillator is operating at the low end of its frequency range, more than 65 megacycles below the acquisition magnetron frequency (B, fig. 75). The +5-volt auto-search signal is applied to the center tap of T6 (fig. 76), causing the AFC motor-generator to retune the acquisition local oscillator to a lower frequency. At the low frequency limit of the acquisition local oscillator tuning range, S13 is mechanically actuated by the AFC motor-generator, removing the −28 volts from K3. Relay K3 deenergizes, causing contacts 3 and 1 to close. A 15-volt auto-search signal is developed in the acquisition AFC across the voltage divider composed of resistors R57 and R55, connected from ground to the 250-volt supply.

2. The −15-volt auto-search signal is applied through connector P2-7, contacts 1 and 3 of K3, P2-11, contacts 1 and 3 of K1, and R32 to the center tap of T6. The 15-volt auto-search signal causes the AFC motor-genera

CONFIDENTIAL
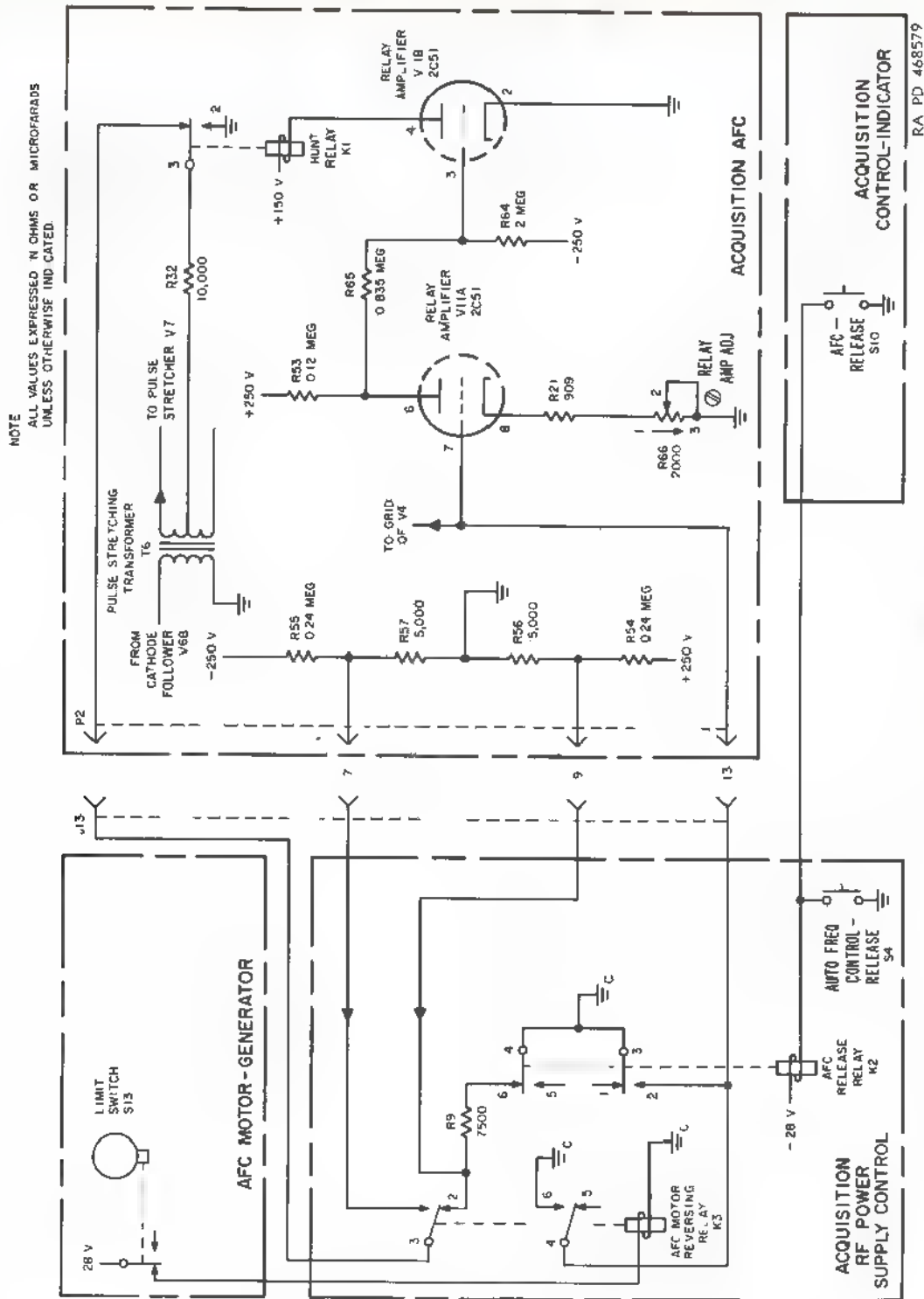
Figure 76. (U) Auto-search circuitry functional schematic diagram.

tor to reverse its direction of rotation, retuning the acquisition local oscillator to the high frequency limit of its tuning range. At the same time, the grid of V11A is grounded through connector P2–13 and contacts 4 and 6 of K3. The grounded grid makes V11A insensitive to limiter bias voltage developed at the grid of V4 when the acquisition local oscillator frequency passes through the sidebands which are ±60 megacycles from the acquisition magnetron frequency. The −15-volt auto-search signal overrides the error pulses produced by V5. This prevents the acquisition local oscillator from locking on the 60-megacycle IF as local oscillator frequency passes through the lower and upper sidebands.

3. When the AFC motor-generator has retuned the acquisition local oscillator to the high frequency limit of its tuning range, S13 is again mechanically actuated by the AFC motor-generator. The −28 volts is again applied through S13 to K3. Relay K3 energizes, causing contacts 3 and 2 to close. The +5-volt auto-search signal at P2–9 is applied through contacts 2 and 3 of K3 and contacts 1 and 3 of K1 to the center tap of T6. Contacts 4 and 6 of K3 open, removing the grid of V11A from ground. The +5-volt auto-search signal causes the AFC motor-generator to reverse its direction of rotation and retune the acquisition local oscillator to a lower frequency. The acquisition local oscillator locks on the 60±5-megacycle upper sideband as described in (c)2 above.

(e) Local oscillator frequency less than 55 megacycles above magnetron frequency.

1. The acquisition AFC is prevented from locking on the upper or lower sidebands during the time the acquisition local oscillator is being tuned from the low to the high frequency limit of its tuning range. However, a condition of the auto-search circuits near the lower 60 ±5-megacycle sideband causes erratic operation of the acquisition local oscillator. This condition occurs when the difference frequency between the acquisition local oscillator frequency and acquisition magnetron frequency is less than +55 megacycles (C, fig. 75).

2. Limiter bias voltage is removed from the grid of V11A (fig. 76), causing V11A to conduct and deenergize K1. The +5-volt auto-search signal is applied to the center tap of T6, causing the AFC motor-generator to retune the acquisition local oscillator to a lower frequency. The grid of V11A is not grounded through K3 at this time, since the acquisition local oscillator is not at the low frequency limit of its tuning range, and the AFC motor-generator has not actuated S13. When the acquisition local oscillator is retuned to a frequency which is 60±5 megacycles below the acquisition magnetron frequency, limiter bias voltage is developed at the grid of V4 and applied to the grid of V11A. The limiter bias voltage cuts off V11A, causing K1 to energize.

3. The acquisition AFC attempts to resume normal operation. However, the polarity of the error pulses developed by V5 at the 60±5-megacycle lower sideband are opposite to the polarity of the error pulses developed by V5 at the 60±5-megacycle upper sideband. The error pulses cause the AFC motor-generator to retune the acquisition local oscillator to a higher frequency. Limiter bias voltage is again removed from the grid of V11A, causing V11A to con-

CONFIDENTIAL

duct and deenergize K1. The +5-volt auto-search signal is again applied to T6, causing the AFC motor-generator to reverse its direction of rotation and retune the acquisition local oscillator to a lower frequency, which again approaches the lower sideband. This hunting by the acquisition local oscillator continues. Hunting is indicated by the flashing of AUTO FREQ. control-hunt indicator light I3 located on the acquisition RF power supply control, and AFC—HUNT indicator light I4 located on the acquisition control-indicator. These two neon indicator lights are operated when the output of the low-power servo amplifier exceeds +40 volts.

4. To correct the hunting action by the acquisition local oscillator and to reestablish normal AFC operation, AUTO FREQ CONTROL-RELEASE switch S4 (located on the acquisition RF power supply control) or AFC—RELEASE switch S10 (located on the acquisition control-indicator) must be operated. Operation of either S4 or S10 applies a ground to K2, causing K2 to energize. Contacts 2 and 3 of K2 close, grounding the grid of V11A through P2-13. Amplifier V11A conducts, causing K1 to deenergize. Since contacts 4 and 6 of K2 are now open, R9 is removed from the voltage divider, leaving only R54 and R56 connected from ground to the +250-volt supply. A +15-volt auto-search signal developed across R54 and R56 is applied through P2-9, contacts 2 and 3 of K3, P2-11, and contacts 1 and 3 of K1 to the center tap of T6. The +15 volt auto-search signal overrides the error pulses produced by V5, causing the AFC motor-generator to retune the acquisition local oscillator to the low frequency limit of its tun-

ing range. From the low frequency limit of the acquisition local oscillator tuning range, the auto-search operation is the same as that described in (c)2 above.

(11) *Miscellaneous components.* The filament circuits of V1 through V5 (fig. 57, TM 9-1430-257 20) are decoupled from the 6.3-volt power supply by the following inductor-capacitor networks: for V1, C25 and L3; for V2, C26 and L4; for V3, C27 and L5; for V4, C28 and L6; for V5, C29 and L7. Capacitor C38 provides decoupling for V6 through V11.

75. Low-Power Servo Amplifier 7614253

This low power servo amplifier is identical to the low-power servo amplifier discussed in paragraph 46.

76. AFC Motor-Generator 7605334

a. General.

(1) The AFC motor generator operates when the IF input to the acquisition receiver deviates from 60 megacycles. At such time, the motor supplies the driving power to retune the acquisition local oscillator and acquisition preselector cavities and readjust repeller plate variable resistor R32 until a 60-megacycle IF is again obtained.

(2) The generator is mounted on the same shaft with the motor. The generator produces a degenerative feedback voltage which is applied to the motor control source (acquisition AFC) to limit the starting torque of the motor and to insure a constant motor speed. The feedback also dampens any oscillations initiated when inertia causes the motor to overshoot the point at which a correct acquisition local oscillator frequency is obtained.

b. Detailed Theory.

(1) *Physical description.*

(a) *Motor.* The motor is of the two-phase induction type, consisting of a rotor and stator (fig. 77). The stator is mounted on the inner periphery of the

202

CONFIDENTIAL

motor-generator housing and is divided into two separate coils. These coils are electrically in quadrature with each other (fig. 78) so that a rotating magnetic field can be set up. The rotor (fig. 77) is a squirrel cage type, with closed loops of heavy wire placed lengthwise along the rotor. The rotor is mechanically connected to a shaft and gear train, to which are attached the acquisition local oscillator and acquisition preselector tuning plungers and the brush arm of repeller plate variable resistor R32.

(b) *Generator.* The generator is a drag-cup type, consisting of a copper cup rotor and a stator. The rotor is mechanically connected to the motor drive mechanism, and the stator is mounted on the inner periphery of the motor-generator housing. The generator stator is divided into two separate coils

which are electrically in quadrature with each other (fig. 78).

(2) *AFC motor-generator excitation.*

(a) *Motor.* Terminal 1 of stator winding 1-2 is connected to the output of the low-power servo amplifier (LPSA); terminal 2 is connected to ground. Terminal 3 of stator winding 3-4 is connected to 120 volts, phase C through contacts 3 and 2 of AFC motor disable relay K4 and AUTO FREQ CONTROL-MOTOR EXC switch S6 (both on the acquisition RF power supply control); terminal 4 is connected to the 120-volt neutral line.

(b) *Generator.* Terminal 7 of stator winding 7-8 is connected to the acquisition AFC; terminal 8 is connected to ground. Terminal 6 of stator winding 5-6 is connected through TACH PHASE ADJ variable resistor R2 to the generator excitation line, which is
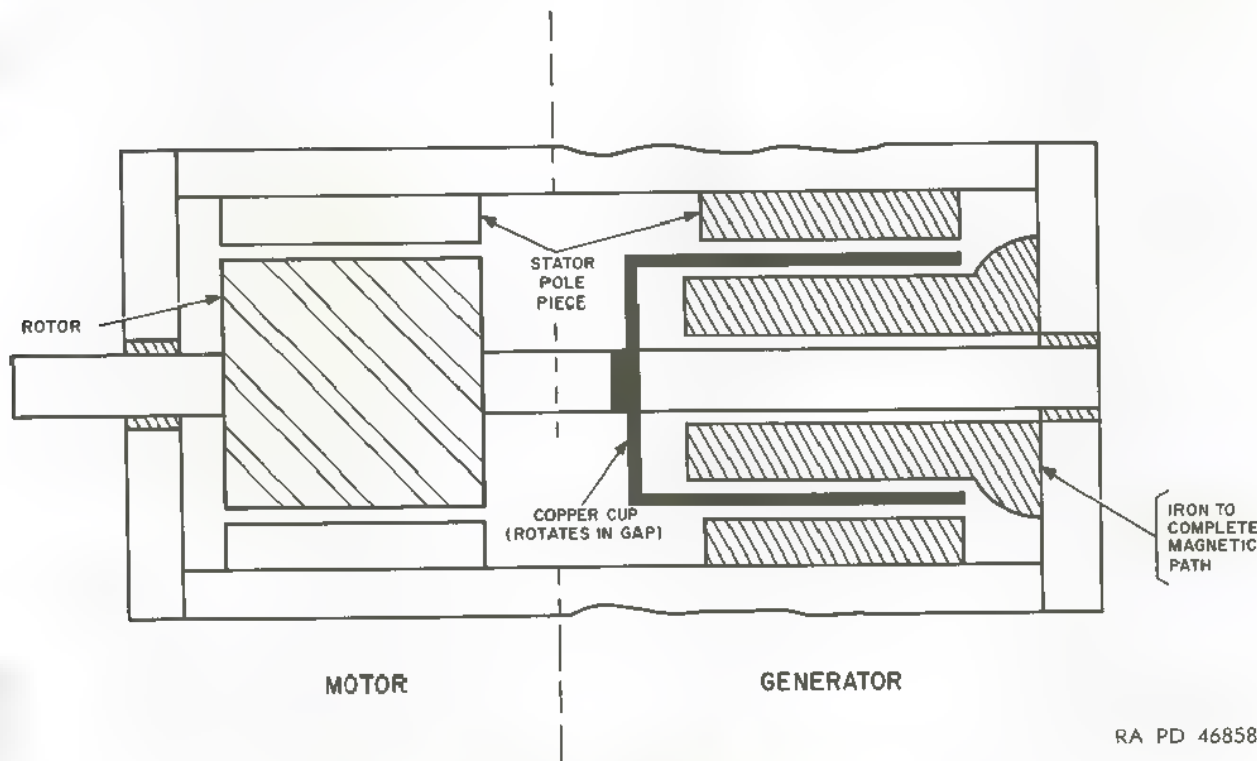
Figure 77. (U) AFC Motor-generator—sectional view.
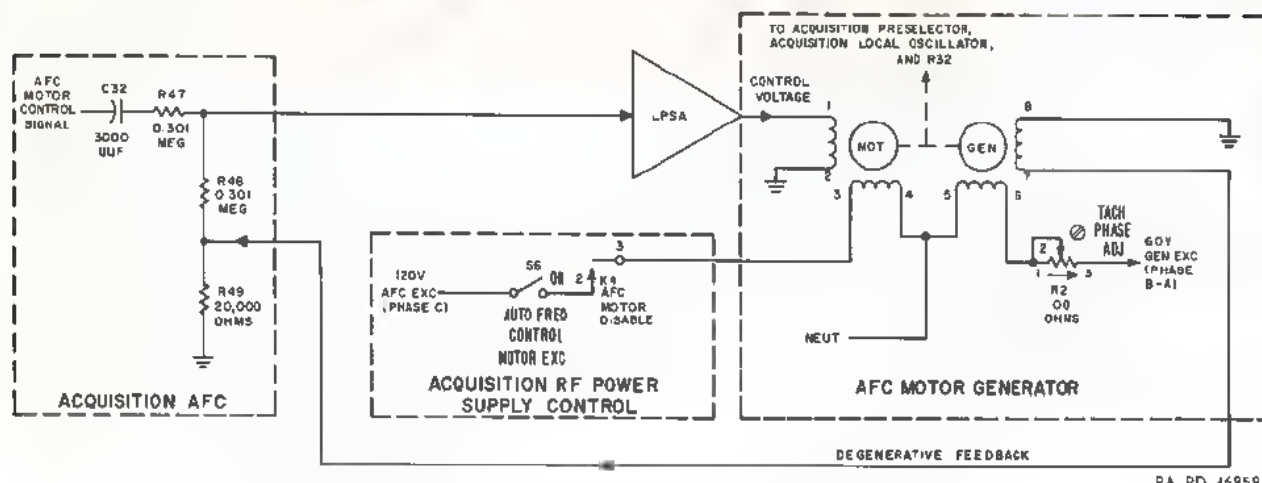
RA PD 468580

Figure 78 (U) AFC Motor-generator—simplified schematic diagram.

phase B–A, 60 volts, 400 cps; terminal 5 is connected to the 120-volt neutral line. Variable resistor R2 compensates for an inherent phase shift between the control voltage and the generator output voltage from stator winding 7–8, thus insuring that these voltages are exactly 180° out of phase.

(3) *Quiescent condition.* When the IF input to the receiver is 60 megacycles, the AFC motor-generator is not activated because there is no control voltage from the LPSA to motor winding 1 2. Consequently, a rotating magnetic field cannot be set up between windings 1–2 and 3–4 since the only voltage present is the 120-volt, 400-cps excitation voltage constantly applied to stator winding 3 4. Without a rotating magnetic field, the motor rotor does not turn, and the shaft and gear tuning mechanism and generator rotor are not driven. Within the generator, 60 volts, 400 cps, is constantly applied to stator winding 5–6. Since a generator produces an output only when its rotor is turned through a magnetic field, there is no voltage feedback to the acquisition AFC.

(4) *Dynamic operation.*

(a) When the IF input to the receiver deviates from 60 megacycles, a 400-cps

control voltage is applied to winding 1 2. The amplitude of this control voltage is determined by the extent of frequency deviation from 60 megacycles. The phase of the control voltage with respect to the 400-cps motor excitation voltage in winding 3–4 is either 90° or 270°, depending upon whether the frequency deviation is above or below the center IF of 60 megacycles. A phase relationship of 90° between the voltages in winding 1–2 and winding 3–4 produces a rotating magnetic field in one direction; a phase relationship of 270° produces a rotating magnetic field in the opposite direction. In either cause, the rotating magnetic field induces a current in the rotor, causing the rotor and drive shaft to turn in the direction of field rotation. Since winding 3–4 is returned to a fixed amplitude 400-cps excitation voltage, the strength of the rotating field is proportional to the amplitude of the control voltage. This causes the torque and speed of the induction motor to be proportional to the amplitude of the control voltage; that is, small control voltage rotates the motor slowly, and a large control voltage rotates it faster.

(*b*) As the drive shaft turns, the generator rotor turns through the magnetic field of winding 5–6. A current induced in the rotor produces a small magnetic field at right angles to the magnetic field set up by winding 5–6. The algebraic addition of the two fields produces a resultant field that is parallel to winding 7–8. This induces a 400-cps voltage in winding 7–8; this voltage is developed across resistor R49 in the acquisition AFC. The greater the motor speed, the larger the magnetic field set up by the generator rotor. This increases the resultant magnetic field that is parallel to winding 7–8, resulting in a greater amplitude of feedback voltage. Stator winding 7–8 is connected so that the feedback voltage to the acquisition AFC is 180° out of phase with the control voltage. Therefore, the feedback voltage is degenerative and constantly opposes the control voltage.

(*c*) Consider AFC motor-generator operation with the system at rest, and a 1-volt AFC motor control signal suddenly applied from the acquisition AFC to the LPSA. The LPSA has a gain of 50,000 and the minimum input signal amplitude required for saturation is 0.002 volt. The 1-volt AFC motor control signal quickly drives the LPSA into saturation and a maximum ampiltude control voltage of 100 volts is applied to winding 1–2. The large amplitude control voltage causes a strong rotating field to be set up, and the rotor and drive shaft attempt to respond to the large control voltage. The sudden initial shaft twist induces almost 1 volt of feedback voltage in winding 7–8. This voltage is developed across R49 in the acquisition AFC. Since the 1-volt AFC motor control signal develops a voltage across R48 and R49, the input to the LPSA is the algebraic sum of the two opposite polarity voltages. This summation results in almost complete cancellation of the control voltage. The cancellation continues until the level of the AFC motor control voltage to the LPSA produces sufficient control voltage to winding 1–2 for a constant motor speed versus feedback voltage. When this occurs, the steady-state voltages could be: AFC motor control signal, 1 volt; generator output, 0.999 volt; LPSA input, 0.001 volt; and control voltage, 50 volts. With these conditions, the motor rotates at approximately one-half of its maximum speed.

(*d*) If the AFC motor control signal suddenly increases to 2 volts, the input voltage to the LPSA would rise to 1.001 volts. The level of this signal quickly saturates the LPSA, producing a maximum control voltage of 100 volts to winding 1–2. A rotating magnetic field of maximum strength is set up, and the greatly increased shaft torque causes approximately 1.998 volts to be induced in generator winding 7–8. Again, this voltage is developed across R49. The 2-volt AFC motor control signal and 1.998-volt feedback signal produce 0.002 volt at the input to the LPSA. Since this voltage produces maximum control voltage output from the LPSA, the motor runs at full speed. The steady-state voltages are: AFC motor control signal, 2 volts; generator output voltage, 1.998 volts; LPSA input, 0.002 volt; and control voltage, approximately 100 volts.

(*e*) If the AFC motor control signal suddenly decreases to 1.996 volts, the motor would continue to run at full speed for an instant, producing 1.998 volts of feedback voltage across R49. The algebraic sum of the opposite polarity voltages across R48 and R49 produces a 0.002-volt input to the LPSA, but of opposite polarity. This results in

CONFIDENTIAL

maximum control voltage to the motor and causes full deceleration of the motor.

77. Acquisition RF Power Supply Control
8158120, 9000009-

a. General. The acquisition RF power supply control (fig. 58, TM 9–1430–257 20) consists of a regulated 800-volt power supply, voltage and current monitoring circuits, and voltage control circuits. The unit functions are listed in (1) through (10) below.

(1) Supplies keep-alive voltage for the acquisition receiver transmitter TR tube.

(2) Supplies operating voltages for the traveling wave tube in the magnetic circuit.

(3) Provides monitoring critical currents in the traveling wave-tube in the magnetic circuit.

(4) Supplies local oscillator repeller plate voltage.

(5) Provides monitoring of critical voltages and currents applied to various units of the acquisition antenna-receiver transmitter group.

(6) Provides local control of IF preamplifier gain.

(7) Provides local control of the noise generator.

(8) Provides local control of magnetron frequency.

(9) Provides local control of AFC motor excitation.

(10) Provides facilities for local monitoring of the acquisition transmitter sync pulse and IFF video pulse.

Note The key letter number combinations shown in parentheses in *b* below refer to figure 58, TM 9-1430–257–20 unless otherwise indicated.

b. Detailed Theory.

(1) *Rectifier V1.* A single-phase, 120-volt, 400 cps input is applied through connectors J1–E and J1–M (A2) to the primaries of transformers T1 and T2. Stepped-up voltage induced in the secondary of T1 is applied to the plates of rectifier V1. Alternate conduction of each plate produces full-wave rectification of the secondary voltage of T1. The rectifier output of V1 is smoothed and filtered through the pi-network consisting of capacitor C1, inductor L1, and capacitor C2. Voltage adjust variable resistor R4 is adjusted to provide −800 volts with respect to ground at connector J2-A as ionization voltage for the acquisition receiver transmitter TR tube. Filament voltage for V1 is obtained from secondary winding 3–5 of T2. Resistors R1 and R2, in parallel, drop filament voltage to the value required for operation of V1.

(2) *Voltage regulators V2 through V8.* The 800-volt output of V1 is divided across 75 volt regulator V2 (A7), 105-volt regulator V3, 150 volt regulators V4 and V5, and 108 volt regulators V6, V7, and V8. The R. F AMPLIFIER VOLTAGE CONTROLS and current divider resistors R10 through R19 are connected as part of the regulated voltage divider network.

(3) *Filament supply.* Transformers T2 and T3 (B3) supply filament voltages to various units of the acquisition antenna-receiver-transmitter group. The primary of T3 is energized by a single-phase, 120-volt, 400-cps input applied through connectors J1–E and J1 K.

(a) Secondary winding 6–7 of T2 furnishes filament power through connectors J2–X and J2–Z to the traveling wave tube in the magnetic circuit.

(b) Secondary winding 10–11 of T2 furnishes filament power through connectors J1 R and J1–S to the local oscillator.

(c) Secondary winding 5–7 of T3 furnishes filament power through connectors J1–H and J1–J to the acquisition IF preamplifier and low power servo amplifier.

(d) Secondary winding 3 4 of T3 furnishes filament power through connectors J1–T and J1–U to the acquisition AFC.

CONFIDENTIAL

(4) *RF amplifier voltage controls.* The negative voltage at the junction of V2 and V3 (725 volts) is applied through connector J2-B to the cathode of the traveling wave tube in the magnetic circuit Control of traveling wave tube electrode voltages (par. 68) and their amplitudes with respect to cathode voltage is exercised by R. F AMPLIFIER VOLTAGE CONTROLS variable resistors.

(a) R. F. AMPLIFIER VOLTAGE CONTROLS—G1 variable resistor R11 (A8) furnishes 0 to 75 volts through connector J2-D to the beam-forming electrode.

(b) R. F. AMPLIFIER VOLTAGE CONTROLS—G2 variable resistor R14 (B9) furnishes 0 to +105 volts through connector J2-E to anode 1.

(c) R. F. AMPLIFIER VOLTAGE CONTROLS—G3 variable resistor R13 (B8) furnishes 0 to +105 volts through connector J2-F to anode 2.

(d) R. F. AMPLIFIER VOLTAGE CONTROLS G4 variable resistor R16 (C7) furnishes +105 to +405 volts through connector J2-G to anode 3.

(e) R. F. AMPLIFIER VOLTAGE CONTROLS—HELIX variable resistor R18 (C7) furnishes +405 to +621 volts through connector J2-H to the helix electrode. Helix current is monitored by R. F. AMPLIFIER HELIX CURRENT meter M2 (C11).

(f) COLLECTOR variable resistor R19 (C7) furnishes +513 to +729 volts through connector J2-J to the collector electrode. Collector current is monitored by R. F. AMPLIFIER COLLECTOR CURRENT meter M3 (C11).

(5) *Local oscillator controls.*

(a) Acquisition local oscillator repeller plate voltage is obtained and controlled from a complex voltage divider. The voltage divider components are fixed resistors R20 (B9), R22, R23, and voltage regulators V9 and V10. Variable resistors associated with the voltage divider are LOCAL OSC CONTROLS—LEVEL variable resistor R21A and R21B and LOCAL OSC CONTROLS—SPREAD variable resistors R24A and R24B. Voltage at the junction of the plate of V3 and the cathode of V4 (−625 volts) is applied through R20, R21A, 108-volt regulator V10, R21B, and 75-volt regulator V9 to the junction of the plate of V5 and the cathode of V6. Cathode voltage of V10 is applied through R22 and R24A to connector J2-K. Plate voltage of V10 is applied through R23 and R24B to connector J2-O. Voltage at the junction of the plate of V5 (C7) and the cathode of V6 (−325 volts) is applied through connector J2-L to the local oscillator cathode.

(b) When R21A is adjusted to zero resistance, R21B is set at maximum resistance. Under these conditions, cathode voltage of V10 is −591.5 volts and plate voltage is −483.5 volts with respect to ground. With R21A adjusted to maximum resistance, R21B is set at zero resistance. These conditions apply −508 volts to the cathode of V10 and −400 volts with respect to ground at the plate. The normal midresistance setting of R21A and R21B produces 529 volts at the cathode of V10 with respect to ground and 421 volts at the plate. Thus, the voltage level across V10 is adjustable within the range of −508 to −591.5 volts with respect to ground at the cathode and −400 to −483.5 volts with respect to ground at the plate. Regulator action of V10 maintains a 108-volt potential difference between the plate and cathode within these ranges.

(c) When R24A and R24B are adjusted to maximum resistance, a minimum output voltage spread is obtained across J2-K and J2-O. With R24A and

CONFIDENTIAL

R24B adjusted to zero resistance, a maximum output voltage spread is obtained across J2-K and J2-O. The normal setting of R24A and R24B produces an output voltage spread across J2-K and J2-O of 100 volts. Under this condition, the voltage at J2 O is − 100 volts with respect to local oscillator cathode voltage, and the voltage at J2-K is 200 volts with respect to local oscillator cathode voltage. Therefore, local oscillator repeller plate voltage is adjustable within the range of − 425 volts to −525 volts with respect to ground.

(6) *NOISE GEN EXC switch S1.* The receiver noise generator is locally energized by operation of NOISE GEN EXC switch S1. Noise generator excitation voltage is applied through connector J1-N and S1 to connector J1-V. When the noise generator is excited, NOISE GEN ON indicator light I2 is illuminated by voltage applied to connector J1-X. Remote operation of the noise generator (par. 67) is controlled by the NOISE GEN switch located on the acquisition control-indicator. The external NOISE GEN switch energizes HV on relay K1 through connector J2-W. With K1 energized, noise generator excitation voltage is applied through relay contacts 2–3 and 4–5 to J1-V. NOISE GEN -HV ON indicator light I1 illuminates when K1 is energized, indicating remote operation of the receiver noise generator.

(7) *MAG FREQ switch S2.* Acquisition magnetron frequency may be locally changed by means of MAG FREQ switch S2. Operation of S2 supplies single-phase, 120-volt, 400-cps excitation to the acquisition magnetron tuning drive motor (par. 64). With S2 placed in the RAISE position, excitation is applied through J1-K, contacts 1–2 of S2, and motor start capacitors C3A and C4 in parallel to connector J1-f, and through

contacts 4–5 of S2 to connector J1-D. With S2 placed in the LOWER position, excitation is applied through J1-K and contacts 8–9 of S2 to J1 D, and through J1-E, contacts 11 12 of S2, C3A and C4 in parallel, to J1-f. With S2 in the normal or midposition, no excitation is applied to the magnetron tuning drive motor.

(8) *IF GAIN switch S3.* The voltage divider, consisting of resistors R7, R41, and IF GAIN knob R8, develops a negative voltage for local control of the acquisition IF preamplifier gain (par. 72). With IF GAIN switch S3 placed in the LOCAL position, variable resistor R8 provides a variable negative voltage applied through contacts 2–3 of S3 and connector J2-S to the acquisition IF preamplifier. With S3 placed in the NORM position, IF preamplifier gain is controlled by a negative voltage developed in the STC control located in the acquisition control-indicator. This voltage is applied through connector J2-T, contacts 1–2 of S3, and J2-S to the IF preamplifier. Contacts 4–5 of S3 are discussed in (11)(k) below.

(9) *AUTO FREQ CONTROL—RELEASE switch S4.* Should the local oscillator lock onto the lower sideband frequency (where local oscillator and magnetron frequencies differ by less than 55 megacycles), the receiver tuning motor will begin to hunt (par. 74). Hunting causes AUTO FREQ control-hunt indicator light I3 to flash. The output of the AFC low-power servo amplifier is applied through connector J1-g and resistor R6 to I3 and through resistor R5 and connector J1-B to the AFC—HUNT indicator light on the acquisition control-indicator. Operation of AUTO FREQ CONTROL—RELEASE switch S4 permits the AFC to sweep, causing the local oscillator to shift to the correct operating frequency. With S4 depressed, AFC release relay K2 is energized, removing

CONFIDENTIAL

resistor R9 from the AFC control circuit Operation of AFC motor reversing relay K3, controlled by a cam-operated switch mounted on the AFC motor shaft, determines the direction of rotation of the motor.

(10) *AUTO FREQ CONTROL—MOTOR EXC switch S6.* A 120-volt 400-cps excitation voltage is applied through connector J1-A, AUTO FREQ CONTROL—MOTOR EXC switch S6, contacts 2-3 of AFC motor disable relay K4, and connector J1-h to the AFC motor-generator Relay K4 is energized when the acquisition magnetron is firing. When the magnetron is not firing, K4 is deenergized, disabling the AFC motor-generator. The AFC motor-generator excitation voltage is removed when either S6 or the AFC switch on the acquisition control-indicator is in OFF position.

(11) *TEST 2 switch S7.* Operation of TEST 2 switch S7 connects TEST 2 meter M4 to monitor critical circuits of the acquisition antenna-receiver-transmitter group.

(a) In G1 VOLTS—F S. 100V POSITION 1, the output of R11 is applied through multiplier resistor R25 and M4 to the junction of V2 and V3.

(b) In G2 VOLTS—F. S. 100V POSITION 2, the output of R14 is applied through M4 and multiplier resistor R26 to the junction of V2 and V3.

(c) In G3 VOLTS—F S. 100V POSITION 3, the output of R13 is applied through M4 and R26 to the junction of V2 and V3.

(d) In G4 VOLTS—F. S. 1000V POSITION 4, the output of R16 is applied through M4 and multiplier resistor R27 to the junction of V2 and V3.

(e) In HEL VOLTS—F. S. 1000V POSITION 5, the output of R18 is applied through M4 and R27 to the junction of V2 and V3.

(f) In COLL VOLTS—F. S. 1000V POSITION 6, the output of R19 is applied through M4 and R27 to the junction of V2 and V3.

(g) In L-O VOLTS (625)—F. S. 1000V POSITION 7, the voltage at the junction of V3 and V4 is applied through multiplier resistor R28 and M4 to ground

(h) In AFC LIM CURR F. S. 100 UA POSITION 8, AFC limiter current developed in the acquisition AFC unit is applied through connector J2-R to meter shunt resistor R30 in parallel with M4.

(i) In AFC XTAL CURR—F. S. 2.5 MA POSITION 9, AFC XTAL current developed in the acquisition AFC unit is applied through connector J2-P to meter shunt resistor R29 in parallel with M4 to ground.

(j) In SIG XTAL CURR—F S. 2.5 MA POSITION 10, signal crystal current developed in the acquisition IF preamplifier is applied through connector J3-J to meter shunt resistor R31 in parallel with M4 to ground.

(k) In REC NOISE TEST—F. S. 100 POSITION 11, the receiver noise output developed in the switching and mixer unit located in the director station group is applied through connectors J3-K and J3-L to M4. When S3 is in the NORM position and S7 is in position 11, M4 is shorted through contacts 4-5 of S3.

(12) *TEST 1 switch 8.* Operation of TEST 1 switch S8 connects TEST 1 meter M5 to monitor magnetron current and power supply voltages in the acquisition antenna-receiver-transmitter group.

(a) In AVE MAG CURR—F. S. 50 MA POSITION 1, magnetron current is applied through J2-N, K4 and resistor R33 in parallel, and the series combination of multiplier resistor R35 and M5 in parallel with meter shunt resistor R34 to ground. Magnetron current is also applied through resistor R32 and connector J1-M to the MAGNETRON

meter on the acquisition control-indicator.

(b) In +150V SUPPLY—F. S. 500V POSITION 2, the +150-volt supply is applied through multiplier resistors R36 and R35 and M5 to ground.

(c) In +250V SUPPLY—F. S. 500V POSITION 3, the +250-volt supply is applied through multiplier resistors R37 and R35 and M5 to ground.

(d) In —250V SUPPLY—F. S. 500V POSITION 4, the —250-volt supply is applied through multiplier resistors R40 and R35 and M5 to ground.

(e) In +270V SUPPLY—F. S. 500V POSITION 5, the +270-volt supply is applied through multiplier resistors R38 and R35 and M5 to +270V (GND).

(f) In +320V SUPPLY—F. S. 500V POSITION 6, the +320-volt supply is applied through multiplier resistors R39 and R35 and M5 to ground.

(13) *SYNC connector J5 and VIDEO connector J6.* The acquisition transmitter sync pulse, developed in the acquisition-track synchronizer located in the director station group, is applied to connector J3-H and is available for monitoring at SYNC connector J5. IFF video is applied to connector J3-B and is available for monitoring at **VIDEO** connector J6. Two 120-volt, 400-cps convenience outlets, J4A and J4B, provide power for external test equipment.

c. Acquisition RF Power Supply Control 8158120. Beginning with system 1146, acquisition RF power supply control 8158120 replaces acquisition RF power supply control 9000009. In acquisition RF power supply control 8158210, an adjustable bias supply consisting of transformer T4, diode CR1, resistors R42, R43, R44, and capacitor C5 is added to correct an error in the noise figure readings. The primary of transformer T4 is energized by a single phase, 120-volt, 400-cps input. The voltage induced in the secondary of T4 is then applied to diode CR1. The rectified output of CR1 is applied to filter circuit R42 and C5 and the dc output of this circuit is applied to voltage divider resistors R43 and R44. A bias voltage is then tapped off METER ZERO variable resistor R44 and is used to neutralize the detector contact potential, permitting a correct noise reading to be obtained.

78 (U). Miscellaneous Cabinet-Mounted Components of Acquisition Receiver-Transmitter 8515397

a. General. This paragraph briefly describes the function of the miscellaneous cabinet-mounted components of the acquisition receiver-transmitter.

Note. The key letter-number combinations shown in parentheses in *b* below refer to figure 55. TM 9-1430-257-20 unless otherwise indicated.

b. Detailed Theory.

(1) *Filter networks for acquisition AFC.* The ac power supply, dc power supply, crystal current, and limiter current connections to the acquisition AFC are decoupled from the 60-megacycle signals by filter networks (D10). Resistor R15 and capacitor C10A decouple at AFC crystal current connector J14-6 Resistor R17 and capacitor C10B decouple at AFC limiter current connector J14-4. Resistor R21 and capacitor C11A decouple at —250-volt power supply connector J14-2. Resistor R19 and capacitor C11B decouple at +150-volt power supply connector J14-7. Resistor R23 and capacitor C12A decouple at +250-volt power supply connector J14-8.

(2) *INTLK switch S1 and interlock switch S3.* INTLK switch S1 (D4) is mounted flush with the cover of the acquisition receiver-transmitter. Interlock switch S3 is mounted flush with the cover of the magnetron hot box. When closed, these switches complete part of the ground path which is applied to terminal 2 of end relay K1 located on the 20-30-second delay timer. This permits high voltage to be applied to the acquisition receiver-transmitter. When the covers associated with either of these switches are opened, the switches open and high voltage is removed from the acquisition receiver-transmitter. This protects maintenance personnel from possible injury due to electric shock.

(3) *Inductor L1 and TACH PHASE ADJ variable resistor R2.* Inductor L1 (B5) is discussed in paragraph 64b(2)(a) and TACH PHASE ADJ variable resistor R2 (C9) is discussed in paragraph 76b(2)(b).

78.1 (U). Acquisition RF Power Supply Control 9156017

a. General. The acquisition RF power supply control (fig. 58.1, TM 9-1430-257-20) consists of a regulated —800-volt power supply, voltage and current monitoring circuits, voltage control circuits, and miscellaneous switching circuits. The unit functions are listed in (1) through (10) below.

(1) Supplies keep-alive voltage for the acquisition receiver transmitter TR tube.

(2) Supplies operating voltages for the traveling wave-tubes in the magnetic circuits.

(3) Provides monitoring for critical currents in the traveling wave-tubes in the magnetic circuits.

(4) Supplies repeller plate voltage for the local oscillator.

(5) Provides monitoring for critical voltages and currents applied to various units of the acquisition antenna-receiver-transmitter group.

(6) Provides local control of IF preamplifier gain.

(7) Provides local control of the noise generators.

(8) Provides local control of magnetron frequency.

(9) Provides local control of AFC motor excitation.

(10) Provides facilities for local monitoring of the acquisition transmitter sync pulse and IFF video pulse.

b. Detailed Theory. The detailed theory of acquisition RF power supply control 9156017 (fig. 58.1, TM 9-1430-257-20) is essentially the same as the theory of acquisition RF power supply control 8158120 or 9000009 discussed in paragraph 77 except for the added variable resistors, meters, and switches used to monitor identical circuits in the added magnetic circuit for the auxiliary receiver channel and switching circuits for the auxiliary noise generator.

78.2 (U). Receiver-Transmitter Subassembly 9156632

Receiver-transmitter subassembly 9156632 (fig. 58.1, TM 9-1430-257-20) consists of preselector cavities 9990523 and 9990524, AFC motor generator 7605334, and the acquisition local oscillator 7599343.

78.3 (U). Auxiliary Frequency Converter 9990516

The operation of auxiliary frequency converter 9990516 is identical to that discussed in paragraph 73. The output is used in the auxiliary IF channel and is applied to the input of the auxiliary IF amplifier 9156573.

78.4 (U). Main Frequency Converter 9989320

The operation of main frequency converter 9989320 is identical to that discussed in paragraph 70.

78.5 (U). Acquisition AFC 9156541

a. General. Acquisition AFC 9156541 performs the same function as acquisition AFC 9143030 discussed in paragraph 74 except for the differences discussed in *b* below.

b. Detailed Theory. The theory of operation of acquisition AFC 9156541 (fig. 57.1, TM 9-1430-257-20) is similar to the theory of operation of acquisition AFC 9143030 discussed in paragraph 74 except for paragraph 57*b*(10) which is replaced by (1) *(a)* through *(e)* below.

Note. All components below are referenced to figure 57.1 TM 9-1430-257-20 unless otherwise indicated.

(1) *Relay amplifiers V11A and V11B.*

(a) Normal operation. When the acquisition local oscillator frequency is 60 ±5 megacycles above the acquisition magnetron frequency, the 60 ±5-megacycles IF signals passed by V1, V2, and V3 develop limiter bias voltage at the grid of V4. The limiter bias voltage is applied from V4 through the low pass filter composed of resistor R23 and capacitors C35 and C5 to the grid of V11A, biasing V11A to cutoff. A positive bias voltage is applied to the grid of V11B through the voltage divider composed of plate resistor R53 and resistors R65 and R64 connected between the —250- and +250-volt supplies. The positive bias voltage causes V11B to draw grid current, which reduces the grid voltage to

zero and induces plate current through V11B and the solenoid winding of hunt relay K1. Relay K1 energizes, closing contacts 2 and 3. This disconnects the hunt signal at P2-11, and bypasses C34 in the signal out circuit of V10 B to ground. The AFC motor-generator is controlled by the error pulse output of V5, which operates modulators V8A, V8B, V9A, and V9B.

(b) *Auto-search operation—general.*

1. If the acquisition local oscillator frequency is more than 65 megacycles above the acquisition magnetron frequency, the IF signals are outside of the 10-megacycles bandpass; are not passed by V1, V2, and V3. Limiter bias voltage is no longer developed at the grid of V4 and applied to the grid of V11A. The absence of limiter bias voltage at the grid causes V11A to conduct, resulting in a reduced plate voltage which is then applied through the voltage divider composed of R53, R65, and R64 to the grid of V11B, causing V11B to cut off. Current through the winding of K1 stops, causing K1 to deenergize. An ac auto-search signal, which can be either in or out of phase with V10B output is applied as an artificial drive voltage from P2-11 through contacts 1 and 3 of K1 and R70 to P1-1, where it is summed with the signal output. Modulators V8A, V8B, V9A, and V9B are operated by the detector V5 dc volts output generated by the frequency deviation, causing the AFC motor-generator to retune the acquisition local oscillator to restore the 60-megacycle IF.

2. Capacitor C34, connected from contact 3 of K1 to ground, is in the circuit only when the acquisition AFC is in auto-search operation (contacts 1 and 3 of K1 closed), and functions as a transi-

ent noise filter. RELAY AMP ADJ variable resistor R66 in the cathode circuit of V11A controls the operation of K1 by limiting current in V11A. Variable resistor R66 is adjusted to assure that the plate voltage drop of V11A does not cut-off V11B until limiter bias voltage is removed from the grid of V11A.

3. In order to explain auto-search operation, the following three relationships between acquisition local oscillator frequency and acquisition magnetron frequency are presented: local oscillator frequency more than 65 megacycles above the magnetron frequency; local oscillator frequency more than 65 megacycles below the magnetron frequency; and local oscillator frequency less than 55 megacycles above magnetron frequency. In each of these conditions, it is assumed that limiter bias voltage is removed from the grid of V11A and that K1 is deenergized.

(c) *Local oscillator frequency more than 65 megacycles above magnetron frequency.*

1. The acquisition local oscillator is operating at the high end of its frequency range, more than 65 megacycles above magnetron frequency (A, fig. 75). Limit switch S13 (fig. 76.1), mechanically operated by the AFC motor-generator, is normally in the closed position, applying a potential of —28 volts through S13 to AFC motor reversing relay K3 located in the acquisition RF power supply control. Relay K3 energizes, causing contacts 2 and 3 to close. An ac auto-search signal is developed in the acquisition AFC across the voltage divider composed of resistors R56 and R9, located in the acquisition RF power supply control, in parallel and resistor R54, connected from

ground to terminal 3 of transformer T8. Resistor R9 is connected from the junction of R54 and R56, through connector P2-9 and contacts 6 and 4 of normally deenergized AFC release relay K2 to ground.

2. The ac auto-search signal is applied through P2-9, contacts 2 and 3 of K3, P2-11, contacts 1 and 3, of K1, R70, and P1-1 to the AFC motor-generator, which retunes the local oscillator to a lower frequency, resulting in a lowered IF. When the local oscillator frequency is 60 +5 megacycles above the magnetron frequency, the IF signals can be passed by V1, V2, and V3. As a result, limiter bias voltage is again developed at the grid of V4 and applied to the grid of V11A. Amplifier V11A is cut off, causing V11B to conduct and energize K1. Contacts 2 and 3 of K1 close, removing the drive voltage from P1-1.

(d) *Local oscillator frequency more than 65 megacycles below magnetron frequency.*

1. The acquisition local oscillator is operating at the low end of its frequency range, more than 65 megacycles below the acquisition magnetron frequency (B, fig. 75). The ac auto-search voltage is applied to P1-1 (fig. 76.1), causing the AFC motor-generator to retune the acquisition local oscillator to a lower frequency. At the low frequency limit of the acquisition local oscillator tuning range, S13 is mechanically actuated by the AFC motor-generator, removing the −28 volts from K3. Relay K3 deenergizes, causing contacts 3 and 1 to close. An ac auto-search signal is developed in the acquisition AFC across the voltage divider composed of resistors R57 and R55, connected from ground to terminal 1 of T8.

2. This ac auto-search signal is shifted 180 degrees in phase from the ac signal which is developed across the divider composed of R54 and R56 because the center tap of T8 is grounded. The ac auto-search signal is applied through connector P2-7, contacts 1 and 3 of K3, P2-11, contacts 1 and 3 of K1, R70, and connector P1-1 to the AFC motor-generator, which retunes the local oscillator to the high frequency limit of its tuning range. The phase shift of 180 degrees in the ac auto-search signal causes the motor to reverse direction of rotation when K3 operates. At the same time, the grid of V11A is grounded through connector P2-8 and contacts 4 and 6 of K3. The grounded grid makes V11A insensitive to limiter bias voltage developed at the grid of V4 when the acquisition local oscillator passes through the sidebands which are ±60 megacycles from the acquisition magnetron frequency. The ac auto-search signal overrides any error pulses produced by V5. This prevents the acquisition local oscillator from locking on the 60-megacycle IF as the local oscillator frequency passes through the lower and upper sidebands.

3. When the AFC motor-generator has retuned the acquisition local oscillator to the high frequency limit of its tuning range, S13 is again mechanically actuated by the AFC motor-generator and −28 volts is again applied through S13 to K3. Relay K3 energizes, causing contacts 3 and 2 to close. The ac auto-search signal at P2-9 is applied through contacts 2 and 3 of K3 and contacts 1 and 3 of K1 to P1-1, reversing the direction of rotation of the motor-generator. Contacts 4 and 6 of K3 opens, disconnecting ground from

the grid of V11A. The ac auto-search signal causes the AFC motor-generator to retune the acquisition local oscillator to a lower frequency. The acquisition local oscillator locks on the 60 ±5-megacycle upper sideband as described in (2) above.

(e) Local oscillator frequency less than 55 megacycles above magnetron frequency.

1. The acquisition AFC is prevented from locking on the upper or lower sidebands during the time the acquisition local oscillator is being tuned from the low to the high frequency limit of its tuning range. However, a condition of the auto-search circuits near the lower 60 ±5-megacycle sideband causes erratic operation of the acquisition local oscillator. This condition occurs when the difference frequency between the local oscillator frequency and magnetron frequency is less than ±55 megacycles (C, fig. 75).

2. Limiter bias voltage is removed from the grid of V11A (fig. 76.1), causing V11A to conduct and deenergize K1. The ac auto-search signal is applied to P1-1, causing the AFC motor-generator to retune the local oscillator to a lower frequency. The grid of V11A is not grounded through K3 at this time, since the local oscillator is not at the low frequency limit of its tuning range, and the AFC motor-generator has not actuated S13. When the acquisition local oscillator is retuned to a frequency which is 60 ±5 megacycles below the acquisition magnetron frequency, limiter bias voltage is developed at the grid of V4 and applied to the grid of V11A. The limiter bias voltage cuts off V11A, causing K1 to energize.

3. The acquisition AFC attempts to resume normal operation. However, the polarity of the error pulses developed by V5 at the 60 ±5 megacycle lower sideband are opposite to the polarity of the error pulses developed by V5 at the 60 ±5-megacycle upper sideband. The error pulses cause the AFC motor-generator to retune the acquisition local oscillator to a higher frequency. Limiter bias voltage is again removed from the grid of V11A, causing V11A to conduct and deenergize K1. The ac auto-search signal is again applied to P1-1, causing the AFC motor-generator to reverse its direction of rotation and retune the acquisition local oscillator to a lower frequency which again approaches the lower sideband. This hunting by the acquisition local oscillator continues. Hunting is indicated by the flashing of AUTO FREQ. control-hunt indicator light I3 located on the acquisition RF power supply control, and AFC-HUNT indicator light I4 located on the acquisition control-indicator. These two neon indicator lights are operated when the output of the low-power servo amplifier exceeds +40 volts.

4. To correct the hunting action by the acquisition local oscillator and to reestablish normal AFC operation, AFC-RELEASE switch S4 (located on the acquisition RF power supply control) or AFC-RELEASE switch S10 (located on the acquisition and IFF control indicator) must be operated. Operation of either S4 or S10 applies a ground to K2, causing K2 to energize. Contacts 2 and 3 of K2 close, grounding the grid of V11A through P2-13. Amplifier V11A conducts, causing K1 to deenergize. Since contacts 4 and 6 of K2 are now open, R9 is removed from the voltage divider leaving only R54 and R56 connected from ground to terminal 3 of T8. An increased ac auto-

search developed across R56 is applied through P2-9, contacts 2 and 3 of K3, P2-11 and contacts 1 and 3 of K1 to P1-1 which overrides the error pulses produced by V5, causing the AFC motor-generator to retune the acquisition local oscillator to the low frequency limit of its tuning range. From the low frequency limit of the acquisition local oscillator tuning range, the autosearch operation is the same as that described in *(c)2* above.

78.6 (U). Auxiliary IF Amplifier 9156573

a. General. Two auxiliary IF amplifiers are used when the antijam display modification is installed. The input to each amplifier is the 60-megacycle output from the frequency converter, with each amplifier providing two IF outputs. A crystal current output for external metering is also provided.

b. Detailed Theory.

(1) The auxiliary IF amplifier is comprised of two grounded grid amplifier stages V1 and V2, thereby permitting maximum gain with a minimum of noise.

(2) The 60-megacycle signal is applied through IF IN connector P1, and is coupled through capacitor C1 to the cathode of grounded grid amplifier V1. Resistor R1 is the cathode resistor which sets the grid lines operating point and capacitor C2 stabilizes this voltage. Inductor L1 tunes the input circuit to the desired frequency. The output of V1 is developed across the primary of transformer T1, and is coupled from the secondary of T1 to the cathode of grounded grid amplifier V2. Transformer T1 is tuned to obtain the desired frequency response by the tuning circuit consisting of capacitors C3 and C4 and inductor L2. Unbypassed cathode resistor R2 allows negative feedback to stabilize the amplifier gain. The output of V2 is developed across the primary of transformer T2, with resistor R3 broadening the frequency response. The sec-

ondary of T2 is tuned to the desired frequency by capacitors C5 and C6. Resistors R4 and R5 function both as output matching resistors and as a voltage divider for deriving a low amplitude output at connector J3 from the high amplitude output appearing at connector J2.

(3) Capacitors C7, C8, and C9 in conjunction with networks Z1 and Z2 provide decoupling for the plate voltage power supply. Inductors L3, L4, and L5 in conjunction with capacitors C10, C11, and C12 form a low pass filter which removes the ac component from the 60-megacycle input, but passes a dc crystal current through connector J1-A to the external metering circuit. Inductors L6, L7, and L8 with capacitors C13, C14, and C15 decouple the filaments and prevent RF from entering the filament transformer.

78.7 (U). IF Amplifier 9156675

a. General. IF amplifier consists of relays K1 and K2, network Z2, and acquisition IF preamplifier 7620695. Refer to figure 55.1, TM 9-1430-257-20 for all references.

b. Detailed Theory.

(1) Theory of acquisition IF preamplifier 7620695 is covered in paragraph 72.

(2) Relay K1, when energized, switches the sync pulse to the modulator off. When deenergized, relay K1 allows the sync pulse to pass to the modulator.

(3) Relay K2, when deenergized, terminates the input from the auxiliary IF channel and applies the input from the main IF channel to the acquisition IF preamplifier. When energized, relay K2 terminates the input from the main IF channel and applies the input from the auxiliary IF channel to the acquisition IF preamplifier.

(4) Network Z2 watches the output of the acquisition IF preamplifier from J1 to the input of coaxial line connected to connector P7.

78.8 (U). Acquisition Preselector Cavities 9990523 and 9990524

Acquisition preselector cavities 9990523 and 9990524 (fig. 55.1, TM 9-1430-257-20) are electrically identical to the acquisition preselector 7621790 discussed in paragraph 69. One of the cavities is used for the main IF channel and the other cavity is used for the auxiliary IF channel.
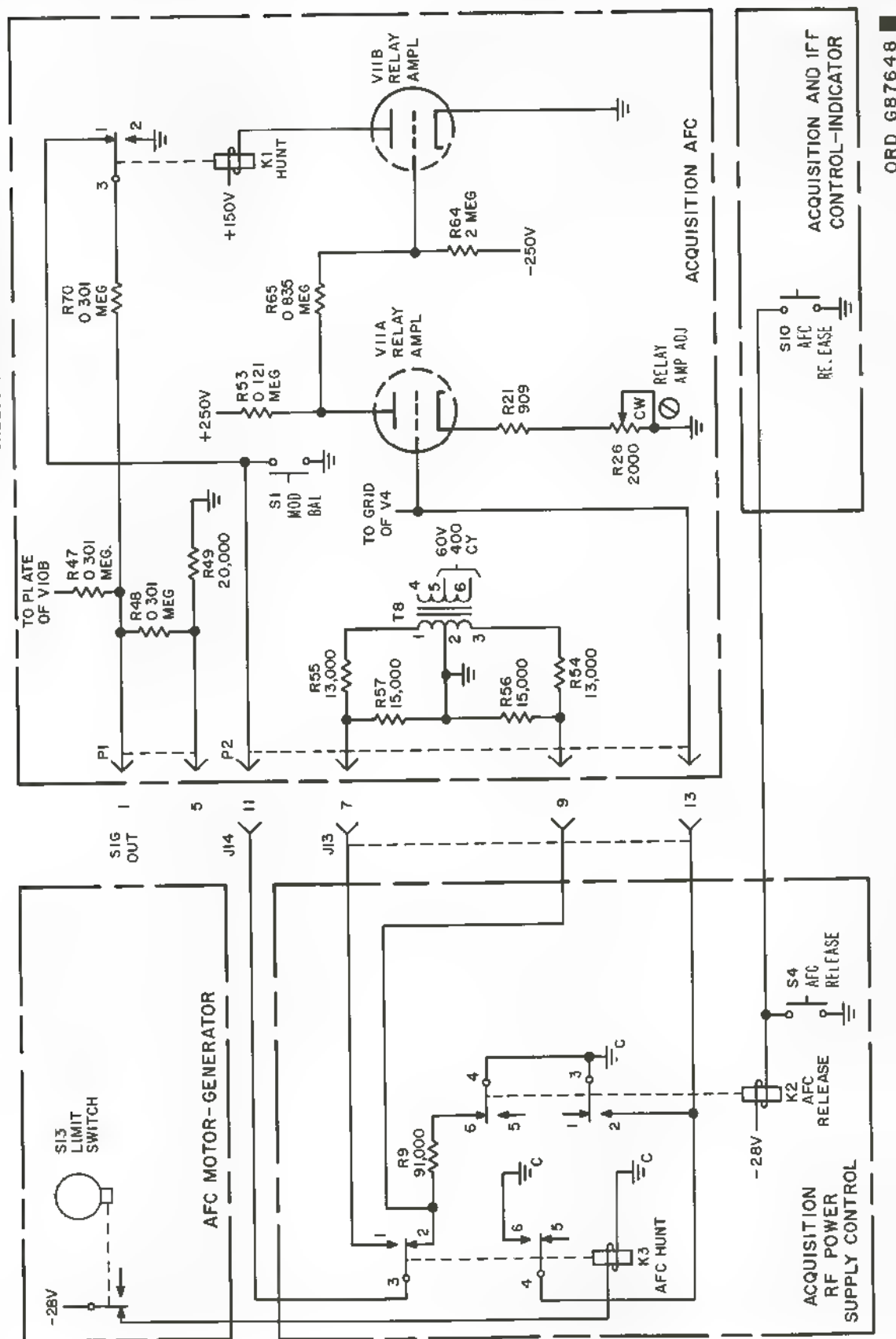
Figure 76.1 (U). Auto-search circuitry—functional schematic diagram— used with AJD.

ORD G87648

210.7

CHAPTER 7 (U)

ACQUISITION ANTENNA

79 (U). General

Acquisition antenna 9000289, 8158132, or 9156580 is a pillbox-and-reflector type antenna which is used by the acquisition radar system to radiate and receive RF energy. The antenna is driven in azimuth through 360° by a three-phase motor which provides antenna rotational speeds of either 5, 10, or 15 rpm. The reflector portion of the antenna is controlled by a hydraulic control unit in a manner which permits the elevation and pattern of the transmitted beam to be varied. The pillbox, reflector assembly, and hydraulic control unit are enclosed in a lightweight fiberglass radome for protection against weather and birds or insects. Figure 79 shows the acquisition antenna with radome removed.

80 (U). Reflector Assembly

a. As shown in figure 80, the reflector assembly is composed of a primary reflector and a secondary reflector, both of which are in the form of gratings. The gratings are made up of many evenly spaced horizontal metallic bars, approximately 15 feet in length and placed so that they form a parabolic
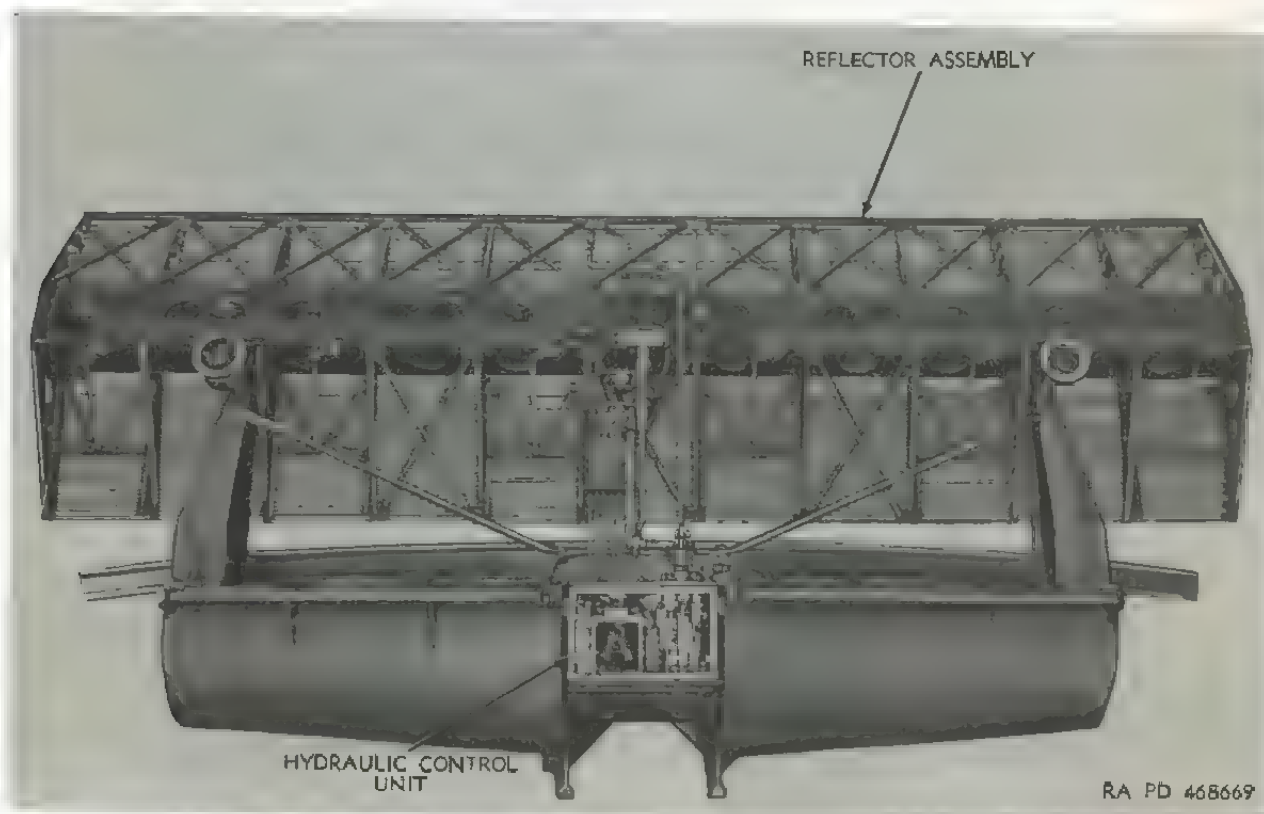
Figure 79 (U). Acquisition antenna—rear view—radome removed.
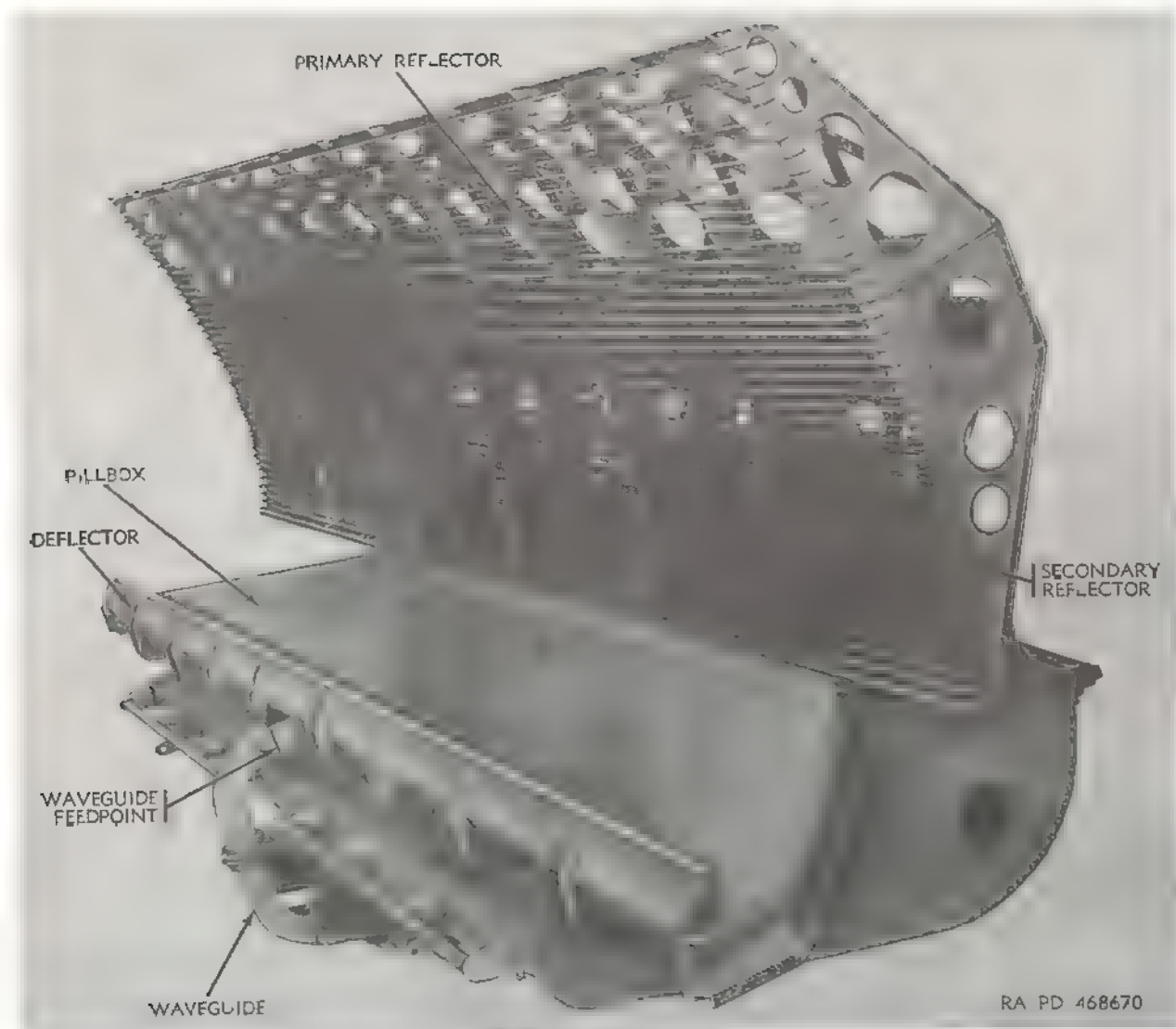
Figure 80. (U) Acquisition antenna—reflector assembly and pillbox.

cross section. The secondary reflector is mounted so that it can be either fully retracted into the primary reflector and become a geometric part of it, or injected into the lower half of the concave surface to change the curvature of the reflector assembly. The secondary reflector is shown fully retracted in A, figure 81, and fully injected in B, figure 81. With the secondary reflector fully retracted, the antenna radiates a long-range pencil-shaped beam of RF energy.

b. With the secondary reflector fully injected, the antenna radiates a shorter range fan-shaped beam of RF energy. The fan-shaped beam is not symmetrical with the axis of maximum radiation; rather, it follows a consecant-squared pattern, radiating more RF energy above the axis than below it. This results in greater elevation coverage for the acquisition radar system. Injection occurs automatically at a predetermined point during the time the reflector assembly is being tilted upward.

PENCIL BEAM (SECONDARY
REFLECTOR RETRACTED)

WAVEGUIDE

A

FAN SHAPED BEAM
(SECONDARY REFLECTOR
INJECTED)

WAVEGUIDE

B
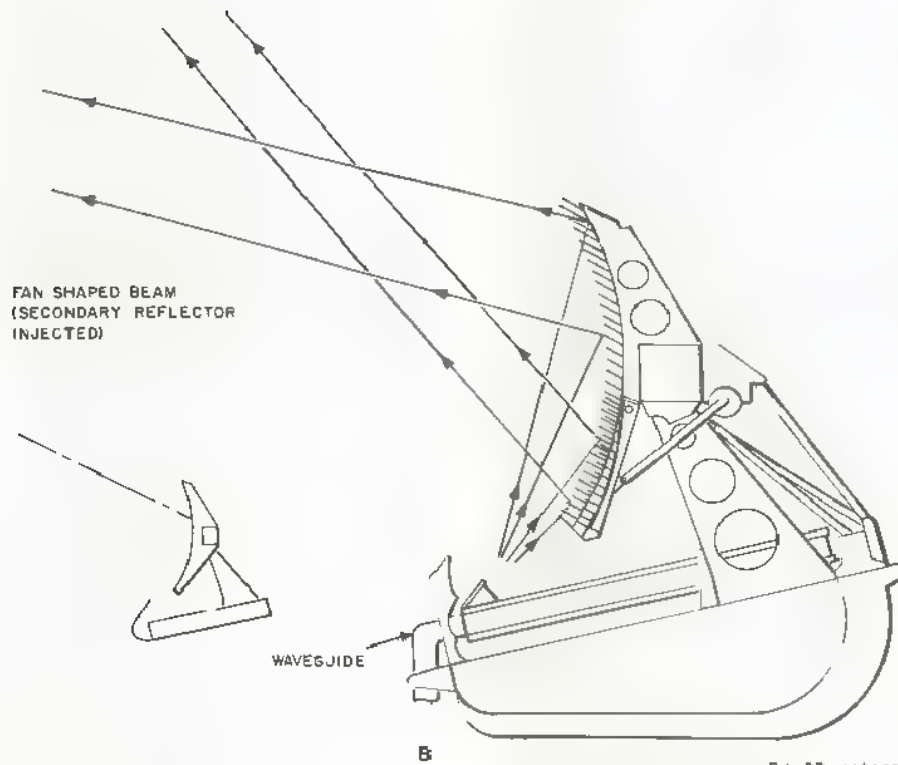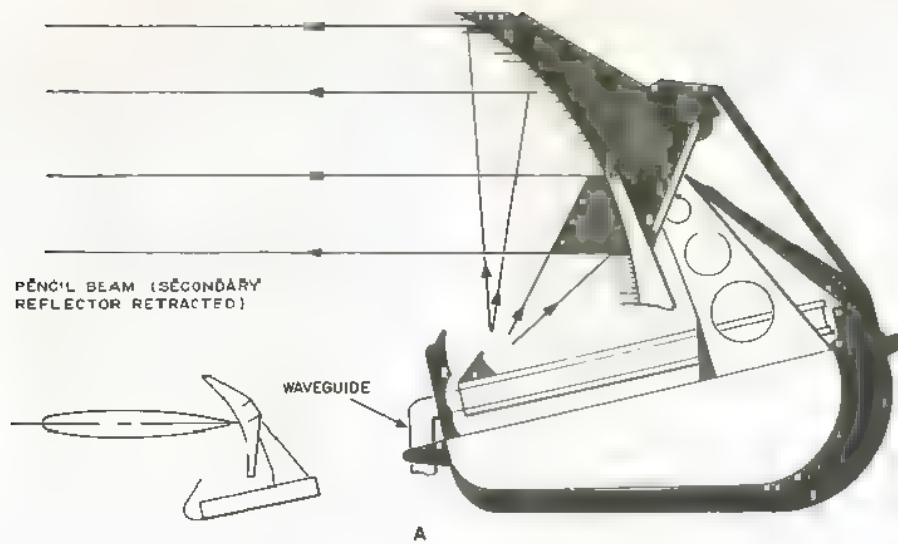
RA PD 468671

Figure 81. (U) Acquisition antenna—secondary reflector retracted and injected.

CONFIDENTIAL

Retraction is likewise automatic and occurs during the time the reflector assembly is being tilted downward. Injection or retraction is completed in 1° of reflector assembly travel. The point in the tilt cycle at which injection and retraction occur is dependent on the vertical scan mode that is selected by the operator. Four vertical scan modes have been adopted for use in the acquisition radar system. A complete discussion of vertical scan and elevation coverage is contained in paragraph 84.

81. Pillbox

The pillbox (fig. 82) is a parabolic cavity which couples RF energy from the waveguide to the reflector assembly. The pillbox receives the RF energy from the waveguide connected at the waveguide feedpoint (fig. 80 and A, fig. 82). The RF energy radiates toward the parabolically curved wall of the pillbox (B, fig. 82). The energy is reflected from the curved wall and is radiated back toward the bend-and-flap (deflector) at the front of the pillbox. The reflected energy is in phase with the energy radiated from the feedpoint. The feedpoint is offset 1 inch from the focal point of the pillbox to prevent standing waves from occurring at the feedpoint. Standing waves, if permitted to occur at the feedpoint, would produce an impedance mismatch between waveguide and pillbox, thus causing a loss of RF energy. The bend and flap (deflector) directs the RF energy, received from the curved wall, toward the gratings of the reflector assembly mounted above the pillbox.

82. Hydraulic Control Unit 8607284 and Cylinders 8011415 and 8011416

a. The hydraulic control unit 8607284 (fig. 83) develops and controls oil pressure to motivate two cylinders which tilt the reflector assembly to permit vertical scan. Each cylinder is designated in terms of the portion of the reflector assembly which it operates. Thus, the cylinder which tilts the primary reflector is termed the primary hydraulic cylinder 8011416; the cylinder which tilts the secondary reflector is termed the secondary hydraulic cylinder 8011415.

b. The primary hydraulic cylinder (fig. 84) is a cylinder-piston mechanism which is anchored to the antenna base. The movable piston shaft of the cylinder is mechanically coupled to the back side of the primary reflector. The primary hydraulic cylinder tilts the primary reflector upward when hydraulic oil pressure is applied to the lower face of the cylinder piston, and downward when pressure is applied to the upper face of the piston. The brake on the cylinder is spring-loaded and serves to clamp the cylinder piston shaft in position when oil pressure in the hydraulic lines falls below 50 pounds per square inch (psi). The secondary hydraulic cylinder (fig. 85) is similar to the primary hydraulic cylinder, except that both ends of its piston shaft are mechanically coupled to the back side of the secondary reflector by means of the secondary-reflector control linkage (fig. 83).

c. Oil pressure to and from the hydraulic cylinders is channeled by the hydraulic control unit (figs. 86 and 87). The hydraulic control unit determines vertical movement of the reflector assembly and is controlled either by ANTENNA - ELEVATION scan switch S6 located on the acquisition control indicator of the battery control console or by jogging switch S1 located on the underside of the hydraulic control unit. The hydraulic control unit contains the following: an oil reservoir, a motor-driven centrifugal pump, a cartridge type oil filter, a relief valve, an oil pressure gage, a distribution block, a solenoid valve, a valve assembly, two check valves, two cam-type momentary contact limit switches (upper and lower), an injection piston, and a hydraulic control relay assembly. The function of the ANTENNA—ELEVATION scan switch and the hydraulic control relay assembly is discussed in paragraph 83.

   (1) The oil reservoir (fig. 88) stores the oil required for use by the hydraulic system.

   (2) The motor-driven centrifugal pump (fig. 89) develops and maintains pressure on the oil. The pump is of the rotary type and is directly driven by a three-phase motor. Both pump and motor are enclosed in a common housing.

   (3) The cartridge-type oil filter (fig. 90) is used for filtering the oil passed by the

CONFIDENTIAL
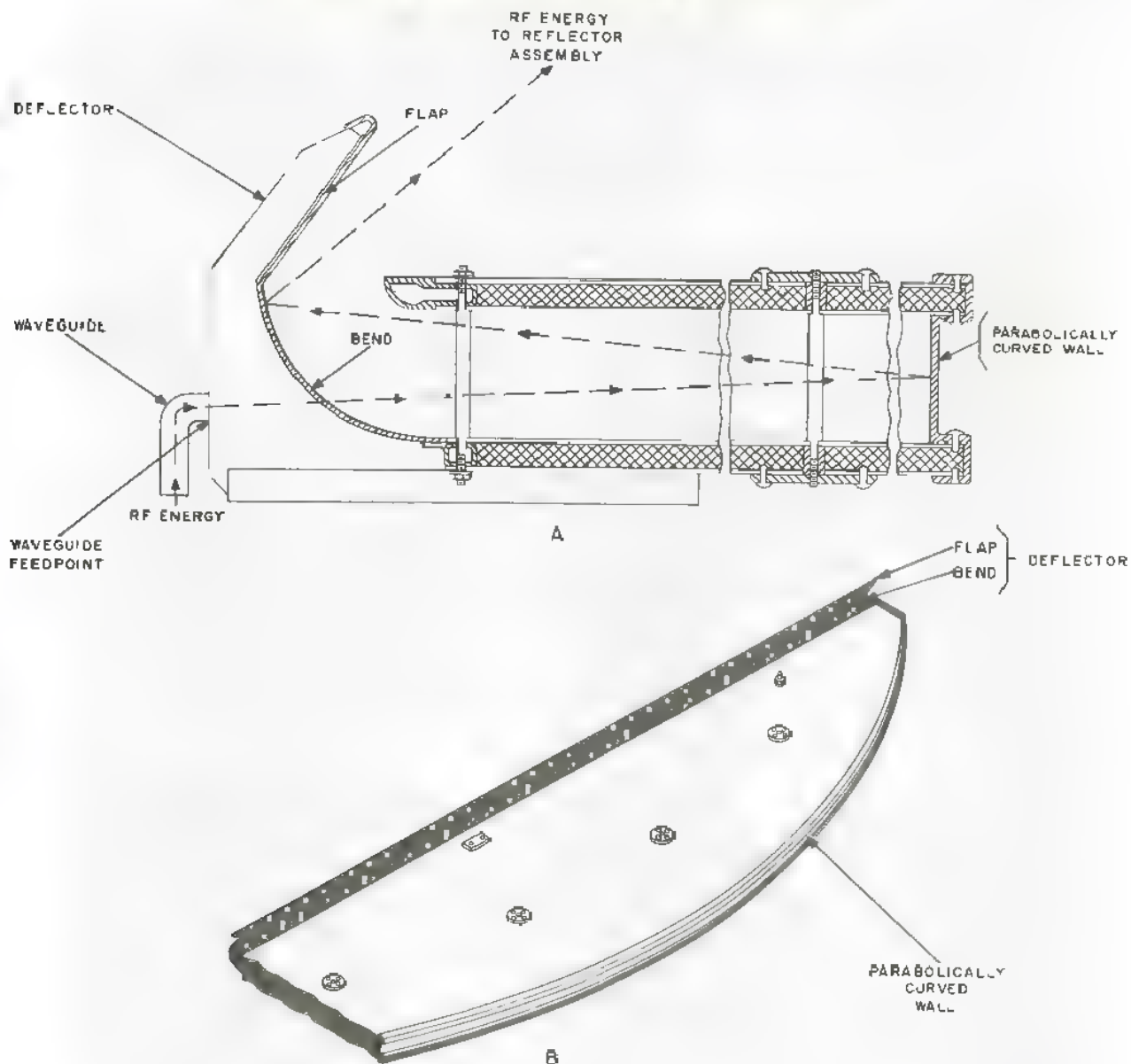
RA PD 468672

Figure 82. (U) Pillbox.

centrifugal pump. Oil flows from the oil pump through the IN port and around the filter cartridge. The filter cartridge collects dirt and other foreign matter on the outside, allowing the filtered oil to flow through the inside of the cartridge to the OUT port. The cartridges are replaced at regular main-tenance intervals to maintain good filtering action.

(4) The relief valve (fig. 91) prevents oil pressure in the hydraulic system from exceeding 250 psi. This valve operates on the principle of the spring-loaded ball poppet. The tension of the spring is adjusted so that the poppet remains seated

CONFIDENTIAL

PRIMARY HYDRAULIC CYLINDER

SECONDARY HYDRAULIC CYLINDER

INJECTION CONTROL ROD

VALVE

SECONDARY REFLECTOR CONTROL LINKAGE

SECONDARY REFLECTOR CONTROL LINKAGE

HYDRAULIC CONTROL UNIT

RA PD 168673
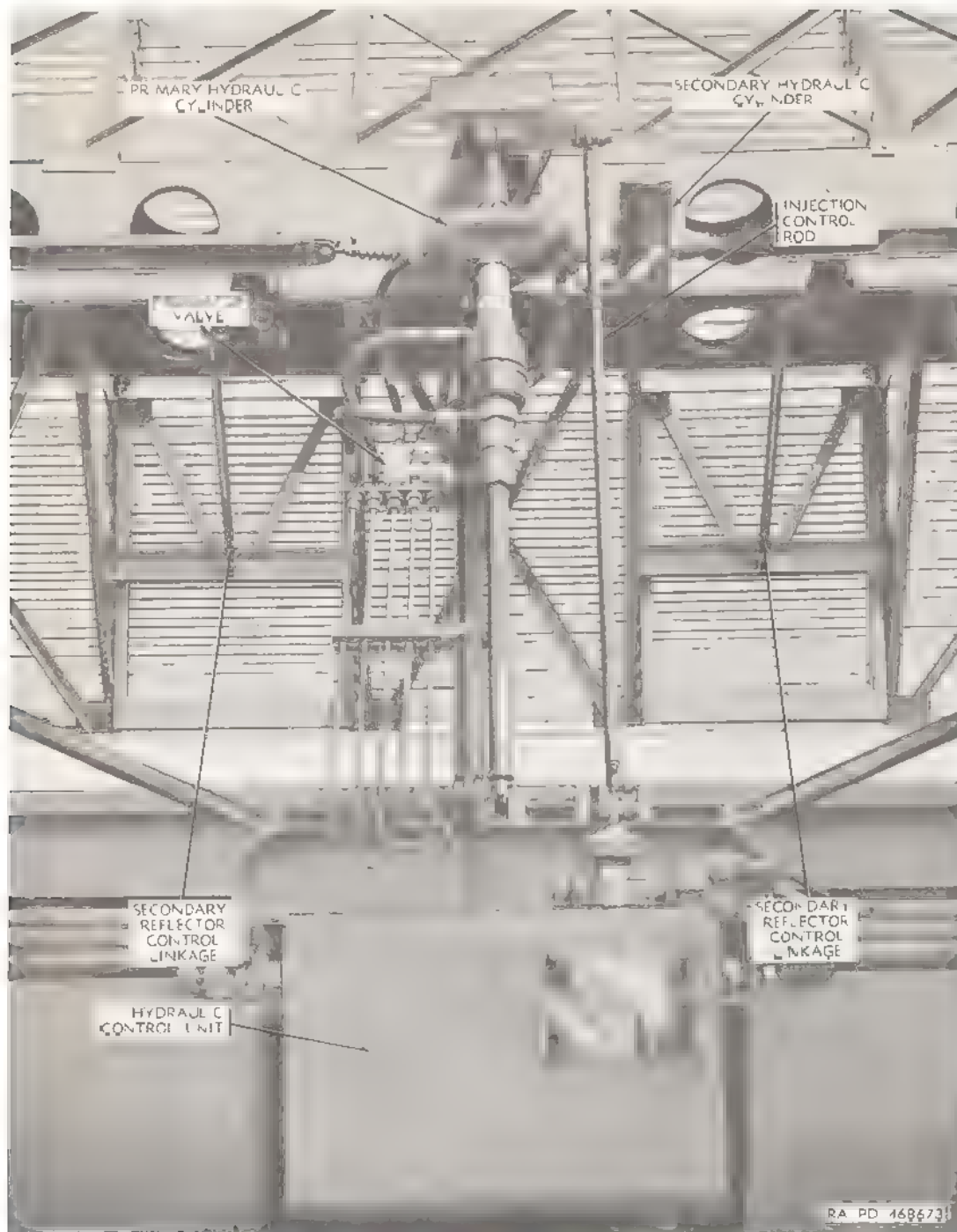
Figure 83. (U) Acquisition antenna — hydraulic control unit, cylinders, and control linkage.

COUPLED TO
PRIMARY REFLECTOR

OIL PRESSURE FROM
DISTRIBUTION BLOCK

BRAKE
SHOE

PISTON
SHAFT

OIL PRESSURE TO BRAKE
ON SECONDARY
HYDRAULIC CYLINDER
ASSEMBLY

BRAKE
SPRINGS

CYLINDER

PISTON

CONNECTED TO
"UP" CHECK
VALVE

CONNECTED TO
"DOWN" CHECK
VALVE

AIR VENT

ANCHORED TO
ANTENNA BASE
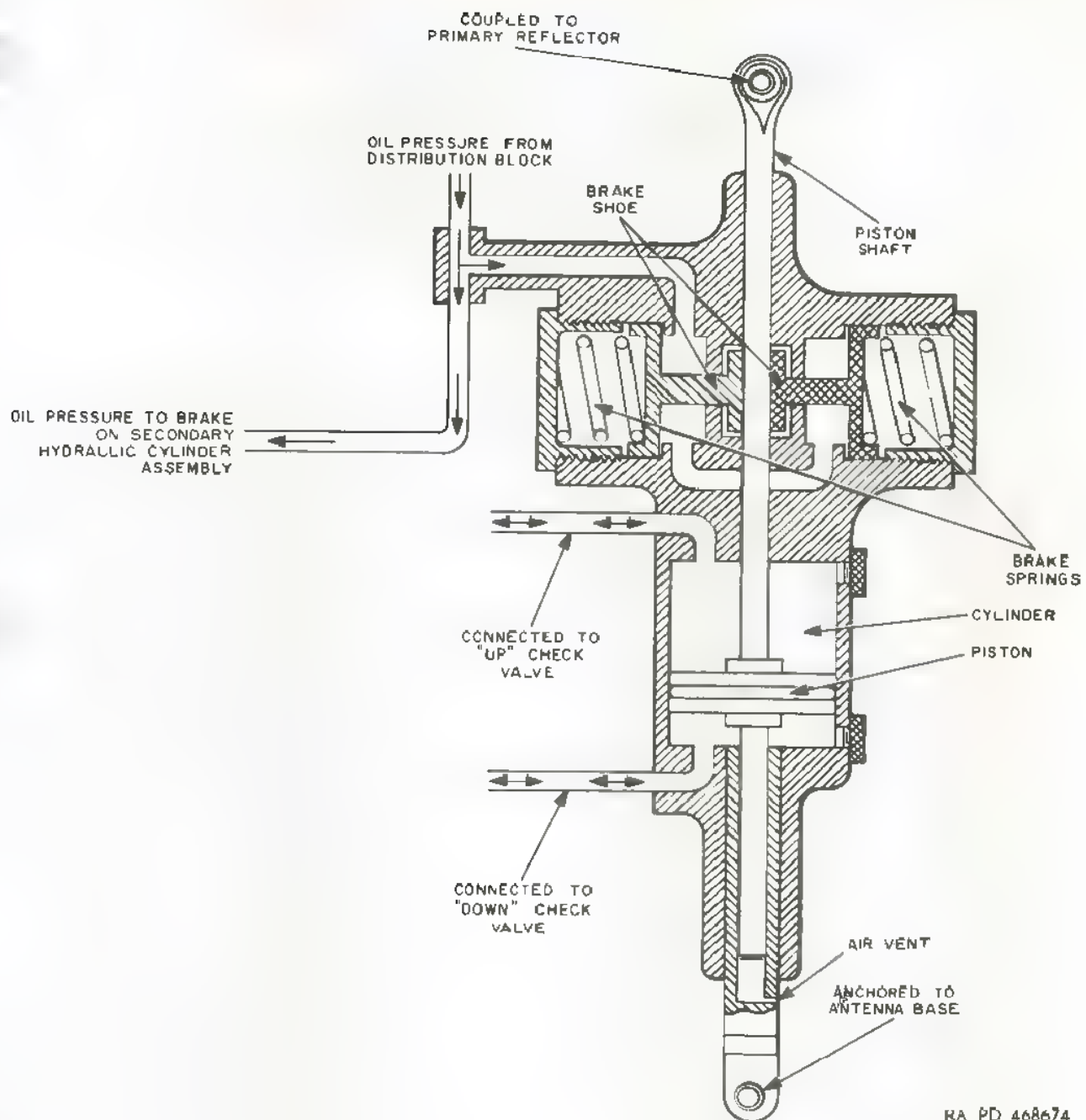
RA PD 468674

Figure 84. (U) Primary hydraulic cylinder and brake.
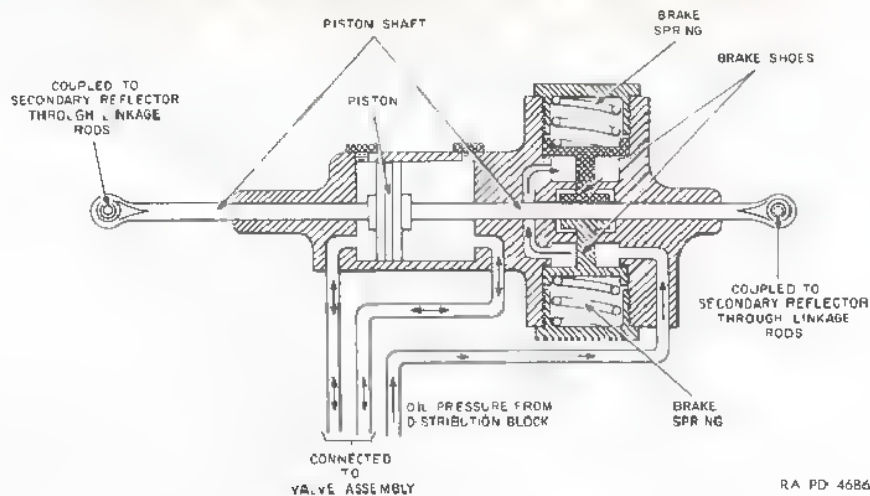
Figure 85. (U) Secondary hydraulic cylinder and brake

as long as the pressure in the system re mains below 250 psi. Pressure in excess of 250 psi overcomes the tension of the spring and unseats the poppet. At this point, oil pressure in excess of 250 psi is allowed to pass through the relief chamber of the valve and enter the return line to the oil reservoir.

(5) The oil pressure gage is connected to the pressure chamber of the relief valve. The gage is graduated to read 0 to 600 psi. A reading of 10 to 20 psi is considered normal when the reflector assembly is at a static elevation. A reading of 250 ± 10 psi is considered normal during the time that the reflector assembly is being tilted.

(6) The distribution block (fig. 92) acts as a junction for oil to and from other functional parts of the hydraulic system. The distribution block has two channels, a pressure channel which receives and distributes oil at a pressure of 250 psi, and a return channel which collects excess and used oil for return to the oil reservoir.

(7) The solenoid valve (fig. 93) is composed of a spring-loaded selector valve and two two electrically operated solenoids (up and down). The selector valve provides two possible paths for channeling oil pressure to the primary hydraulic cylinder. One path (A, fig. 93) channels

oil pressure to the bottom face of the cylinder piston for elevating the reflector assembly. The other path (B, fig. 93) channels oil pressure to the top face of the cylinder piston for depressing the reflector assembly. The path for the oil pressure depends on the position of the movable portion of the valve; this position is determined by the solenoid that is energized. If neither of the two solenoids is energized, the selector valve is held at center position by the action of the springs. At center position (C, fig. 93), oil flows into and out of the valve which channels the oil directly back to the reservoir. Thus, the oil pressure is diverted from paths leading to the primary hydraulic cylinder.

(8) The two identical check valves (figs. 94 and 95), designated "up" and "down", respectively, determine the rate of flow of oil returned from the primary hydraulic cylinder to the reservoir. When the "up" solenoid of the solenoid valve is energized, oil pressure flows into the "down" check valve (fig. 94), unseats the spring-loaded ball poppet, and continues unrestricted to the cylinder of the primary hydraulic cylinder. This causes the primary hydraulic cylinder piston to move in a direc-

INJECTION
PISTON

INJECTION
ADJUSTMENT
SCREW

O L PRESSURE
GAGE

LOWER LIMIT
SWITCH

0 9
SCALE

CHECK VALVES

O L RESERVOIR

MOTOR DRIVEN
CENTRIFUGAL PUMP

RELIEF VALVE

VALVE ASSEMBLY

UPPER LIMIT
ADJUSTMENT
SCREWS

UPPER LIMIT
SWITCH

RA PD 468676
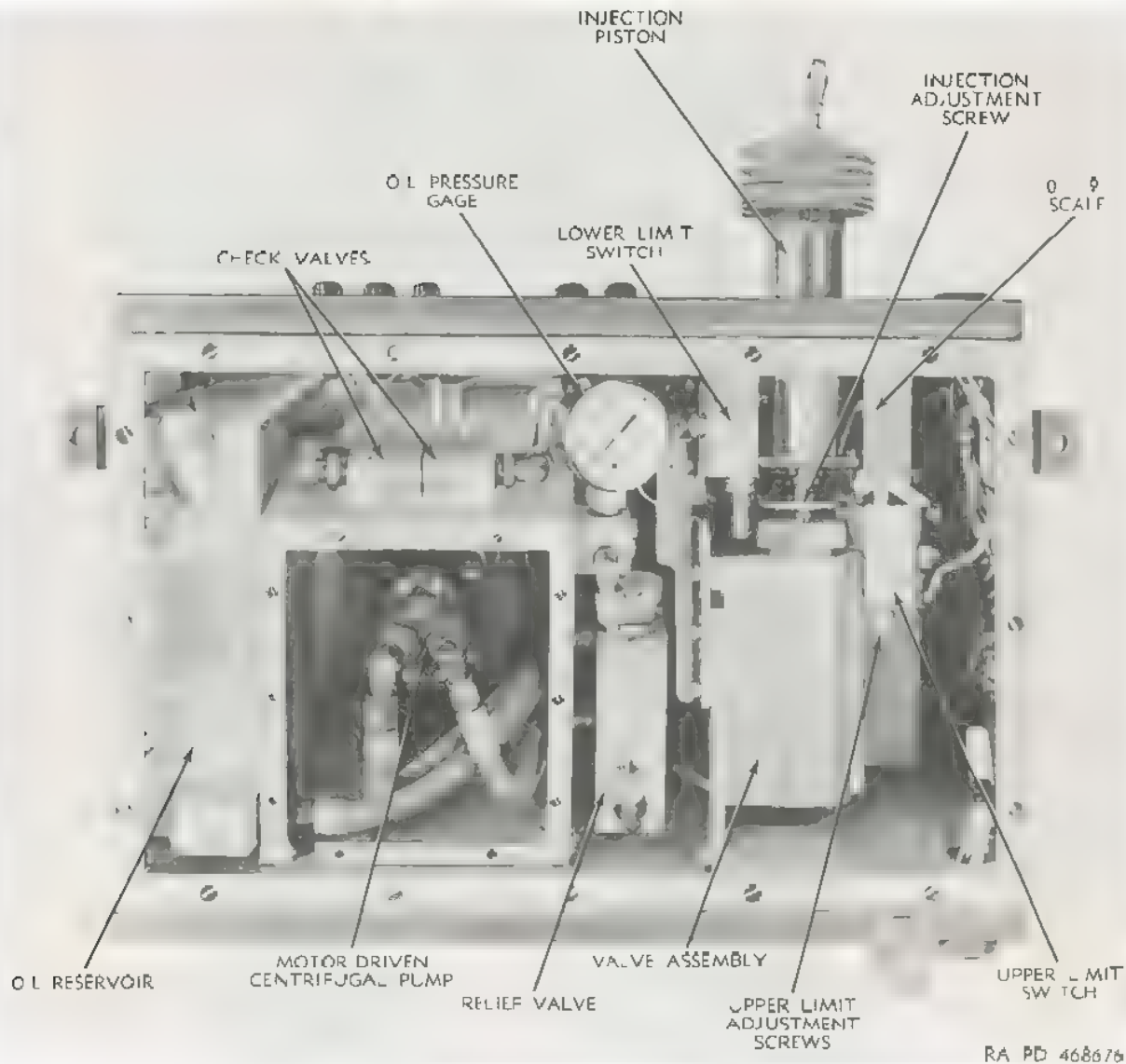
Figure 86. (U) Hydraulic control unit—front view—cover removed.

tion that tilts the reflector assembly upward and forces oil out of the cylinder. The oil that is forced out of the cylinder passes through the "up" check valve to enter the return line to the reservoir. However, the ball poppet of the "up" check valve cannot be unseated when pressure is applied to its back side. Therefore, the oil must bypass the poppet and enter the return line through the spring-loaded plunger. The amount of oil flow

through and around this plunger is determined by the spring tension on the plunger. When spring tension is increased, the flow of oil is proportionately restricted. This causes back pressure to develop on the primary hydraulic cylinder piston. The back pressure acts to slow the movement of the piston, thereby slowing the movement of the reflector assembly. When the "down" solenoid of the solenoid valve is energized, the above
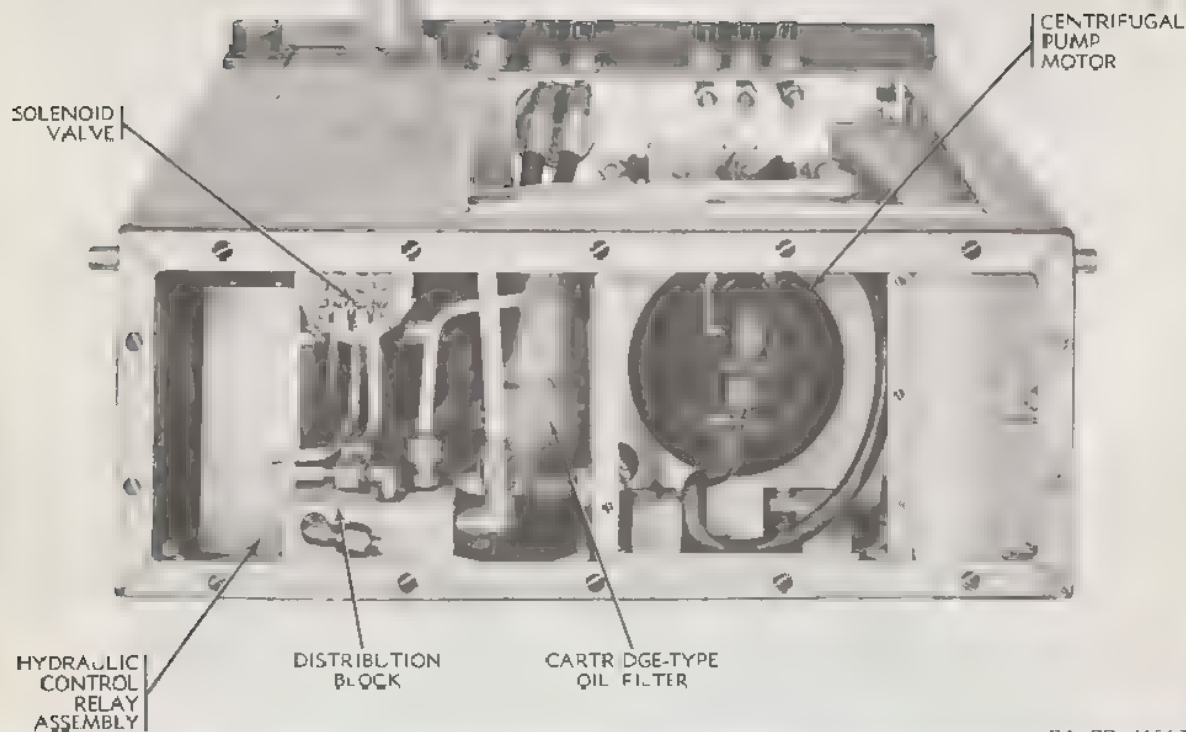
Labels on figure:
SOLENOID VALVE
CENTRIFUGAL PUMP MOTOR
HYDRAULIC CONTROL RELAY ASSEMBLY
DISTRIBUTION BLOCK
CARTRIDGE-TYPE OIL FILTER
RA PD 468677

Figure 87. (U) Hydraulic control unit—rear view—cover removed.

action is duplicated, except that the function of the check valves is interchanged (fig. 95). The pressurized oil is now directed to the primary hydraulic cylinder through the "up" check valve. The "down" check valve, in this case, performs the function of developing back pressure for the cylinder piston.

(9) The valve assembly (fig. 96) channels pressurized oil to and from the secondary hydraulic cylinder. The valve assembly is similar to the solenoid valve, except that it is mechanically operated. The spring-loaded movable portion of the valve assembly is coupled to the primary reflector of the reflector assembly by

means of the injection-control rod (fig. 83). As the primary reflector is tilted up or down, the position at which the injection-control rod operates the movable portion of the valve assembly (fig. 96) is reached. At this point, the valve assembly admits pressurized oil into the cylinder of the secondary hydraulic cylinder. Since there are no check valves to restrict oil forced out of the cylinder, the cylinder piston feels no back pressure and is caused to move rapidly to the extreme end of the cylinder. This is the only difference between primary and secondary hydraulic cylinder action. Thus, the secondary reflector is injected and
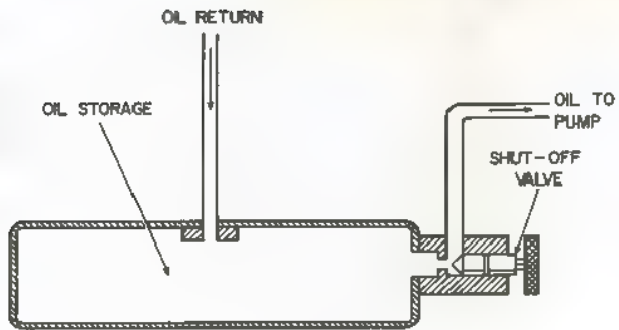
Figure 88 (U) Oil reservoir.
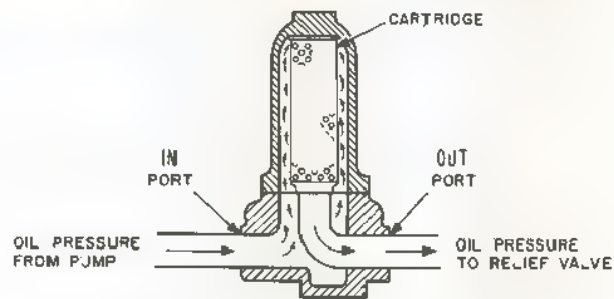
Figure 90 (U) Cartridge-type oil filter.
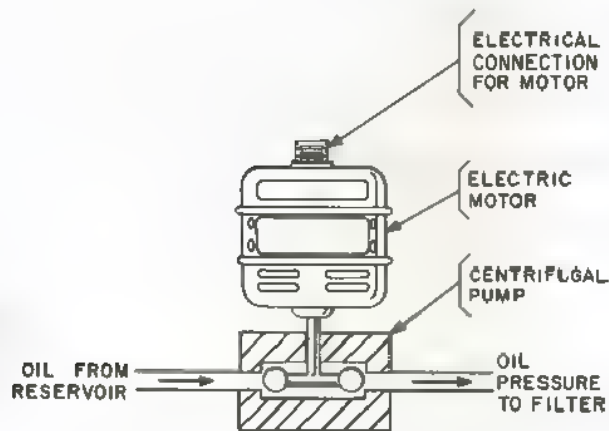
Figure 89 (U) Motor-driven centrifugal pump
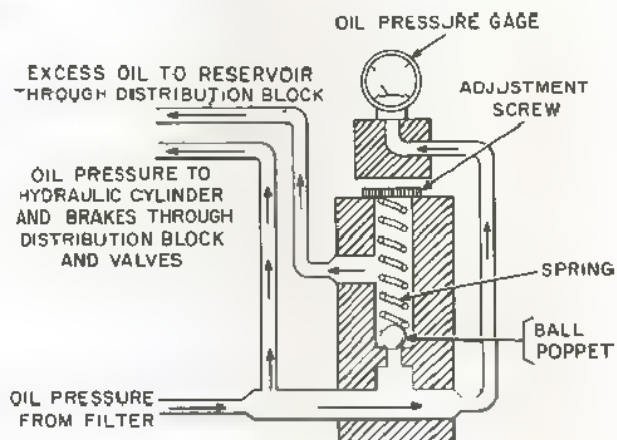
Figure 91 (U) Relief valve and oil pressure gage.

retracted rapidly when the reflector assembly is tilted up and down, respectively.

(10) The upper limit switch and lower limit switch (fig. 97) control the limits of reflector assembly tilt during automatic vertical scan operation of the antenna. The limit switches are of the momentary contact type and are operated alternately by a cam on the injection-control rod. The contacts of the upper limit switch are normally closed. The contacts of the lower limit switch are normally open. The limit switches, together with ANTENNA—ELEVATION scan switch S6, located on the acquisition control-indicator and the hydraulic control relay assembly, act to control the solenoid valve.

d. Figure 98 is a simplified drawing showing the channeling of oil pressure and the position of hydraulic system elements during an upward tilt of the reflector assembly. With three-phase power applied to the centrifugal pump motor, oil under pressure flows from the oil pump through the oil filter and into the relief valve. The relief valve is connected to two lines feeding the input side of the distribution block.

e. In the distribution block, one line directs oil pressure in excess of 250 psi back to the reservoir; the second line directs oil pressure of 250 psi into three paths on the output side of the distribution block. One of these paths leads to the brakes; the

OIL RETURN FROM
PRIMARY HYDRAULIC CYLINDER
THROUGH CHECK VALVE
AND SOLENOID VALVE

OIL RETURN
CHANNELS

OIL RETURN FROM SECONDARY HYDRAULIC CYLINDER THROUGH VALVE ASSEMBLY

OIL PRESSURE TO PRIMARY HYDRAULIC CYLINDER THROUGH SOLENOID VALVE AND CHECK VALVE (250 PSI)

OIL PRESSURE TO SECONDARY HYDRAULIC CYLINDER THROUGH VALVE ASSEMBLY (250 PSI)

OIL PRESSURE TO HYDRAULIC CYLINDER BRAKES (250 PSI)

OIL PRESSURE CHANNELS

EXCESS OIL PRESSURE FROM RELIEF VALVE

OIL PRESSURE FROM RELIEF VALVE (250 PSI)

OIL RETURN TO
RESERVOIR

RA PD 468682

Figure 92 (U) Distribution block.

second of these paths leads to the solenoid valve; and the third path leads to the valve assembly. Since the "up" solenoid is energized for an upward tilt of the reflector assembly, the movable portion of the solenoid valve is in the position shown.

f. In this position, the solenoid valve channels oil pressure through the "down" check valve to the lower face of the piston in the primary hy-

draulic cylinder. This causes the primary reflector to be tilted upward. Oil forced out of the upper end of the primary hydraulic cylinder is returned to the reservoir through the "up" check valve and the return port provided by the solenoid valve. The "up" check valve supplies back pressure which regulates maximum oil flow to approximately 1.2 gallons per minute, thus regulat-

CONFIDENTIAL

OIL RETURN TO RESERVOIR

OIL PRESSURE FROM DISTRIBUTION BLOCK

PRESSURE PORT

"UP" SOLENOID

"DOWN" SOLENOID

SPRING

SELECTOR VALVE

OIL FORCED OUT OF PRIMARY HYDRAULIC CYLINDER

OIL PRESSURE TO BOTTOM FACE OF PRIMARY HYDRAULIC CYLINDER PISTON

A "UP" SOLENOID ENERGIZED

OIL RETURN TO RESERVOIR

OIL PRESSURE FROM DISTRIBUTION BLOCK

PRESSURE PORT

"UP" SOLENOID

"DOWN" SOLENOID

SPRING

SELECTOR VALVE

OIL PRESSURE TO TOP FACE OF PRIMARY HYDRAULIC CYLINDER PISTON

OIL FORCED OUT OF PRIMARY HYDRAULIC CYLINDER

B "DOWN" SOLENOID ENERGIZED

OIL RETURN TO RESERVOIR

OIL PRESSURE FROM DISTRIBUTION BLOCK

PRESSURE PORT

"UP" SOLENOID

"DOWN" SOLENOID

SPRING

SELECTOR VALVE

C NEUTRAL POSITION

RA PD 468683

Figure 93. (U) Solenoid valve.

223

RESTRICTED
OIL RETURN
TO RESERVOIR
THROUGH SOLENOID VALVE

UNRESTRICTED
OIL PRESSURE
FROM SOLENOID VALVE

BALL
POPPET

SPRING

PRESSURE
PORT

"DOWN"
CHECK
VALVE

SPRING–
LOADED
PLUNGERS

ADJUSTMENT
SCREWS

"UP"
CHECK
VALVE

UNRESTRICTED OIL PRESSURE
TO PRIMARY HYDRAULIC CYLINDER

OIL FORCED OUT OF
PRIMARY HYDRAULIC CYLINDER
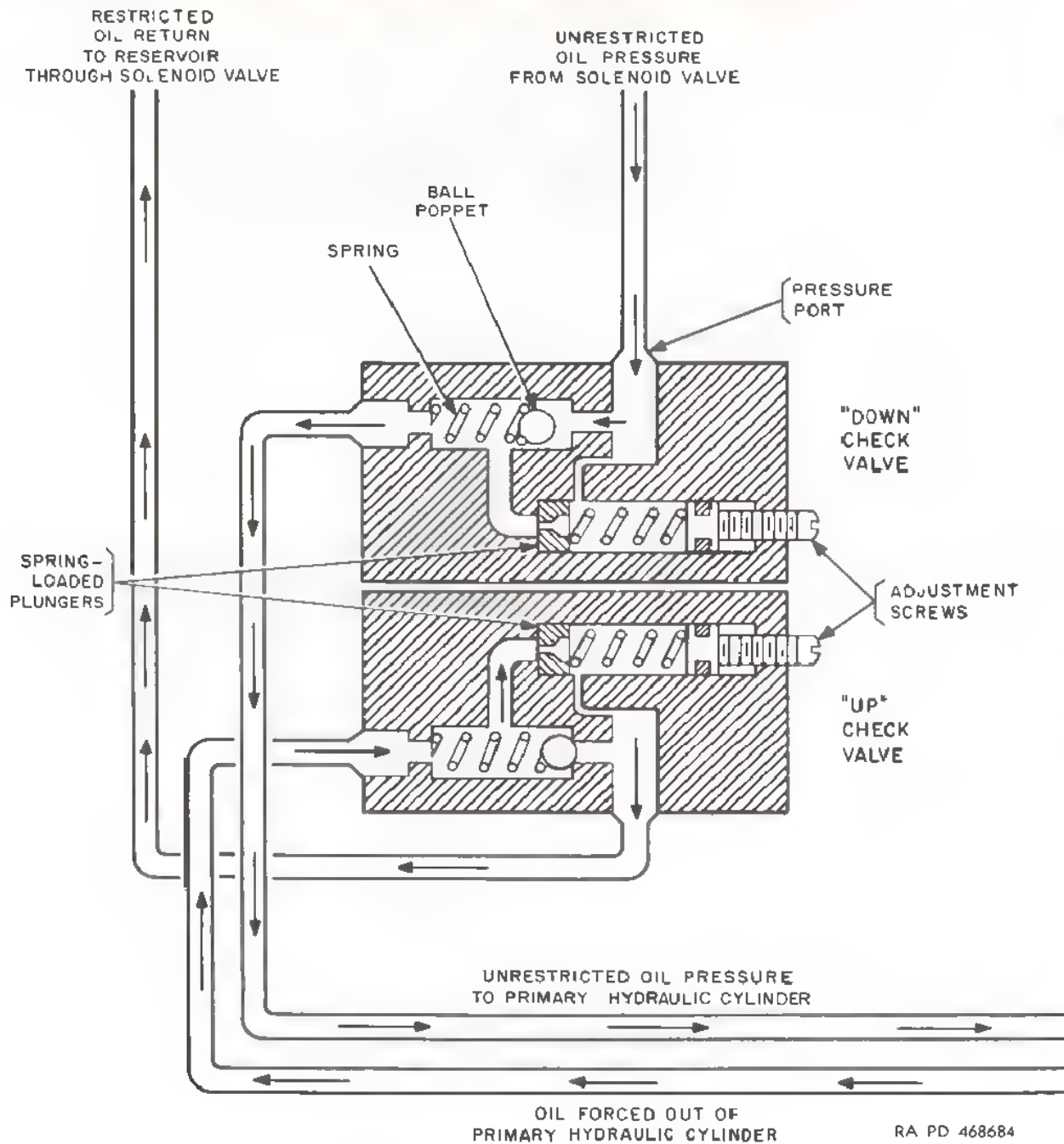
RA PD 468684

Figure 94. (U) Check valves—function while elevating reflector assembly.

UNRESTRICTED
OIL PRESSURE
FROM SOLENOID VALVE

RESTRICTED
OIL RETURN
TO RESERVOIR

"DOWN"
CHECK VALVE

ADJUSTMENT SCREWS

SPRING-LOADED
PLUNGERS

"UP"
CHECK VALVE

SPRING-LOADED BALL POPPET

OIL FORCED OUT OF
PRIMARY HYDRAULIC CYLINDER

UNRESTRICTED OIL PRESSURE
TO PRIMARY HYDRAULIC CYLINDER
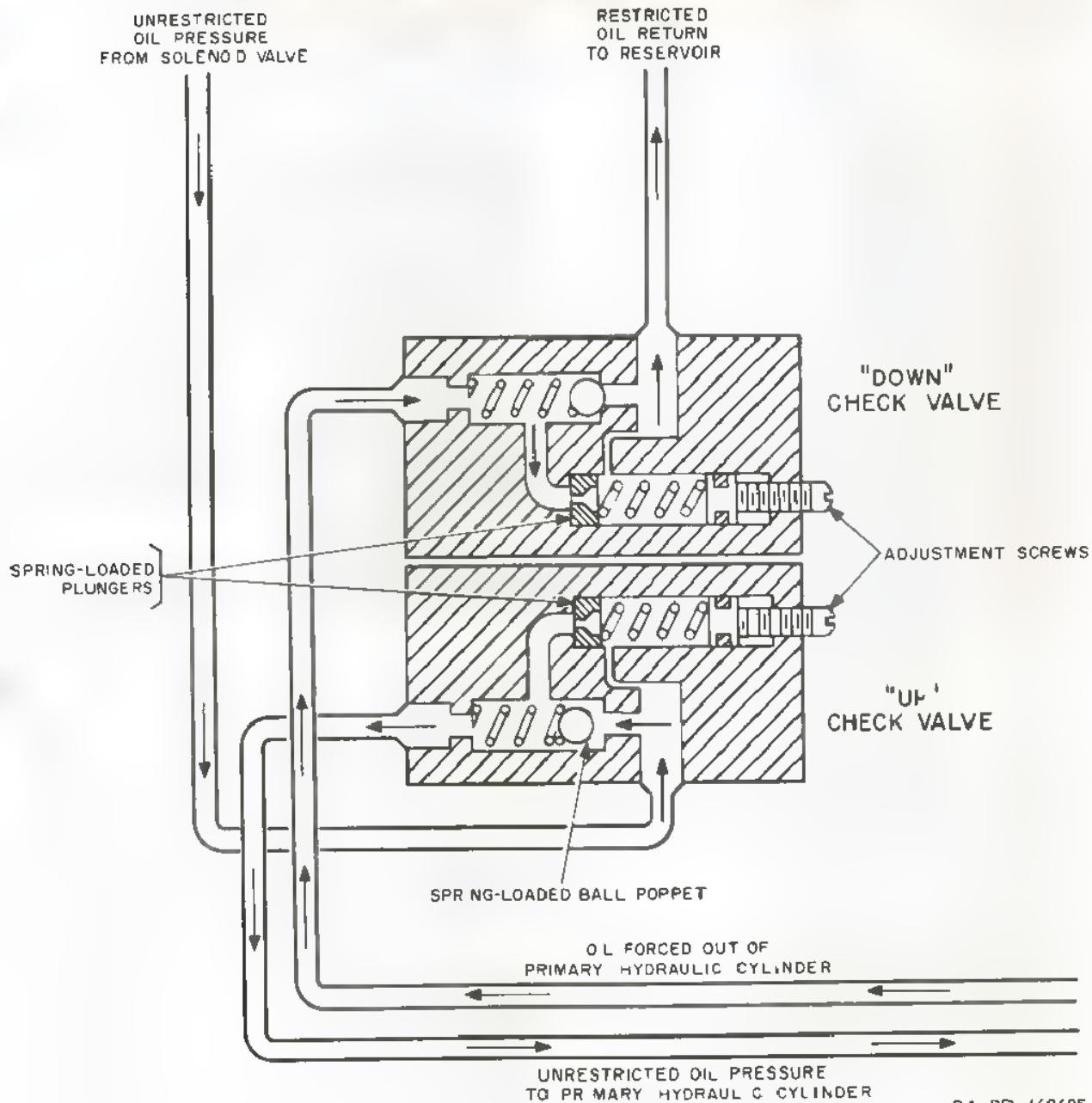
RA PD 468685

Figure 95. (U) Check valves—function while depressing reflector assembly.

ing the speed at which the reflector assembly is elevated. (The "down" check valve assumes this regulatory function when the reflector assembly is being tilted downward.)

g. As the primary reflector tilts upward, the injection-control rod fastened to it applies mechanical pressure to the top of the spring-loaded plunger of the valve assembly. At a predetermined time (variable with scan mode), the valve assembly admits oil pressure through its pressure

MECHANICAL PRESSURE
REMOVED BY
INJECTION—CONTROL ROD

MOVABLE PORTION

OIL RETURN
TO RESERVOIR

OIL PRESSURE
TO LEFT FACE OF
SECONDARY HYDRAULIC
CYLINDER PISTON

OIL PRESSURE
FROM DISTRIBUTION BLOCK

OIL FORCED OUT OF
SECONDARY HYDRAULIC
CYLINDER

RETRACTED POSITION

MECHANICAL PRESSURE
APPLIED BY
INJECTION—CONTROL ROD

OIL RETURN
TO RESERVOIR

OIL FORCED OUT OF
SECONDARY HYDRAULIC
CYLINDER

OIL PRESSURE FROM
DISTRIBUTION BLOCK

OIL PRESSURE TO RIGHT FACE
OF SECONDARY HYDRAULIC
CYLINDER PISTON

INJECTED POSITION

RA PD 468686

Figure 96 (U) Valve assembly.

port to the lower face of the piston in the secondary hydraulic cylinder. This causes the secondary reflector to be injected. Oil forced out of the upper end of the secondary hydraulic cylinder is returned to the reservoir through the return port provided by the valve assembly.

83. Hydraulic Control Relay Assembly 7612085

a. The hydraulic control relay assembly (fig. 99 and fig. 63, TM 9-1430-257-20) operates in conjunction with the limit switches to apply the ground potential necessary for energizing the solnoids of the solenoid valve. ANTENNA—ELEVATION scan switch S6, located on the acquisition control-indicator, applies ground to energize either the "up" solenoid or the "down" solenoid. Switch S6 is a three-position toggle switch, spring-loaded between center position and UP position.

b. When S6 is held manually in the UP position, ground potenital is applied to energize "up" relay K3. With K3 energized, ground potential is applied through its contacts and those of deener-

gized limit relay K1 to antenna elevation relay K2. As a result, K2 is energized and its contacts close to permit 120-volt, 400-cps, three-phase power to be applied to start the hydraulic pump motor. With K3 energized, ground is applied to energize the "up" solenoid of the solenoid valve. The reflector assembly tilts upward until stopped by the bottoming of the primary hydraulic cylinder piston against the end of the cylinder. The reflector assembly is held in this position or any intermediate elevated position due to the action of the primary hydraulic cylinder brake.

c. When the operator releases S6, the switch arm of S6 springs back to normal center position, thereby deenergizing K3, K2, and the "up" solenoid. With K2 deenergized, the hydraulic pump motor is deactivated. The deenergized state of the "up" solenoid permits the solenoid valve to offer an unrestricted path for oil to the reservoir. The unrestricted path through the solenoid valve causes a very rapid reduction in oil pressure throughout the entire hydraulic system. The drop in oil pressure (below 50 psi) permits the

226

CONFIDENTIAL

ROLLER

INJECTION
PISTON

LOWER
LIMIT
SWITCH

ROLLER

CAM

UPPER
LIMIT
SWITCH
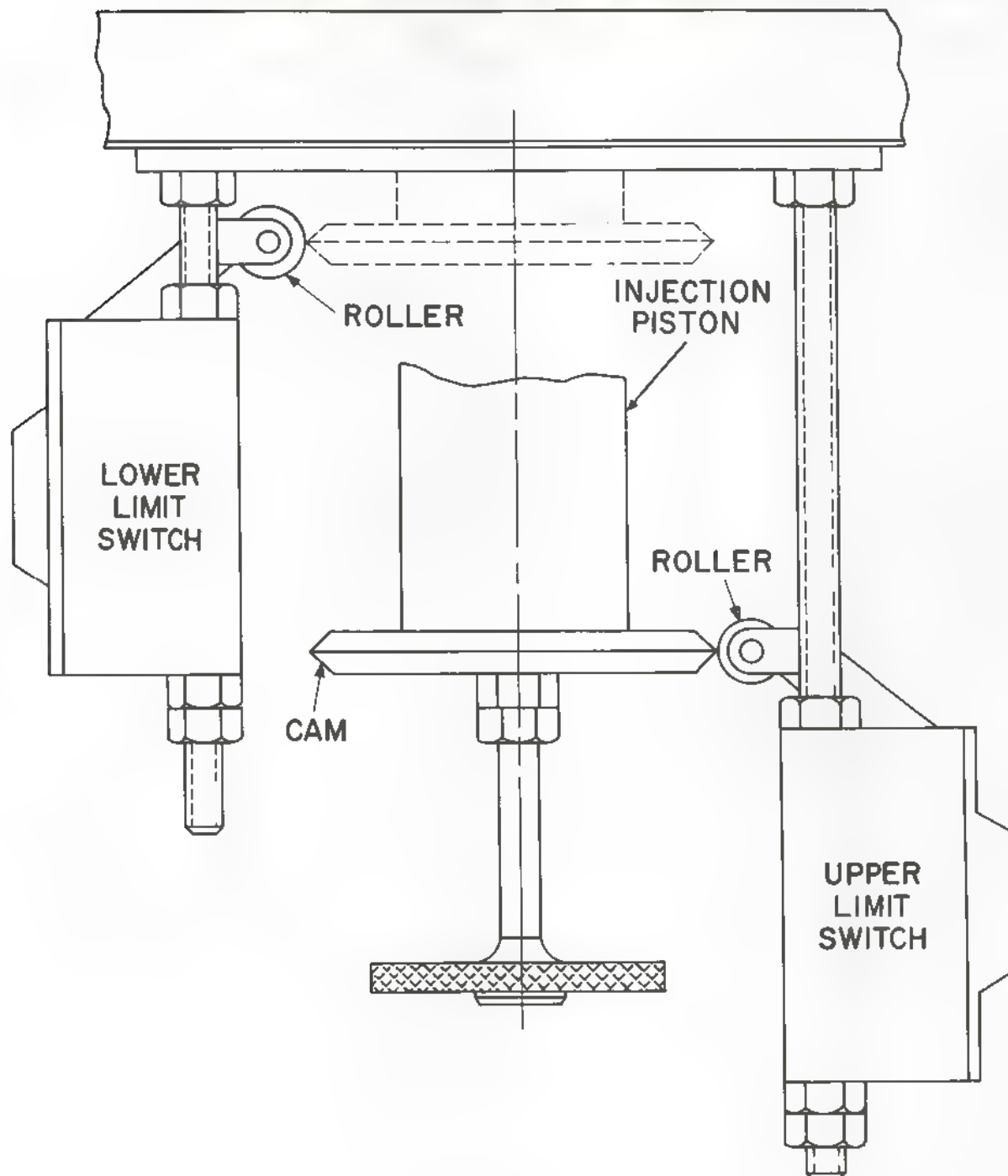
RA PD 468687

Figure 97. (U) Limit switches assembly.

CONFIDENTIAL

PRIMARY
REFLECTOR

SECONDARY
REFLECTOR

INJECTION-
CONTROL ROD

SECONDARY
HYDRAULIC
CYLINDER

UP

UP

PRIMARY
HYDRAULIC
CYLINDER

"UP"
CHECK VALVE

"DOWN"
CHECK VALVE

VALVE ASSEMBLY

BRAKE

BRAKE

"UP"
SOLENOID

"DOWN"
SOLENOID

REGULATOR
VALVE

SOLENOID
VALVE

DISTRIBUTION
BLOCK

| OIL RESERVOIR | OIL PUMP | OIL FILTER | RELIEF VALVE |

MOTOR

OIL
PRESSURE
GAGE
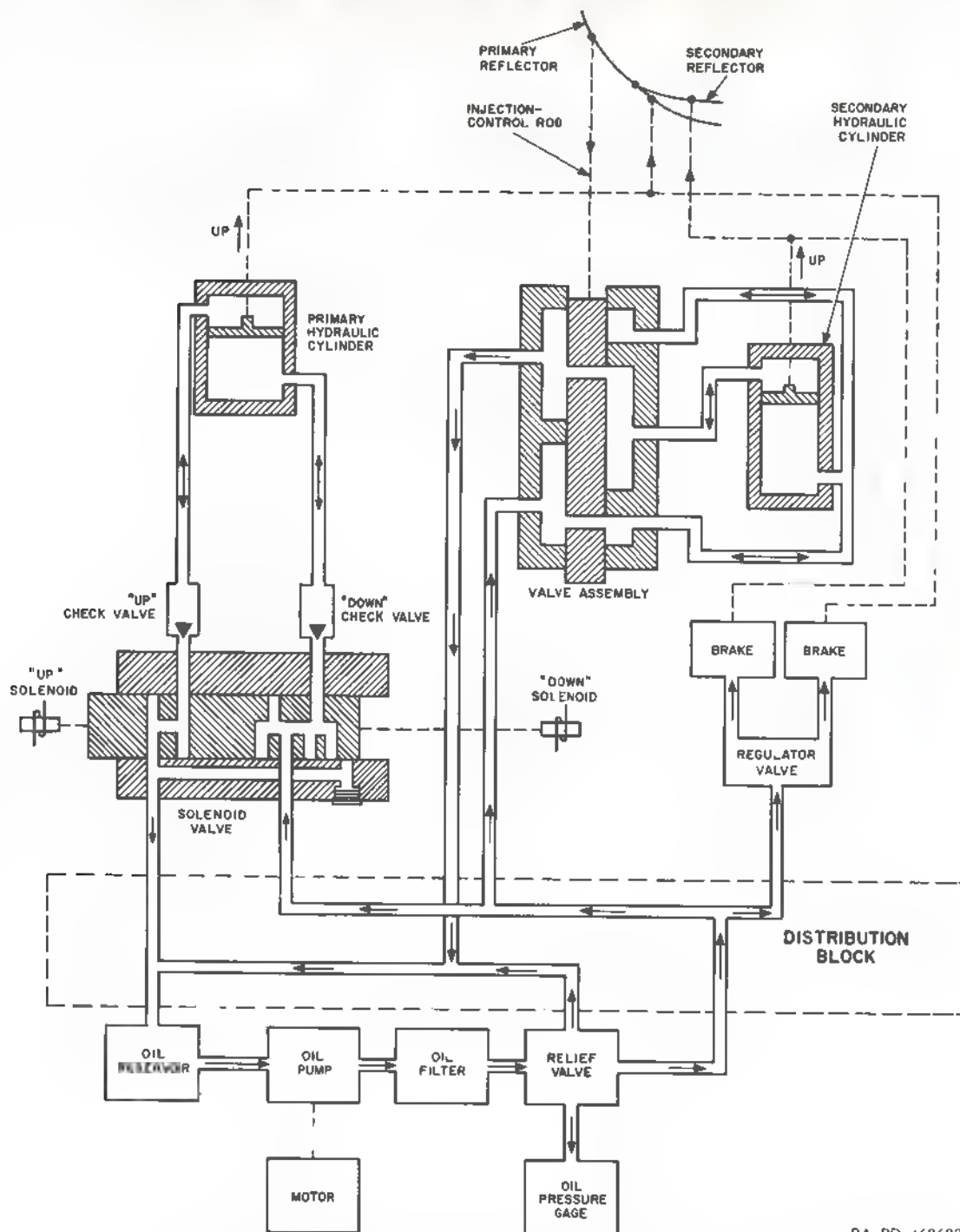
RA PD 468688

Figure 98. (U) Hydraulic system, simplified showing upward title of reflector assembly
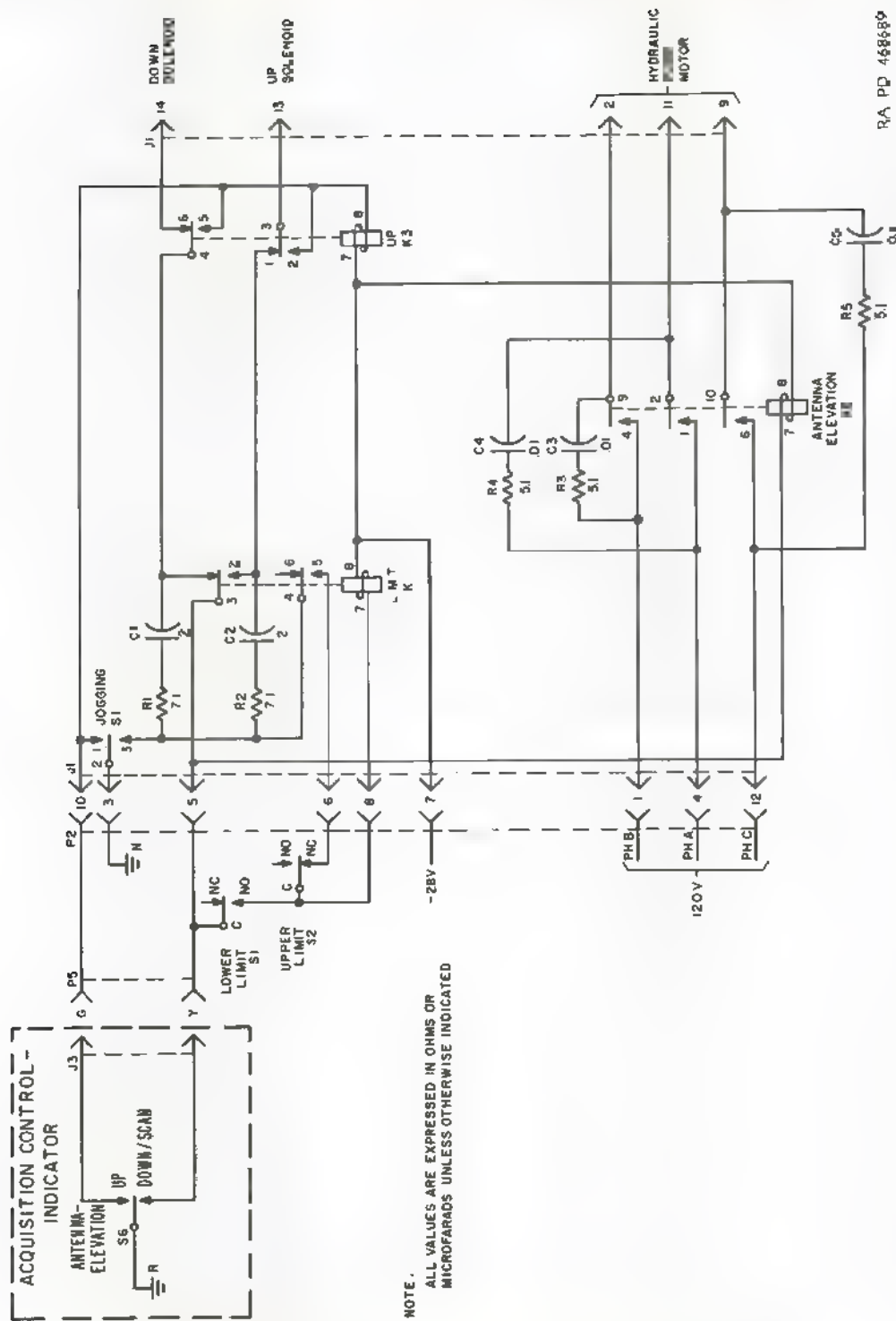
Figure 99. (U) Hydraulic control relay assembly and related circuits.

RA PD 468689

brakes to operate, thus locking the reflector assembly in the position reached at the time of switch release.

d. When S6 is placed in the DOWN/SCAN position, antenna elevation relay K2 is energized to start the hydraulic pump motor. At the same time, the "down" solenoid of the solenoid valve is energized by the ground applied through contacts of deenergized relays K1 and K3. The oil pressure, channeled to the primary hydraulic cylinder, at this time is in a direction which causes the reflector assembly to tilt downward. When the reflector assembly reaches a predetermined point, it causes the normally open lower limit switch to be operated to the closed position. In the closed position, the lower limit switch permits ground to be applied to K1, thus energizing K1. Contacts 1 and 3 of K1 open and contacts 2 and 3 of K1 close to deenergize the "down" solenoid and energize the "up" solenoid. With the "up" solenoid energized, the reflector assembly moves upward and permits the lower limit switch to be restored to its normally open condition. Relay K1 remains energized by virtue of the ground connection completed through holding contacts 4 and 5 and the contacts of the normally closed upper limit switch.

e. The reflector assembly tilts upward until it reaches a predetermined elevation, at which time it operates the upper limit switch, causing the switch to open. This deenergizes relay K1 and opens contacts 2 and 3 to deenergize the "up" solenoid. When K1 deenergizes, contacts 1 and 3 of K1 close to energize the "down" solenoid. Thus, the reflector assembly continues to automatically scan between elevation limits determined by the physical settings of the limit switches when S6 is in the DOWN/SCAN position.

f. Jogging switch S1, located on the underside of the hydraulic control unit, permits local control of reflector assembly elevation for purposes of checking mechanical function and making adjustments. When held in one or the other of its two operating positions, the jogging switch applies ground to energize either the "up" or "down" solenoid and at the same time activate the hydraulic system. The jogging switch, when used, bypasses the effect of the limit switches and per

mits maximum tilt of the reflector assembly. RC networks R1 C1, R2 C2, R3-C3, and R4-C4 prevent arcing across contacts of the relays in the hydraulic control relay assembly.

84. Vertical Scan and Elevation Coverage

a. Four vertical scan modes have been adopted for use in the acquisition antenna. Any of these four modes can be selected by making two adjustments in the hydraulic control unit of the antenna. The injection adjustment screw (fig 86), related to valve assembly operation, determines the elevation angle at which the secondary reflector is injected. The upper limit adjustment screws position the upper limit switch to set the upper limit of automatic vertical scan. The upper limit of elevation can be overridden when ANTENNA—ELEVATION scan switch S6 on the acquisition control-indicator is held manually in the UP position.

b The vertical scan mode selected for use depends on the terrain of the radar site and the expected altitude of enemy aircraft. The hydraulic system is capable of tilting the reflector assembly from a minimum angle of 0° to a relative maximum angle of 9°, where 0° is the position of the reflector assembly when fully depressed. Reflector assembly elevation is read on the 0° to 9° scale in the hydraulic control unit (fig. 86). At the 0° elevation, the reflector assembly transmits an RF beam, pencil-like in shape, whose axis (line through nose of beam and origin) forms a 2° angle with the horizontal. Thus, the beam angle is 2° when the reflector assembly angle is 0°. Each degree of increase in reflector assembly angle causes the beam angle to be increased by 2°. The beam angle is increased by an additional 2° when the secondary reflector is fully injected into the reflector assembly. The injection action is completed in 1° of reflector assembly tilt. Injection changes the beam from pencil shape to fan shape. The pencil-shaped beam provides long range, low elevation coverage; the fan-shaped (cosecant-squared) beam provides shorter range, but higher elevation coverage. The degree of tilt of the RF beam (beam angle) in mils is read on the ANTENNA—ELEVATION indicator located on the acquisition control-indicator. The reading on the

ANTENNA—ELEVATION indicator does not indicate the 2 additional degrees of elevation caused by secondary reflector injection.

c. The conditions for the four modes of vertical scan are described in (1) through (4) below. These scan modes plus data on related ANTENNA—ELEVATION indicator readings and area coverage are illustrated in figures 100 and 101.

(1) *Vertical scan mode No. 1 (A, fig. 100).* A pencil beam is radiated at reflector assembly angle−0° (beam angle−2°). Secondary reflector injection begins at this point and injection is completed at reflector assembly angle 1° (beam angle−6°). The 6° beam angle is obtained as follows: at reflector assembly angle =0, the beam angle is 2°; tilting the reflector assembly 1° elevates the beam 2°; and injection of the secondary reflector elevates the beam an additional 2°. Thus, the total beam angle is 6°. The upper limit of reflector assembly tilt in scan mode No 1 is 9° (beam angle 22°). The time for a complete up-and-down scan is approximately 40 seconds.

(2) *Vertical scan mode No 2 (B, fig. 100).* A pencil beam is radiated from reflector assembly angle=0° (beam angle−2°) to reflector assembly angle=2° (beam angle −6°) Secondary reflector injection begins at reflector assembly angle−2° and injection is completed at 3° (beam angle =10°). The upper limit of reflector assembly tilt in scan mode No. 2 is 4.5° (beam angle=13°). The time for a complete up-and-down scan is approximately 20 seconds.

(3) *Vertical scan mode No. 3 (A, fig. 101).* A pencil beam is radiated from reflector assembly angle−0° (beam angle −2°) to reflector assembly angle −4° (beam angle −10°). Secondary reflector injection begins at reflector assembly angle −4° and injection is completed at 5° (beam angle=14°). The upper limit of reflector assembly tilt in scan mode No. 3 is 6.5° (beam angle=17°). The time for

a complete up-and down scan is approximately 28 seconds.

(4) *Vertical scan mode No. 4 (B, fig. 101).* A pencil beam is radiated from reflector assembly angle−0° (beam angle=2°) to reflector assembly angle=6° (beam angle 14°). Secondary reflector injection begins at reflector assembly angle −6° and injection is completed at 7° (beam angle−18°). The upper limit of reflector assembly tilt in mode No. 4 is 9° (beam angle=22°). The time for a complete up-and-down scan is approximately 40 seconds.

85. Miscellaneous Antenna-Mounted Components

a. The regulator valve (fig. 83) is connected in series with the line supplying oil pressure to the brakes. The purpose of this regulator valve is to maintain sufficient oil pressure against the brake springs (figs. 84 and 85) to prevent brake operation during the time that automatic scan is taking place In automatic scan, the selector valve of the solenoid valve (fig. 93) passes through its center position as the "up" and "down" solenoids are alternately energized and deenergized. Each time this occurs, an unrestricted path for oil to the reservoir is completed. This momentarily lowers the oil pressure in the hydraulic system and, consequently, would lower the oil pressure against the brake springs were it not for the action of the regulator valve. The regulator valve traps the pressure and maintains it against the brake springs during the switch-over in the solenoid valve.

b. Synchro transmitter B1 (fig. 102) is mechanically geared to the primary reflector of the acquisition antenna and electrically connected to a synchro receiver located behind the acquisition control-indicator panel. The rotor of the synchro receiver drives the ANTENNA ELEVATION indicator located on the panel. This arrangement provides an indication in mils of the beam angle, neglecting the effect caused by injection of the secondary reflector. A complete discussion of synchro operation is contained in paragraph 47.

CONFIDENTIAL

SCAN MODE 1

REFLECTOR ASSEMBLY ANGLE -DEGREES

BEAM ANGLE - DEGREES

ANTENNA ELEVATION INDICATOR READING - MILS
(NOTE)

9 — UPPER LIMIT OF SCAN

356   22
20   7
15   5
10   3
71   5   1 — INJECTION COMPLETE
36   2   0 — INJECTION BEGINS

22 DEG

6 DEG

2 DEG

APPROX ALTITUDE - THOUSANDS OF FEET

240
160
80
0

0   178,000   250,000
       166,000

APPROX RANGE - YARDS

A
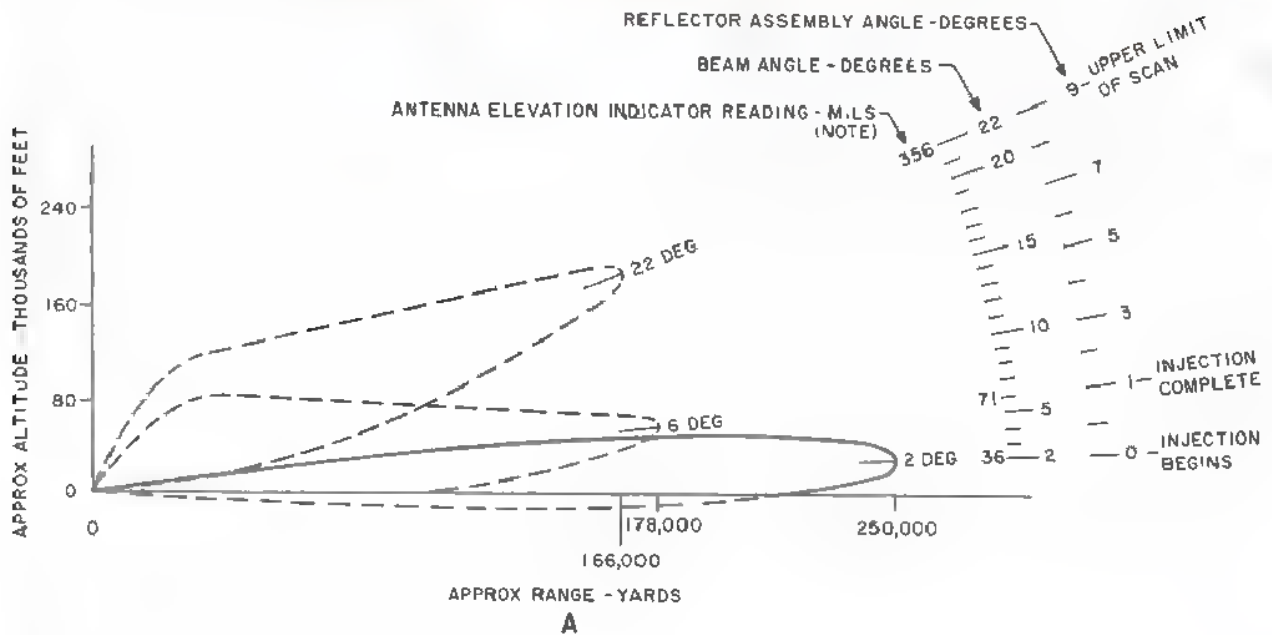
NOTE.

THE READING ON THE ANTENNA–ELEVATION
INDICATOR DOES NOT INCLUDE THE 2 ADDITIONAL
DEGREES OF ELEVATION CAUSED BY SECONDARY
INJECTION

SCAN MODE 2

REFLECTOR ASSEMBLY ANGLE - DEGREES

BEAM ANGLE - DEGREES

ANTENNA ELEVATION INDICATOR READING - MILS
(NOTE)

9
22
20   7
15   5   4 5 — UPPER LIMIT OF SCAN
196   3 — INJECTION COMPLETE
142   10   2 — INJECTION BEGINS
106   5
36   2   0

13 DEG
10 DEG
6 DEG
2 DEG

APPROX ALTITUDE - THOUSANDS OF FEET

240
160
80
0

0   176,000   250,000

APPROX RANGE - YARDS

B
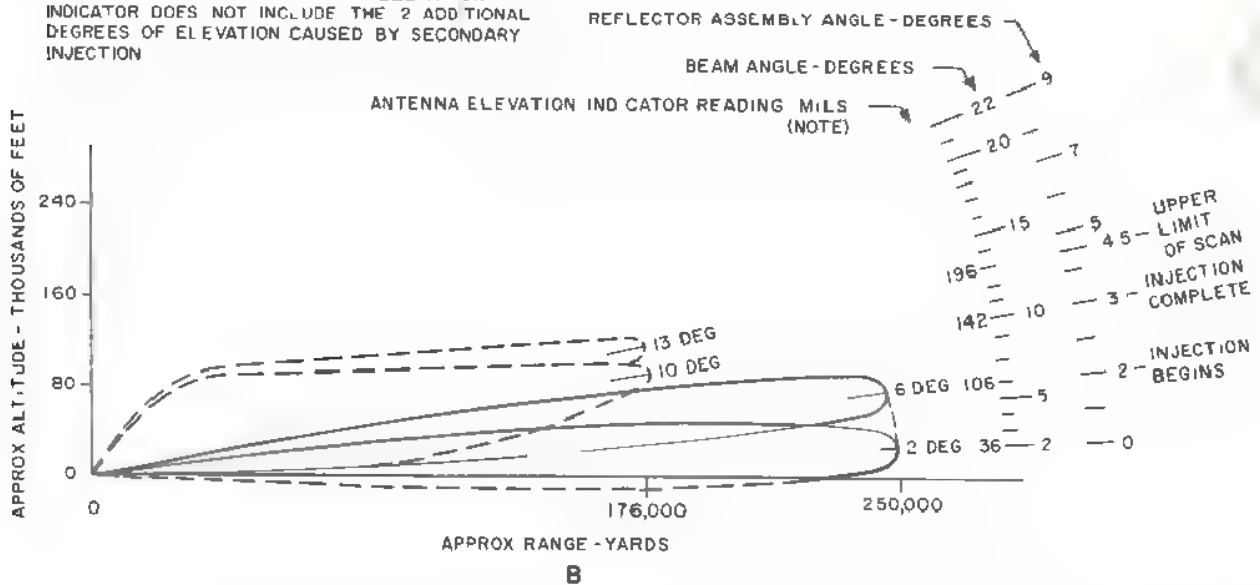
RA PD 468690

Figure 100. (U) Vertical scan modes No. 1 and No 2—elevation coverage.

232

SCAN MODE 3

REFLECTOR ASSEMBLY ANGLE - DEGREES

BEAM ANGLE - DEGREES

ANTENNA ELEVATION INDICATOR READING - MLS (NOTE)

APPROXIMATE ALTITUDE THOUSANDS OF FEET

240

160

80

0

17 DEG
14 DEG
10 DEG
2 DEG

9

22
20
65   7   UPPER LIMIT
                OF SCAN
267   15   5   INJECTION
        14   COMPLETE
214
                4   INJECTION
178   10   BEGINS

                2

        5

36   2   0

0

APPROXIMATE RANGE   YARDS
174,000   250,000

SCAN MODE 4

REFLECTOR ASSEMBLY ANGLE - DEGREES

BEAM ANGLE - DEGREES

ANTENNA ELEVATION INDICATOR READING - MLS (NOTE)

APPROXIMATE ALTITUDE - THOUSANDS OF FEET

240

160

80

0

22 DEG
18 DEG
14 DEG
2 DEG

9   UPPER LIMIT
        OF SCAN
356   22
        20   7   INJECTION
                    COMPLETE
278
                    INJECTION
249   15   6   BEGINS
        14
        10   4

                2

        5

36   2   0

0

APPROXIMATE RANGE - YARDS
169,000   250,000

B

NOTE

THE READING ON THE ANTENNA-ELEVATION
INDICATOR DOES NOT INCLUDE THE TWO ADD-
TIONAL DEGREES OF ELEVATION CAUSED BY
SECONDARY INJECTION.

RA PD 468691

Figure 101 (U). Vertical scan modes No. 3 and No. 4 elevation coverage.
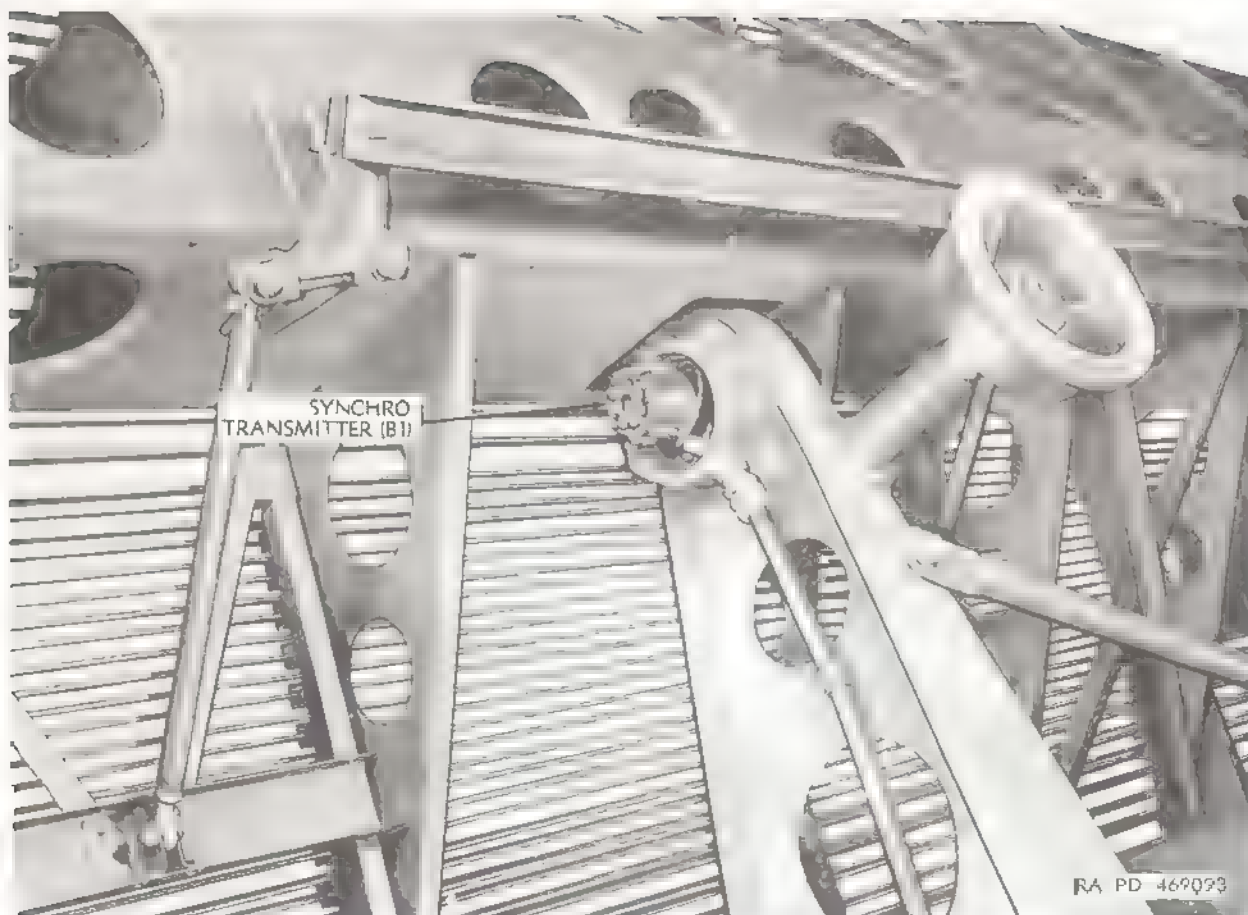
Figure 102 (U). Acquisition antenna—left rear view showing synchro transmitter.

86 (U). Acquisition Electro-Mechanical Vertical Scan System

a. General.

(1) Beginning with system 1071, the hydraulic control unit of the acquisition antenna is replaced by the electromechanical unit to provide the vertical scan function. Hydraulic control u. 8607284 is replaced by electro-mechanical control box 9007806 (fig. 103). Hydraulic control relay assembly 7612085, a part of the hydraulic control unit, is replaced by electromechanical control panel 9154368 in systems 1071 through 1306. In systems 1307 through 1362, electro-mechanical control panel 9988941 is used. Primary hydraulic cylinder 8011416 is replaced by primary actuator 8159580 (fig. 104) in systems 1071 and up. Secondary hydraulic cylinder 8011415 is replaced by secondary actuator 8159579. The hydraulic oil lines are replaced by electrical cables for interconnecting the actuators and control box.

(2) Due to the foregoing modifications, acquisition antenna
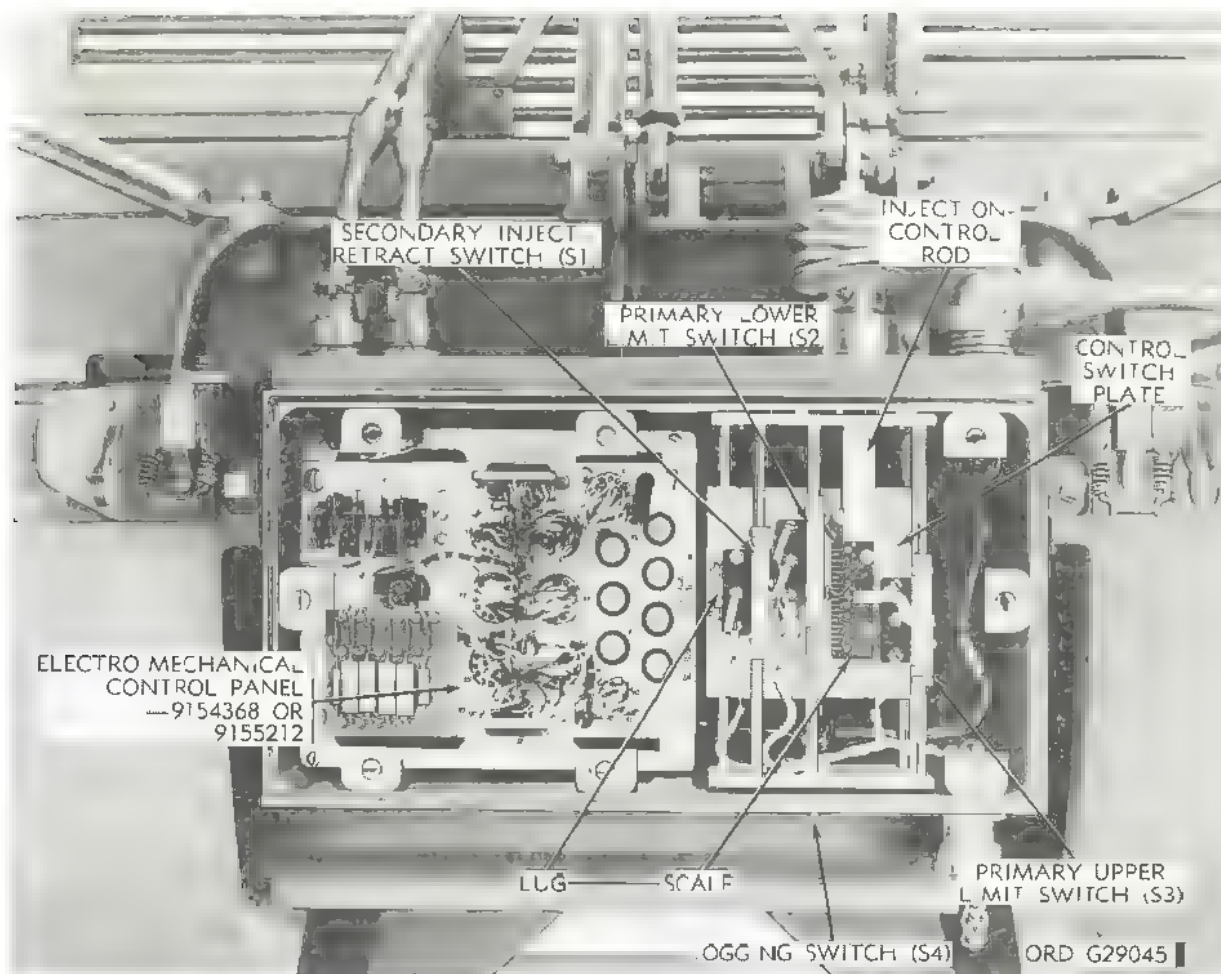
Figure 103. (U) Electro - mechanical control box 9007806 - internal view.

9000289 is modified to acquisition antenna 8158132. As with the old antenna, elevation of the new acquisition antenna is controlled by ANTENNA—ELEVATION scan switch S6 on the acquisition control-indicator of the battery control console. The new and old antennas are identical in construction, and information in paragraph 84 on vertical scan modes and elevation coverage pertains equally to both antennas.

(3) In the new scan system an electrical means is used for determining the point in the scan cycle when injection and retraction of the secondary reflector occurs. Secondary inject-retract switch S1 (fig. 103), mounted to the left of primary upper limit switch S2 and primary lower limit switch S3 in the control box, is operated by the control switch plate connected to the injection control rod. The control switch plate has a horizontal lug and moves in a direction opposite to that of primary reflector tilt. Movement of the control switch plate
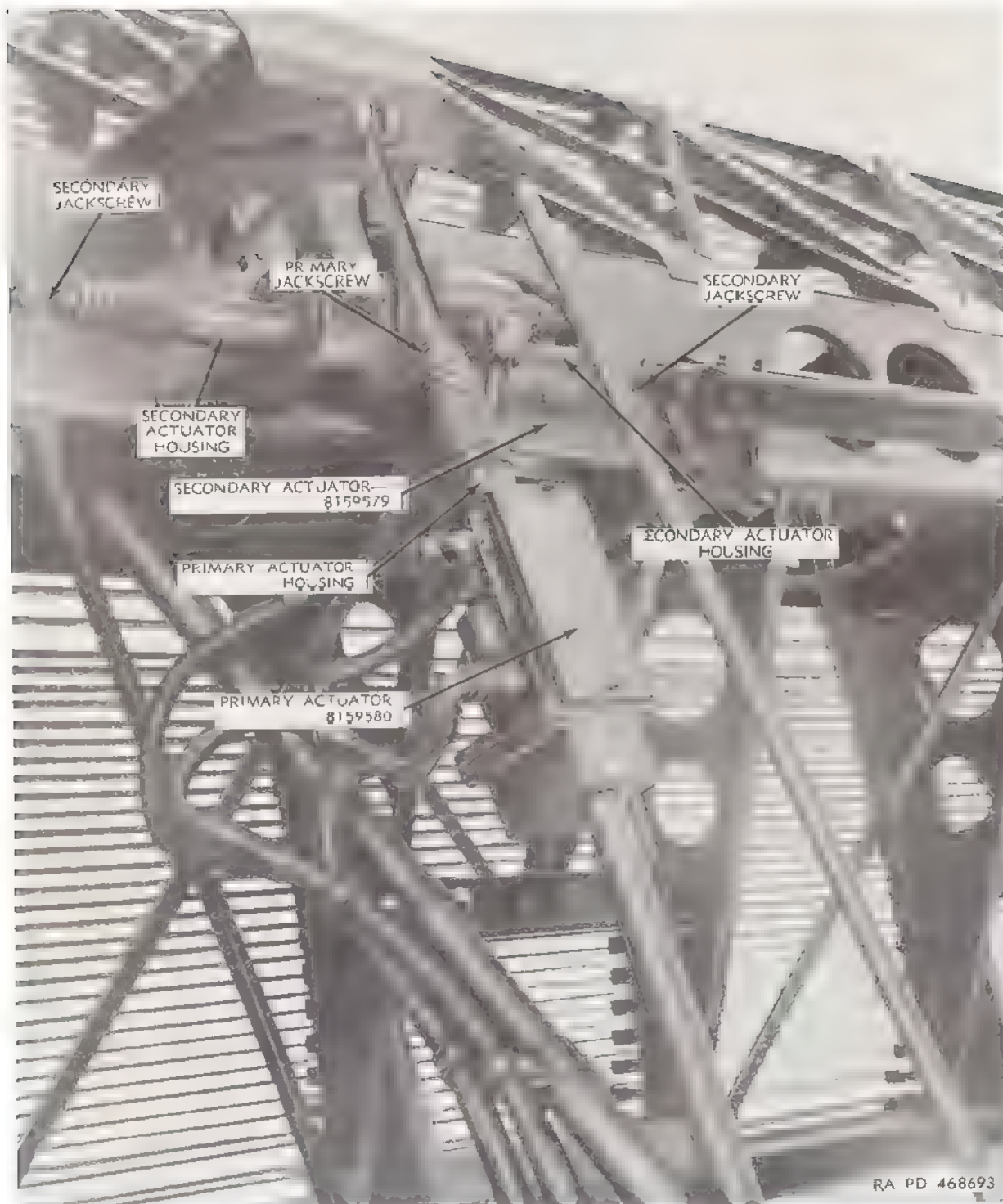
Figure 104.   (U) Acquisition antenna 8158132—partial rear view—radome removed.

causes the lug to operate S1 in addition to S2 and S3 during each complete vertical scan cycle. The effect obtained in operating S1 is analogous to that obtained in the old system wherein the injection control rod operated the adjustable valve assembly to cause injection and retraction of the secondary reflector (par. 82c(9)).

b. Primary Actuator 8159580. The primary actuator (fig. 104) used in the new system consists of a 3-phase, 120-volt, 400-cps motor that is geared to a jackscrew mechanically coupled to the primary reflector. As the motor turns, the jackscrew moves in or out of the actuator housing to tilt the primary reflector down or up, respectively, depending on the direction of motor rotation. The actuator housing also contains two momentary-contact normally closed sensitive switches termed primary up safety switch S2 and primary down safety switch S1, respectively. The safety switches protect the actuator motor from burnout at the extreme limits of primary reflector travel.

c. Secondary Actuator 8159579. The secondary actuator (fig. 104) is identical to the primary actuator, except that the jackscrew of the secondary actuator extends from both ends of the actuator housing to permit lateral pressure to be applied simultaneously to both halves of the secondary-reflector control linkage. The secondary actuator contains four momentary-contact normally closed sensitive switches. Two switches, termed secondary inject safety switch S2 and secondary retract safety switch S3, respectively, protect the actuator motor from burnout at the extreme limits of secondary reflector travel. The remaining two switches are termed secondary inject limit switch S1 and secondary retract limit switch S4, respec-

tively. These two limit switches are preset at the factory to a physical position which permits them to define normal operating limits of secondary reflector travel in a manner similar to that in which switches S2 and S3 in the control box define normal operating limits of primary reflector travel.

d. Electro-Mechanical Control Box 9007806 Using the Electro-Mechanical Control Panel - 9154368. The electro-mechanical control box (fig. 103) contains the electro-mechanical control panel 9154368, primary lower limit switch S2, secondary inject-retract switch S1, primary upper limit switch S3, the 0 to 9° scale, the control switch plate, and jogging switch S4. The electro-mechanical control panel consists of twelve relays, a 100-volt dc power supply, and seven fuses. Six of the twelve relays form a group which controls the operation of the primary reflector by controlling the operation of the primary actuator motor. The remaining six relays form a second group which controls the operation of the secondary reflector by controlling the operation of the secondary actuator motor. In each relay group, two relays control the tilt of the reflector associated with the group. The remaining four relays in each group act as a brake unit. Each brake unit controls and times the application of 100 volts dc to windings of the actuator motor with which the brake unit is associated. The application of 100 volts dc to an actuator motor occurs automatically when 3-phase ac driving power is removed from the respective motor. Three-phase ac driving power is removed from the motor when the two relays which control motor operation (reflector tilt) are deenergized. Deenergizing the two motor control relays of either relay group completes a path for energizing the brake unit of that group.

Note. The key letter-number com-
binations shown in parentheses in e
and f below refer to figure 105 unless
otherwise indicated.

e. "Up" Operation Using the Electro-
Mechanical Control Panel - 9154368.

(1) Primary actuator motor B3.
When ANTENNA—ELEVATION
scan switch S6 (B1) on the ac-
quisition control-indicator is
manually held in the UP posi-
tion, ground is applied through
connector P1-A (C2) to ener-
gize primary up relay K11 in
the electro-mechanical control
panel. The current path for
energizing K11 is from -28 volts
through connector P1-I (C2)
through contacts 5-15 of de-
energized primary down relay
K10, primary up safety switch
S2, solenoid of K11, contacts
7-16 of deenergized K10, and
contacts 2-1 of S6 to ground.
With K11 energized, 3-phase
ac power is applied to the wind-
ings of the primary actuator
motor. Phase A is applied
through connector P1-J (A2),
fuse F5, and contacts 7-16 of
deenergized primary braking
relay K8 to one winding of pri-
mary actuator motor B3. Phase
B is applied through connector
P1-H (A2), contacts 13-2 of
energized K11, fuse F1, and
contacts 14-3 of deenergized
K8 to the second winding of B3.
Phase C is applied through con-
nector P1-C (A2), contacts 14-4
of energized K11, fuse F7, and
contacts 1-13 of deenergized K8
to the third winding of B3. With
3-phase power thus applied to
B3, the motor rotates in a di-
rection which causes the pri-
mary reflector (and hence the
entire reflector assembly) to

tilt upward. With switch S6 held
in the UP position, the reflectors
continue to tilt upward until
their limits are reached and re-
main there.

(2) Secondary actuator motor B2.
As the primary reflector is
driven upward, the injection
control rod (fig. 103) causes the
control switch plate to be driven
downward. At a predetermined
time, depending on the scan
mode (physical position of sec-
ondary inject-retract switch
S1), the lug on the control switch
plate momentarily closes S1.
At this instant, S1 (C4) com-
pletes the path of the -28-volts
to the solenoid of secondary
inject relay K12, thereby ener-
gizing K12. The current path for
energizing K12 is from -28
volts through P1-I (C2), sec-
ondary inject-retract switch
S1, secondary inject limit switch
S1, secondary inject safety
switch S2, contacts 1-13 of de-
energized secondary retract re-
lay K9, solenoid of K12, contacts
7-16 of deenergized primary
down relay K10, and S6-2 and
1 to ground. Holding contacts
14-4 of energized K12 maintain
K12 energized after the lug of
the control switch plate (fig.
103) has passed S1 and is on
the way toward S2. With K12
(C6) energized, 3-phase ac
power is applied to the wind-
ings of secondary actuator
motor B2. Phase A is applied
through connector P1-J (A2),
fuse F6, contacts 9-17 of de-
energized secondary braking
relay K6, and contacts 6-15 of
energized K12 to one winding
of B2. Phase B is applied through
connector P1-H (A2), contacts
17-10 of energized K12, fuse

electro-mechanical scan circuit - functional schematic diagram.

ORD G22918

Figure 105. (U) Acquisition antenna – elevation electro-mechanica

7 | 8 | 9 | 10 | | | 12 | 13 | 14 |

ISITION ANTENNA —8158132
CHANICAL CONTROL BOX —9007806
HANICAL CONTROL PANEL —9155212

PRIMARY ACTUATOR —8159580

B3 PRIMARY ACTUATOR
NEUTRAL MOT

SECONDARY ACTUATOR —8159579

B2 SECONDARY ACTUATOR
NEUTRAL MOT

S2 SECONDARY INJECT SAFETY
S1 SECONDARY INJECT-LIMIT
S3 SECONDARY RETRACT SAFETY
S4 SECONDARY RETRACT-LIMIT

PRIMARY ACTUATOR —8159580

S PRIMARY DOWN SAFETY
S2 PRIMARY UP SAFETY

B ELEVATION TRANSMITTER SYNCHRO

C3 0.047
R3 30
C4 0.047
R4 30
C 0.047
R1 130
C2 0.047
R2 130

YEL
RED CR1 BLK T1
YEL

R8 430
C5B 6

R5 6800
R6 6800

K6 SECONDARY INJECT 240
K1 SECONDARY BRAKING 5000
K2 PRIMARY BRAKING 5000

P1

J3 J4 J3 J5

ORD G23729

na – elevation electro-mechanical scan circuit - functional schematic diagram.

Figure 105.1 (U) Acquisition antenna – elevation electro-mechanical scan circuit – functional schematic

F4, and contacts 5-15 of deenergized K6 to the secondary winding of B2. Phase C is applied through connector P1-C (A2), contacts 12-18 of energized K12, fuse F2, and contacts 14-3 of deenergized K6 to the third winding of B2. With 3-phase power thus applied, to motor B2, the motor rotates in a direction which causes the secondary reflector to be injected.

(3) Secondary inject limit switch S1. Secondary reflector injection is completed during a particular one degree of primary reflector upward tilt as determined by the preselected scan mode. Motor B2 rotates until the internal mechanism of the actuator opens normally closed momentary-contact secondary inject limit switch S1 in the secondary actuator. At this point in the upward tilt of the reflector assembly, the secondary reflector is fully injected. Opening S1 deenergizes K12 to remove ac driving power from B2. This energizes the secondary brake unit.

(4) Secondary braking relay K6 and hold relay K5. The secondary brake unit is comprised of secondary braking relay K6, secondary timing relay K2A, secondary timing relay K2B, and secondary hold relay K5. The action of the brake unit and the energization path is discussed in g below. With the secondary reflector fully injected, the reflector assembly continues to be driven upward by primary actuator motor B3 until the internal mechanism of the actuator opens normally closed, momentary-contact, primary up safety switch S2. At this time

the reflector assembly is at maximum elevation. Opening the primary up safety switch deenergizes K11 to remove ac driving power from primary actuator motor B3. This energizes the primary brake unit.

(5) Primary brake relay K8 and hold relay K7. The primary brake unit is comprised of primary braking relay K8, primary timing relay K1A, primary timing relay K1B, and primary hold relay K7. The action of the primary brake unit and energization path is described in g below. It should be noted that in the "up" operation (S6 manually held in the UP position), the action of primary upper limit switch S3 has no effect on circuit operation even though it is operated by the lug of the control switch plate. However, in the "down/scan" operation discussed in f below, S3 determines the upper limit of reflector assembly tilt.

f. "Down/Scan" Operation Using the Electro-Mechanical Control Panel - 9154368.

(1) Primary actuator motor B3. When ANTENNA—ELEVATION scan switch S6 is placed in the DOWN/SCAN position, ground is applied through primary lower limit switch S2 to energize primary down relay K10 in the control panel. The current path for energizing K10 is from -28 volts through connector P1-I (C2), contacts 15-5 of deenergized primary up relay K11, primary down safety switch S1, solenoid of K10, contacts 9-17 of deenergized K11, contacts of unoperated S2, and contacts 2-3 of S6 to ground. With K10 energized, 3-phase ac power is ap-

in the actuator. At this point in the downward tilt of the reflector assembly, the secondary reflector is fully retracted. Opening secondary retract limit switch S4 breaks the holding circuit through contacts 18-12 of K9. This allows K9 to deenergize removing ac driving power from the secondary actuator motor. This energizes the secondary brake unit. The action of the secondary brake unit is described in g below.

(4) <u>Primary lower limit switch S2 and primary upper limit switch S3.</u> With the secondary reflector fully retracted, the reflector assembly continues to be driven downward by primary actuator motor B3 until the lug of the control switch plate reaches and operates primary lower limit switch S2. Relay K10 is thereby deenergized and the -28-volt circuit for operating the primary brake unit is completed for a brief moment through contacts 18-11 of deenergized relays K10 and K11. With S2 operated, ground is applied through S2 and contacts 16-7 of deenergized K10 to energize K11. Ground is also applied through J2-4 to contact 16 of K11. With K11 energized, 3-phase ac power is applied to the primary actuator motor in the manner described in e above, and the up operation is initiated. As the reflector assembly starts to tilt upward the lug of the control switch plate starts to move downward, returning S2 to the unoperated position and braking the ground connection to K11. However, holding contacts 16-8 of energized K11 maintain the relay

energized by continuing the ground path from contact 16 through unoperated primary upper limit switch S3, connector P2-5, and contacts 16-7 of deenergized K10 to the solenoid of K11. Thus, the reflector assembly is permitted to be driven upward until the lug of the control switch plate operates S3. When S3 is operated, it breaks the ground connection to K11, causing K11 to be deenergized. When K11 is deenergized, contacts 17-9 complete a path for ground through unoperated S2, J2-10 to energize K10. For the brief moment preceding the energization of K10, the primary brake unit operates. With K10 again energized, ac power is applied to primary actuator motor B3 and the reflector scans downward. The reflector assembly is driven downward until S2 is operated. The entire cycle repeats until stopped by placing S6 in the center position.

g. Brake Units Using the Electro-Mechanical Control Panel - 9154368.

(1) As mentioned in d above, there are two brake units for stopping motor rotation, one for primary actuator motor B3 and one for secondary actuator motor B2. The primary actuator brake unit consists of solenoid type relays K7 and K8, and thermal-type relays K1A and K1B. The secondary brake unit consists of solenoid-type relays K2A and K2B, and thermal-type relays K1 and K3. A brake unit is activated from the moment the -28-volt supply circuit is completed to the heating elements of the thermal relays of the particular brake

gizing K5 closes contacts 13-2 and 14-4 of K5. Relay K5 is held energized through holding contacts 14-4 until the —28 volts is removed from the brake circuit. The energizing of K5 marks the end of the heating cycle and the beginning of the cooling cycle of K2A and K2B because contacts 14-3 of K5 are opened and the —28 volts is removed from the heating elements of K2A and K2B. Immediately after the cooling cycle begins, K2B deenergizes. However, this has no immediate effect since K5 is held energized by holding contacts 14-4. Some time later K2A opens, breaking the —28-volt circuit to K6, allowing K6 to deenergize. The deenergizing of K6 removes the 100-volt dc braking voltage from B2, completing the braking cycle. The circuit remains in this condition until the —28 volts is removed from the brake circuit by energizing K9 or K12. When either K9 or K12 is energized, the —28 volts is removed by the opening of contacts 17-9 and 16-7, respectively. Removing the —28 volts allows K5 to deenergize, rendering the brake circuit ready for the next braking cycle.

h. Electro-Mechanical Control Box 9007806 Using Electro-Mechanical Control Panel 9988-941. The electro-mechanical control box (fig. 103) contains electro-mechanical control panel 9988941, primary lower limit switch S2, secondary inject-retract switch S1, primary upper limit switch S3, the 0 to 9-degree scale, the control switch plate, and jogging switching S4 The electro-mechanical control panel consists of six relays, a 100-volt dc power supply, and four fuses. Three of the six relays form a group which controls the operation of the primary reflector by controlling the operation of the primary actuator motor, The remaining three relays form a second group which controls the operation of the secondary reflector by controlling the operation of the secondary actuator motor. In each relay group, two relays control the tilt of the reflector associated with the group. The remaining relay in each group acts as a brake unit. Each brake unit controls and times the application of 100 volts dc to windings of the actuator motor with which the

brake unit is associated. The application of 100 volts dc to an actuator motor occurs automatically when 3-phase ac driving power is removed from the respective motor. Three-phase ac driving power is removed from the motor when the two relays which control motor operation (reflector tilt) are deenergized. Deenergizing the two motor control relays of either relay group completes a path for energizing the brake unit of that group.

Note The key letter-number combinations shown in parentheses in *i* and *j* below refer to figure 105.1 unless otherwise indicated.

i. "Up" Operation Using Electro-Mechanical Control Panel 9988941.

(1) *Primary actuator motor B3.* When ANTENNA — ELEVATION scan switch S6 (B1) on the acquisition control-indicator is manually held in the UP position, ground is applied through connector P1-A (C2) to energize primary up relay K5 in the electro-mechanical control panel. The current path for energizing K5 is from —28 volts through connector P1-I (C2) through contacts 5-15 of deenergized primary down relay K4, primary up safety switch S2, solenoid of K5, contacts 7-16 of deenergized K4, and contacts 2-1 of S6 to ground. With K5 energized, 3-phase ac power is applied to the windings of the primary actuator motor. Phase A is applied through connector P1-J (A2), fuse F4, and contacts 12-18 of energized primary up relay K5 to one winding of primary actuator motor B3. Phase B is applied through connector P1-H (A2), fuse F1, contacts 13-2 of primary up relay K5, contacts 1-3 of deenergized K2 to the second winding of B3. Phase C is applied through connector P1-C (A2), fuse F2, contacts 4-14 of energized K5, and contacts 6-4 of deenergized K2 to the third winding of B3. With 3-phase power thus applied to B3, the motor rotates in a direction which causes the primary reflector (and hence the entire reflector assembly) to tilt upward. With switch S6 held in the UP position, the reflectors

for energizing K4 is from –28 volts through connector P1-I (C2), primary down safety switch S1, solenoid of K4, contacts 9-17 of deenergized K5, contacts of unoperated S2, and contacts 2-3 of S6 to ground. With K4 energized, 3-phase ac power is applied to the windings of primary actuator motor B3 so that connections to the motor for phase B and phase C are interchanged with respect to connections described for the primary up operation in *i* above. The connection of phase A remains the same as described in *i* above. Phase B is applied through connector P1-H (A2), fuse F1, contacts 17-10 of energized K4, and contacts 6-4 of deenergized K2 to the third winding of B3. Phase C is applied through connector P1-C (A2), fuse F2, contacts 14-4 of energized K4, and contacts 1-3 of deenergized K2 to the second winding of B3. With 3-phase power thus applied to primary actuator motor B3, the motor rotates in a direction opposite to that described in *i* above, causing the primary reflector (and hence the entire reflector assembly) to tilt downward.

(2) *Secondary actuator motor B2.* As the primary reflector is driven downward, the injection control rod (fig. 103) causes the control switch plate to be driven upward. When the plate is driven up to the point where the lug on the plate alines itself with secondary inject-retract switch S1, S1 closes momentarily. At this instant, S1 (C3) completes the path of the –28 volts to the solenoid of secondary retract relay K3, thereby energizing K3. The current path for energizing K3 is from –28 volts through connector P1-I (C2), switch S1, secondary retract limit switch S4, secondary retract safety switch S3, contacts 1-13 of deenergized secondary inject relay K6, solenoid of K3, contacts 17-9 of deenergized primary up relay K5, unoperated S2, and contacts 3-2 of S6 to ground. Holding contacts 18-12 of energized K3 maintain K3 energized

after the lug (fig. 103) of the control switch plate has passed S1 and is on the way toward S3. With K3 (C5) energized, 3-phase ac power is applied to the windings of motor B2 so that connections to the motor for phase B and phase C are interchanged with respect to connections described for the secondary up operation in *i* above. Phase A is applied through connector P1-J (A2), fuse F4, and contacts 8-16 of energized K3 to one winding of motor B2. Phase B is applied through connectors P1-H (A2), fuse F1, contacts 15-6 of energized K3, and contacts 6-4 of deenergized K1 to the third winding of motor B2. Phase C is applied through connector P1-C (A2), fuse F2, contacts 4-14 of energized K3, fuse F4, and contacts 1-3 of deenergized K1 to the second winding of motor B2. With 3-phase power thus applied to B2, the motor rotates in a direction opposite that described in *i* above, causing the secondary reflector to retract.

(3) *Secondary retract limit switch S4.* Secondary reflector retraction, like injection, is completed during the same particular one-degree movement of the primary reflector. Secondary actuator motor B2 rotates until the internal mechanism of the actuator opens normally-closed momentary-contact secondary retract limit switch S4 in the actuator. At this point in the downward tilt of the reflector assembly, the secondary reflector is fully retracted. Opening secondary retract limit switch S4 breaks the holding circuit through contacts 18-12 of K3. This allows K3 to deenergize removing ac driving power from the secondary actuator motor. This energizes the secondary brake unit. The action of the secondary brake unit is described in *k* below.

(4) *Primary lower limit switch S2 and primary upper limit switch S3.* With the secondary reflector fully retracted, the reflector assembly continues to be driven downward by primary actuator

brake unit. The complete explanation of secondary brake unit operation follows in (4) and (5) below.

(4) When secondary retract relay K3 is energized, capacitor C5A is charged to 100 volts by the 100-volt dc power supply through contacts 17-10 of energized relay K3 and resistor R7. When K3 is deenergized, capacitor C5A discharges through resistor R7, contacts 17-9 of deenergized relay K3, contacts 16-7 of deenergized relay K6, resistor R5, and the solenoid of secondary braking relay K1, thus energizing relay K1 until capacitor C5A is discharged. Energized relay K1 connects the 100-volt dc braking voltage to secondary actuator motor B2 through contacts 5-4 and 2-3 of relay K1. The braking voltage stops the rotation of motor B2. The braking voltage is removed when relay K1 is deenergized, thus rendering the brake unit ready for the next brake cycle.

(5) When secondary inject relay K6 is energized, capacitor C5A is charged to 100 volts by the 100-volt dc power supply through contacts 16-8 of energized relay K6, contacts 17-9 of deenergized relay K3, and resistor R7. When K6 is deenergized, capacitor C5A discharges through resistor R7, contacts 17-9 of deenergized relay K3, contacts 16-7 of deenergized relay K6, resistor R5, and the solenoid of secondary braking relay K1, thus energizing relay K1 until capacitor C5A is discharged. Energized relay K1 then applies the braking voltage to secondary actuator motor B2 as explained in (4) above. The braking voltage is

removed when relay K1 is deenergized, thus rendering the brake unit ready for the next braking cycle.

(6) Semiconductor diode CR2 isolates the primary and secondary braking relays to prevent interaction between the primary and secondary brake units.

86.1 (U). Acquisition Antenna 9156580

a. *General.* Acquisition antenna 9156580 is identical to acquisition antenna 8158132 except for the addition of the auxiliary acquisition antenna added by DA MWO 9-1400-268-50.

b. *Detailed Theory.*

(1) The auxiliary acquisition antenna is mounted on the radome and is connected to rotary coupler 9156621 through a rigid coaxial transmission line.

(2) The auxiliary antenna is a modified gage and has a carefully tailored antenna pattern. The auxiliary antenna is a receiving antenna only. The patterns of the acquisition antenna and the auxiliary acquisition antenna are matched in the horizontal and vertical planes. The antenna pattern of the auxiliary acquisition antenna coincides with that of the normal acquisition antenna except for the main lobe. If the proper signal gains exist in each receiver channel, the power output of the auxiliary receiver channel is greater than the power output of the main receiver channel except when a signal source lies along the axis of the main lobe of the acquisition pattern. Thus, the precise azimuth of the signal source can be determined.

F4, and contacts 5-15 of deenergized K6 to the secondary winding of B2. Phase C is applied through connector P1-C (A2), contacts 12-18 of energized K12, fuse F2, and contacts 14-3 of deenergized K6 to the third winding of B2. With 3-phase power thus applied, to motor B2, the motor rotates in a direction which causes the secondary reflector to be injected.

(3) Secondary inject limit switch S1. Secondary reflector injection is completed during a particular one degree of primary reflector upward tilt as determined by the preselected scan mode. Motor B2 rotates until the internal mechanism of the actuator opens normally closed momentary-contact secondary inject limit switch S1 in the secondary actuator. At this point in the upward tilt of the reflector assembly, the secondary reflector is fully injected. Opening S1 deenergizes K12 to remove ac driving power from B2. This energizes the secondary brake unit.

(4) Secondary braking relay K6 and hold relay K5. The secondary brake unit is comprised of secondary braking relay K6, secondary timing relay K2A, secondary timing relay K2B, and secondary hold relay K5. The action of the brake unit and the energization path is discussed in g below. With the secondary reflector fully injected, the reflector assembly continues to be driven upward by primary actuator motor B3 until the internal mechanism of the actuator opens normally closed, momentary-contact, primary up safety switch S2. At this time

the reflector assembly is at maximum elevation. Opening the primary up safety switch deenergizes K11 to remove ac driving power from primary actuator motor B3. This energizes the primary brake unit.

(5) Primary brake relay K8 and hold relay K7. The primary brake unit is comprised of primary braking relay K8, primary timing relay K1A, primary timing relay K1B, and primary hold relay K7. The action of the primary brake unit and energization path is described in g below. It should be noted that in the "up" operation (S6 manually held in the UP position), the action of primary upper limit switch S3 has no effect on circuit operation even though it is operated by the lug of the control switch plate. However, in the "down/scan" operation discussed in f below, S3 determines the upper limit of reflector assembly tilt.

f. "Down/Scan" Operation Using the Electro-Mechanical Control Panel - 9154368.

(1) Primary actuator motor B3. When ANTENNA—ELEVATION scan switch S6 is placed in the DOWN/SCAN position, ground is applied through primary lower limit switch S2 to energize primary down relay K10 in the control panel. The current path for energizing K10 is from -28 volts through connector P1-I (C2), contacts 15-5 of deenergized primary up relay K11, primary down safety switch S1, solenoid of K10, contacts 9-17 of deenergized K11, contacts of unoperated S2, and contacts 2-3 of S6 to ground. With K10 energized, 3-phase ac power is ap-

plied to the windings of primary actuator motor B3 so that connections to the motor for phase B and phase C are interchanged with respect to connections described for the primary up operation in e above. The connection of phase A remains the same as described in e above. Phase B is applied through connector P1-H (A2), contacts 17-10 of energized K10, fuse F7, and contacts 1-13 of deenergized K8 to the third winding of B3. Phase C is applied through connector P1-C (A2), contacts 14-4 of energized K10, fuse F1, and contacts 14-3 of deenergized K8 to the second winding of B3. With 3-phase power thus applied to primary actuator motor B3, the motor rotates in a direction opposite to the described in e above, causing the primary reflector (and hence the entire reflector assembly) to tilt downward.

(2) Secondary actuator motor B2. As the primary reflector is driven downward, the injection control rod (fig. 103) causes the control switch plate to be driven upward. When the plate is driven up to the point where the lug on the plate alines itself with secondary inject-retract switch S1, S1 closes momentarily. At this instant, S1 (C3) completes the path of the -28 volts to the solenoid of secondary retract relay K9, thereby energizing K9. The current path for energizing K9 is from -28 volts through connector P1-I (C2), switch S1, secondary retract limit switch S4, secondary retract safety switch S3, contacts 1-13 of deenergized secondary inject relay K12, solenoid of K9, contacts 17-9 of de-

energized primary up relay K11, unoperated S2, and contacts 3-2 of S6 to ground. Holding contacts 18-12 of energized K9 maintain K9 energized after the lug (fig. 103) of the control switch plate has passed S1 and is on the way toward S3. With K9 (C5) energized, 3-phase ac power is applied to the windings of motor B2 so that connections to the motor for phase B and phase C are interchanged with respect to connections described for the secondary up operation in e above. Phase A is applied through connector P1-J (A2), fuse F6, contacts 9-17 of deenergized secondary braking relay K6, and contacts 8-16 of energized K9 to one winding of motor B2. Phase B is applied through connectors P1-H (A2), contacts 15-6 of energized K9, fuse F2, and contacts 14-3 of deenergized K6 to the third winding of motor B2. Phase C is applied through connector P1-C (A2), contacts 4-14 of energized K9, fuse F4, and contacts 5-15 of deenergized K6 to the second winding of motor B2. With 3-phase power thus applied to B2, the motor rotates in a direction opposite that described in e above, causing the secondary reflector to retract.

(3) Secondary retract limit switch S4. Secondary reflector retraction, like injection, is completed during the same particular one degree movement of the primary reflector. Secondary actuator motor B2 rotates until the internal mechanism of the actuator opens normally-closed momentary-contact secondary retract limit switch S4

in the actuator. At this point in the downward tilt of the reflector assembly, the secondary reflector is fully retracted. Opening secondary retract limit switch S4 breaks the holding circuit through contacts 18-12 of K9. This allows K9 to deenergize removing ac driving power from the secondary actuator motor. This energizes the secondary brake unit. The action of the secondary brake unit is described in g below.

(4) <u>Primary lower limit switch S2 and primary upper limit switch S3.</u> With the secondary reflector fully retracted, the reflector assembly continues to be driven downward by primary actuator motor B3 until the lug of the control switch plate reaches and operates primary lower limit switch S2. Relay K10 is thereby deenergized and the -28-volt circuit for operating the primary brake unit is completed for a brief moment through contacts 18-11 of deenergized relays K10 and K11. With S2 operated, ground is applied through S2 and contacts 16-7 of deenergized K10 to energize K11. Ground is also applied through J2-4 to contact 16 of K11. With K11 energized, 3-phase ac power is applied to the primary actuator motor in the manner described in e above, and the up operation is initiated. As the reflector assembly starts to tilt upward the lug of the control switch plate starts to move downward, returning S2 to the unoperated position and braking the ground connection to K11. However, holding contacts 16-8 of energized K11 maintain the relay

energized by continuing the ground path from contact 16 through unoperated primary upper limit switch S3, connector P2-5, and contacts 16-7 of deenergized K10 to the solenoid of K11. Thus, the reflector assembly is permitted to be driven upward until the lug of the control switch plate operates S3. When S3 is operated, it breaks the ground connection to K11, causing K11 to be deenergized. When K11 is deenergized, contacts 17-9 complete a path for ground through unoperated S2, J2-10 to energize K10. For the brief moment preceding the energization of K10, the primary brake unit operates. With K10 again energized, ac power is applied to primary actuator motor B3 and the reflector scans downward. The reflector assembly is driven downward until S2 is operated. The entire cycle repeats until stopped by placing S6 in the center position.

g. <u>Brake Units Using the Electro-Mechanical Control Panel - 9154368.</u>
(1) As mentioned in d above, there are two brake units for stopping motor rotation, one for primary actuator motor B3 and one for secondary actuator motor B2. The primary actuator brake unit consists of solenoid type relays K7 and K8, and thermal-type relays K1A and K1B. The secondary brake unit consists of solenoid-type relays K2A and K2B, and thermal-type relays K1 and K3. A brake unit is activated from the moment the -28-volt supply circuit is completed to the heating elements of the thermal relays of the particular brake

unit. A brake unit once activated, remains activated until either the -28-volt supply line to the thermal relays is interrupted or the thermal elements complete a heating and cooling cycle. The primary brake unit is activated each time phase B and phase C driving power is removed from the primary actuator motor windings. This occurs when both K11 and K10 are deenergized during the same time interval. At such time the -28-volt circuit is completed to the primary brake unit through contacts 18-11 of K11 and K10. The secondary brake unit is activated each time phase B and phase C driving power is removed from the secondary actuator motor windings. This occurs when both K9 and K12 are deenergized. When a brake unit is activated, its braking relay (K6 in the secondary braking unit or K8 in the primary braking unit) is energized. Energizing K6 or K8 applies the 100-volt dc output of a bridge rectifier to windings of the secondary actuator motor or windings of the primary actuator motor in place of the removed phase B and phase C power. The effect of the 100-volt dc potential on the motor is to provide an electromagnetic clutching action which overcomes rotor inertia and stops rotation.

(2) The bridge rectifier consists of transformer T1 and the four-selenium diode units designated as CR1. The primary of T1 is supplied by 120 volts, 400 cps. This voltage is obtained from phase B of the 3-phase power supply at connector P1-H and neutral of the 3-phase power supply at connector P1-D. The primary of T1 is fused by F3.

(3) Since the operation of the primary brake unit is identical to that of the secondary brake unit, only the secondary brake unit is discussed. Thermal relay K1A in the primary brake unit is identical to thermal relay K2A in the secondary brake unit; thermal relay K1B in the primary brake unit is identical to thermal relay K2B in the secondary brake unit. The complete explanation of secondary brake unit operation follows in (4) and (5) below.

(4) When both K9 and K12 are deenergized, -28 volts is applied through contacts 7-16 of K12 and 9-17 of K9 to the brake circuit. The -28 volts is applied through contacts 1-13 of K5 energizing K6. Secondary braking relay K6 connects the 100-volt dc braking voltage from the bridge rectifier circuit to motor B2. The connections from the rectifier are made through contacts 2-13 and 14-4 of K6 and through P1-11 and J1-D to B2. The dc return is from B2 through J1-B to the rectifier. This voltage stops the rotation of B2.

(5) The -28 volts is also applied through contacts 14-3 of K5 to start the heating cycle for (thermal) secondary timing relays K2B and K2A. Shortly after the heating cycle starts, K2A energizes closing contacts 5-7 of K2A. This has no immediate effect since K6 is already energized. Some time later (interval set at the factory), K2B energizes closing contacts 5-7 of K2B and energizes K5. Ener-

gizing K5 closes contacts 13-2 and 14-4 of K5. Relay K5 is held energized through holding contacts 14-4 until the —28 volts is removed from the brake circuit. The energizing of K5 marks the end of the heating cycle and the beginning of the cooling cycle of K2A and K2B because contacts 14-3 of K5 are opened and the —28 volts is removed from the heating elements of K2A and K2B. Immediately after the cooling cycle begins, K2B deenergizes. However, this has no immediate effect since K5 is held energized by holding contacts 14-4. Some time later K2A opens, breaking the —28-volt circuit to K6, allowing K6 to deenergize. The deenergizing of K6 removes the 100-volt dc braking voltage from B2, completing the braking cycle. The circuit remains in this condition until the —28 volts is removed from the brake circuit by energizing K9 or K12. When either K9 or K12 is energized, the —28 volts is removed by the opening of contacts 17-9 and 16-7, respectively. Removing the —28 volts allows K5 to deenergize, rendering the brake circuit ready for the next braking cycle.

h. Electro-Mechanical Control Box 9007806 Using Electro-Mechanical Control Panel 9988-941. The electro-mechanical control box (fig. 103) contains electro-mechanical control panel 9988941, primary lower limit switch S2, secondary inject-retract switch S1, primary upper limit switch S3, the 0 to 9-degree scale, the control switch plate, and jogging switching S4. The electro-mechanical control panel consists of six relays, a 100-volt dc power supply, and four fuses. Three of the six relays form a group which controls the operation of the primary reflector by controlling the operation of the primary actuator motor. The remaining three relays form a second group which controls the operation of the secondary reflector by controlling the operation of the secondary actuator motor. In each relay group, two relays control the tilt of the reflector associated with the group. The remaining relay in each group acts as a brake unit. Each brake unit controls and times the application of 100 volts dc to windings of the actuator motor with which the

brake unit is associated. The application of 100 volts dc to an actuator motor occurs automatically when 3-phase ac driving power is removed from the respective motor. Three-phase ac driving power is removed from the motor when the two relays which control motor operation (reflector tilt) are deenergized. Deenergizing the two motor control relays of either relay group completes a path for energizing the brake unit of that group.

Note. The key letter-number combinations shown in parentheses in *i* and *j* below refer to figure 105 1 unless otherwise indicated

i. "Up" Operation Using Electro-Mechanical Control Panel 9988941.

(1) *Primary actuator motor B3.* When ANTENNA — ELEVATION scan switch S6 (B1) on the acquisition control-indicator is manually held in the UP position, ground is applied through connector P1-A (C2) to energize primary up relay K5 in the electro-mechanical control panel. The current path for energizing K5 is from —28 volts through connector P1-I (C2) through contacts 5-15 of deenergized primary down relay K4, primary up safety switch S2, solenoid of K5, contacts 7-16 of deenergized K4, and contacts 2-1 of S6 to ground. With K5 energized, 3-phase ac power is applied to the windings of the primary actuator motor. Phase A is applied through connector P1-J (A2), fuse F4, and contacts 12-18 of energized primary up relay K5 to one winding of primary actuator motor B3 Phase B is applied through connector P1-H (A2), fuse F1, contacts 13-2 of primary up relay K5, contacts 1-3 of deenergized K2 to the second winding of B3. Phase C is applied through connector P1-C (A2), fuse F2, contacts 4-14 of energized K5, and contacts 6-4 of deenergized K2 to the third winding of B3. With 3-phase power thus applied to B3, the motor rotates in a direction which causes the primary reflector (and hence the entire reflector assembly) to tilt upward With switch S6 held in the UP position, the reflectors

continue to tilt upward until their limits are reached and remain there.

(2) *Secondary actuator motor B2.* As the primary reflector is driven upward, the injection control rod (fig. 103) causes the control switch plate to be driven downward. At a predetermined time, depending on the scan mode (physical position of secondary inject-retract switch S1), the lug on the control switch plate momentarily closes S1. At this instant, S1 (C4) completes the path of the -28 volts to the solenoid of secondary inject relay K6, thereby energizing K6. The current path for energizing K6 is from -28 volts through P1-I (C2), secondary inject-retract switch S1, secondary inject limit switch S1, secondary inject safety switch S2, contacts 1-13 of deenergized secondary retract relay K3, solenoid of K6, contacts 7-16 of deenergized primary down relay K4, and S6-2 and 1 to ground. Holding contacts 14-4 of energized K6 maintain K6 energized after the lug of the control switch plate (fig. 103) has passed S1 and is on the way toward S2. With K6 (C6) energized, 3-phase ac power is applied to the windings of secondary actuator motor B2. Phase A is applied through connector P1-J (A2), fuse F4, and contacts 6-15 of energized K6 to one winding of B2. Phase B is applied through connector P1-H (A2), fuse F1, contacts 17-10 of energized K6, and contacts 1-3 of deenergized K1 to the second winding of B2. Phase C is applied through connector P1-C (A2), fuse F2, contacts 12-18 of energized K6, and contacts 6-4 of deenergized K1 to the third winding of B2 With 3-phase power thus applied to motor B2, the motor rotates in a direction which causes the secondary reflector to be injected.

(3) *Secondary inject limit switch S1.* Secondary reflector injection is completed during a particular one degree of primary reflector upward tilt as determined by the preselected scan mode. Motor B2 rotates until the internal mechanism of the actuator opens normally-closed momentary-contact secondary inject limit switch S1 in the secondary actuator. At this point in the upward tilt of the reflector assembly, the secondary reflector is fully injected. Opening S1 deenergizes K12 to remove ac driving power from B2. This energizes the secondary brake unit.

(4) *Secondary braking relay K1.* The secondary brake unit is operated by secondary braking relay K1. The action of the secondary brake unit and the energization path are discussed in *k* below. With the secondary reflector fully injected, the reflector assembly continues to be driven upward by primary actuator motor B3 until the internal mechanism of the actuator opens normally-closed, momentary-contact, primary up safety switch S2. At this time the reflector assembly is at maximum elevation. Opening the primary up safety switch deenergizes K5 to remove ac driving power from primary actuator motor B3. This energizes the primary brake unit

(5) *Primary braking relay K2.* The primary brake unit is operated by primary braking relay K2 The action of the primary brake unit and energization path are described in *k* below. It should be noted that in the "up" operation (S6 manually held in the UP position), the action of primary upper limit switch S3 has no effect on circuit operation even though it is operated by the lug of the control switch plate. However, in the "down/scan" operation discussed in *j* below, S3 determines the upper limit of reflector assembly tilt.

j. "Down/Scan" Operation Using Electro-Mechanical Control Panel 9988941.

(1) *Primary actuator motor B3.* When ANTENNA — ELEVATION scan switch S6 is placed in the DOWN/SCAN position, ground is applied through primary lower limit switch S2 to energize primary down relay K4 in the control panel. The current path

for energizing K4 is from −28 volts through connector P1-I (C2), primary down safety switch S1, solenoid of K4, contacts 9-17 of deenergized K5, contacts of unoperated S2, and contacts 2-3 of S6 to ground. With K4 energized, 3-phase ac power is applied to the windings of primary actuator motor B3 so that connections to the motor for phase B and phase C are interchanged with respect to connections described for the primary up operation in i above. The connection of phase A remains the same as described in i above. Phase B is applied through connector P1-H (A2), fuse F1, contacts 17-10 of energized K4, and contacts 6-4 of deenergized K2 to the third winding of B3. Phase C is applied through connector P1-C (A2), fuse F2, contacts 14-4 of energized K4, and contacts 1-3 of deenergized K2 to the second winding of B3. With 3-phase power thus applied to primary actuator motor B3, the motor rotates in a direction opposite to that described in i above, causing the primary reflector (and hence the entire reflector assembly) to tilt downward.

(2) *Secondary actuator motor B2.* As the primary reflector is driven downward, the injection control rod (fig. 103) causes the control switch plate to be driven upward. When the plate is driven up to the point where the lug on the plate alines itself with secondary inject-retract switch S1, S1 closes momentarily At this instant, S1 (C3) completes the path of the −28 volts to the solenoid of secondary retract relay K3, thereby energizing K3. The current path for energizing K3 is from −28 volts through connector P1-I (C2), switch S1, secondary retract limit switch S4, secondary retract safety switch S3, contacts 1-13 of deenergized secondary inject relay K6, solenoid of K3, contacts 17-9 of deenergized primary up relay K5, unoperated S2, and contacts 3-2 of S6 to ground. Holding contacts 18-12 of energized K3 maintain K3 energized

after the lug (fig. 103) of the control switch plate has passed S1 and is on the way toward S3. With K3 (C5) energized, 3-phase ac power is applied to the windings of motor B2 so that connections to the motor for phase B and phase C are interchanged with respect to connections described for the secondary up operation in i above. Phase A is applied through connector P1-J (A2), fuse F4, and contacts 8-16 of energized K3 to one winding of motor B2. Phase B is applied through connectors P1-H (A2), fuse F1, contacts 15-6 of energized K3, and contacts 6-4 of deenergized K1 to the third winding of motor B2. Phase C is applied through connector P1-C (A2), fuse F2, contacts 4-14 of energized K3, fuse F4, and contacts 1-3 of deenergized K1 to the second winding of motor B2. With 3-phase power thus applied to B2, the motor rotates in a direction opposite that described in i above, causing the secondary reflector to retract.

(3) *Secondary retract limit switch S4.* Secondary reflector retraction, like injection, is completed during the same particular one-degree movement of the primary reflector. Secondary actuator motor B2 rotates until the internal mechanism of the actuator opens normally-closed momentary-contact secondary retract limit switch S4 in the actuator. At this point in the downward tilt of the reflector assembly, the secondary reflector is fully retracted. Opening secondary retract limit switch S4 breaks the holding circuit through contacts 18-12 of K3. This allows K3 to deenergize removing ac driving power from the secondary actuator motor. This energizes the secondary brake unit. The action of the secondary brake unit is described in k below.

(4) *Primary lower limit switch S2 and primary upper limit switch S3.* With the secondary reflector fully retracted, the reflector assembly continues to be driven downward by primary actuator

motor B3 until the lug of the control switch plate reaches and operates primary lower limit switch S2. Relay K4 is thereby deenergized and the primary brake unit is operated. The action of the primary brake unit and the energization path are discussed in *k* below. With S2 operated, ground is applied through S2 and contacts 16-7 of deenergized K4 to energize K5. Ground is also applied through J2-4 to contact 16 of K5. With K5 energized, 3-phase ac power is applied to the primary actuator motor in the manner described in *i* above, and the up operation is initiated. As the reflector assembly starts to tilt upward, the lug of the control switch plate starts to move downward, returning S2 to the unoperated position and breaking the ground connection to K5. However, holding contacts 16-8 of energized K5 maintain the relay energized by continuing the ground path from contact 16 through unoperated primary upper limit switch S3, connector P2-5, and contacts 16-7 of deenergized K4 to the solenoid of K5. Thus, the reflector assembly is permitted to be driven upward until the lug of the control switch plate operates S3. When S3 is operated, it breaks the ground connection to K5, causing K5 to be deenergized. When K5 is deenergized, contacts 17-9 complete a path for ground through unoperated S2 and J2-10 to energize K4. For the brief moment preceding the energization of K4, the primary brake unit operates. With K4 again energized, ac power is applied to primary actuator motor B3 and the reflector scans downward. The reflector assembly is driven downward until S2 is operated. The entire cycle repeats until stopped by placing S6 in the center position.

k. Brake Units Using Electro-Mechanical Control Panel 9988941.

(1) As mentioned in *h* above, there are two brake units for stopping motor rotation, one for primary actuator

motor B3 and one for secondary actuator motor B2. The primary actuator brake unit consists of relay K2, resistors R6 and R8, and capacitor C5B. The secondary brake unit consists of relay K1, resistors R5 and R7, and capacitor C5A. The primary brake unit is activated each time phase B and phase C driving power is removed from the primary actuator motor windings. This occurs when both K5 and K4 are deenergized during the same time interval. The secondary brake unit is activated each time phase B and phase C driving power is removed from the secondary actuator motor windings. This occurs when both K3 and K6 are deenergized. When a brake unit is activated, its braking relay (K1 in the secondary braking unit or K2 in the primary braking unit) is energized. Energizing K1 or K2 applies the 100-volt dc output of a bridge rectifier to windings of the secondary actuator motor or windings of the primary actuator motor in place of the removed phase B and phase C power. The effect of the 100-volt dc potential on the motor is to provide an electro-magnetic clutching action which overcomes rotor inertia and stops rotation.

(2) The bridge rectifier consists of transformer T1 and the four-selenium diode units designated as CR1. The primary of T1 is supplied by 120 volts, 400 cps. This voltage is obtained from phase B of the 3-phase power supply at connector P1-H and neutral of the 3-phase power supply at connector P1-D. The primary of T1 is fused by F3.

(3) Since the operation of the primary brake unit is identical to that of the secondary brake unit, only the secondary brake unit is discussed. Operation of primary braking relay K2, resistors R6 and R8, and capacitor C5B in the primary brake unit is identical to operation of secondary braking relay K1, resistors R5 and R7, and capacitor C5A in the secondary

QUISITION ANTENNA —8158132
MECHANICAL CONTROL BOX —9007806
MECHANICAL CONTROL PANEL —9988941

NOTES
1. ALL VALUES ARE EXPRESSED IN OHMS OR MICROFARADS UNLESS OTHERWISE INDICATED
2. CIRCUITRY BETWEEN ACQUISITION ANTENNA AND ACQUISITION CONTROL-INDICATOR OMITTED TO SIMPLIFY DIAGRAM

PRIMARY ACTUATOR —8159580

MOT B3 PRIMARY ACTUATOR
NEUTRAL

SECONDARY ACTUATOR —8159579

MOT B2 SECONDARY ACTUATOR
NEUTRAL

S2 SECONDARY INJECT SAFETY
S1 SECONDARY INJECT-LIMIT
NC
S3 SECONDARY RETRACT SAFETY
SECONDARY RETRACT-LIMIT

PRIMARY ACTUATOR —8159580

S1 PRIMARY DOWN SAFETY
S2 PRIMARY UP SAFETY

C3 0.047   R3 130
C4 0.047   R4 130
C1 0.047   R
C2 0.047   R2 13

YEL
RED   CR1   T1
YEL

R8 430   C5B 16

R5 6800   R6 6800

K6 SECONDARY INJECT 240
K1 SECONDARY BRAKING 5000
K2 PRIMARY BRAKING 5000

B1 ELEVATION TRANSMITTER SYNCHRO
S1 S2 S3   R1 R2

ORD GB1745

on antenna—elevation electro-mechanical scan circuit—
functional schematic diagram.

Figure 105.1 (U). Acquisition antenna—elevation electro-mechanical functional schematic diagram.

238.2

CHAPTER 8 (CMHA)

DIRECTOR-COMPUTER GROUP—MISCELLANEOUS ACQUISITION RADAR COMPONENTS

87 (U). FUIF Interconnecting Box 9013084 and Cover 9013079

a. General. The FUIF (fire unit integration facility) interconnecting box and cover provide space for mounting terminal boards, subassemblies, relays, fuses, and fuse indicator lamps that are associated with the FUIF equipment and radar signal simulator AN/MPQ-36.

b. Detailed Theory. Terminal boards in the FUIF interconnecting box provide terminals for connecting, at a common point, several leads carrying the same data. Three subassemblies are mounted in the box: FUIF relay assembly 8518681, FUIF fixed attenuator 8518708, and PPI test panel 9136426. Mounted on the cover are four 0.031-ampere fuses and four fuse indicator lamps. ACQ RADAR –250V fuse F1 (fig. 46, TM 9–1430–257–20) protects the acquisition radar –250-volt supply from damage caused by failures in the FUIF equipment. If a malfunction occurs in the FUIF equipment connected to the –250-volt supply and blows F1, the –250-volt supply will continue to operate in the acquisition radar system; only the FUIF equipment will become inoperative. ACQ RADAR +250V fuse F2 provides the same protection to the acquisition radar +250-volt supply. COMP –250V fuse F3 and COMP +250V fuse F4 protect the –250- and +250-volt supplies, respectively, in the computer. Fuse indicator lights I1 through I4 are blown fuse indicators that operate in conjunction with fuses F1 through F4, respectively. Relay K2, when energized, allows –24 volts to pass through its contacts to J29–72 and then to a solenoid in the cable connector from the radar signal simulator. This action causes the connector to eject from the trailer mounted director station. Relay K1, when energized, applies –28 volts to the trailer mounted tracking station through contacts 10 and 4, causing a similar ejection action in the trailer mounted tracking station. Relay K3, when energized, makes the connection between terminals 33 and 35 of J29. This connection is used in the radar signal simulator. Resistor assembly 9008129 contains resistors and a capacitor to match and connect circuits from the radar signal simulator to circuits in the trailer mounted director station.

87.1 (U). Auxiliary Acquisition Interconnecting Box 9985602 and Cover 9985622

a. General. The auxiliary acquisition interconnecting box and cover provide space for monitoring terminal boards, subassemblies, relays, fuses, and fuse indicator lamps that are associated with the FUIF equipment, radar signal simulator AN/MPQ-36, and the AAR (auxiliary acquisition radar).

b. Detailed Theory. The theory of operation of the auxiliary acquisition interconnecting box and cover is similar to the theory of operation of the FUIF interconnecting box and cover discussed in paragraph 87. The auxiliary acquisition interconnecting box and cover (fig. 46.1, TM 9–1430–257–20) contain three subassemblies: resolver-video amplifier 9990729, FUIF relay assembly 8518681, and FUIF fixed attenuator 8518708. Transformers T1 through T4 are used to couple preknock, sync, and IFF video signals from the AAR to the Nike system and sync from the acquisition radar system to the tracking radar system.

87.2 (U). Auxiliary Acquisition Control Interconnecting Group 9988902 and Auxiliary Acquisition Interconnecting Box 9989089

a. The auxiliary acquisition control interconnecting group consists of auxiliary acquisition cabinet 9143830, HIPAR auxiliary control-indicator 9156314, LOPAR auxiliary control-indicator 9156366, HIPAR resolver amplifier 9984381, FUIF relay assembly 9984404, and

PPI test panel 9136426. It provides space for mounting connectors, terminal boards, fuses, and fuse indicator lamps. Four 0.031-ampere fuses and four fuse indicator lamps are mounted on the cover. ACQ RADAR –250V fuse F1 (B2, fig. 94, TM 9–1430–257–20) protects the LOPAR –250-volt supply from damage caused by failures in the FUIF equipment. If a malfunction occurs in the FUIF equipment connected to the –250-volt supply and F1 blows, the –250-volt supply will continue to operate; only the FUIF equipment will become inoperative. ACQ RADAR +250V fuse F2 provides the same protection for the LOPAR +250-volt supply. COMP –250V fuse F3 and COMP +250V fuse F4 protect the –250-volt and +250-volt supplies in the computer. Fuse indicator lights DS1 through DS4 are blown fuse indicators for F1 through F4, respectively.

   b. The auxiliary acquisition interconnecting box provides space for mounting terminal boards, connectors, and cables associated with the HIPAR, LOPAR, and FUIF equipment. The terminal boards provide terminals for connecting signal and power leads into the director station trailer wiring.

▌87.3 (U). HIPAR Auxiliary Control-Indicator 9156314

   a. General. The HIPAR auxiliary control-indicator contains part of the controls and indicators for the high-power acquisition radar. It is a subassembly of the auxiliary acquisition control interconnecting group.

   b. Detailed Theory.

   (1) The external automatic tuning mechanism can be made to tune the HIPAR transmitter and receiver to one of 10 preselected frequencies by operating any one of CHANNEL SELECT switches S1 through S10 (fig. 95, TM 9–1430–257–20). A second set of contacts on the switches disables the high-voltage circuits during the tuning period, which is approximately 30 seconds. HIPAR STATUS-OPERATE indicator light DS5 indicates that power is available at the channel select switches. CHANNEL indicator

light DS1 indicates which of the 10 channels is in use.

   (2) HIPAR STATUS-READY indicator light DS3 and HIPAR STATUS-ON indicator light DS4 indicate that the transmitter is ready to operate or is in operation.

   (3) DRIVE OVERLOAD RESET indicator light DS2 indicates an overload in the tuning circuits. DRIVE OVERLOAD RESET switch S12 is used to reapply power when the overload is cleared.

   (4) BATTLE SHORT switch S11 is used to bypass the delay timers in an emergency situation. TEST ENABLE switch S13 conditions the equipment for testing. POWER OUT meter M1 gives an indication proportional to the power output of the HIPAR transmitter.

87.4 (U). LOPAR Auxiliary Control-Indicator ▌ 9156366

   a. General. The LOPAR auxiliary control-indicator contains part of the controls and indicators for the LOPAR. It is a subassembly of the auxiliary acquisition control interconnecting group.

   b. Detailed Theory.

   (1) INDICATOR HV switch S6 (fig. 96, TM 9–1430–257–20) applies ac power to the indicator high-voltage circuits, and INDICATOR HV-ON indicator light DS5 indicates that the power is on.

   (2) The magnetron high-voltage control circuit consists of HV SUPPLY switch S3, auto transformer T1, HV SUPPLY-ON indicator light DS3, HV SUPPLY-READY indicator light DS4, HV SUPPLY-ON switch S4, HV SUPPLY-OFF switch S5, and contacts 2 and 1 of S2B. In order to turn on the magnetron high voltage, the control knob for T1 must be operated to the minimum output or START position, closing S3. If NOISE GEN switch S2 is in the OFF position, closing S4 completes a relay ground

circuit enabling the magnetron high-voltage circuits. The external relay locks through closed contacts of S5, and T1 may be adjusted for full output without breaking the high-voltage circuit. Operating S5 breaks the high-voltage circuit. Resistors R2 and R3 are current limiting resistors to protect T1 against overload.

(3) When S2 is in the ADJ position, the external noise generator circuit is energized by —28 volts applied through terminal 195 of auxiliary acquisition control interconnecting group, contacts 5-7 of S2B, 9-11 of C2A, and terminal 194 of the auxiliary acquisition control interconnecting group. NOISE indicator light DS2 is illuminated by 28v applied through contacts 5-7 of S2B. At the same time, meter M1 and shunt resistor R1 are connected across the output of the receiver noise circuit. When S2 is operated to MEAS, the noise generator circuit is disabled by open contacts 9-10 of S2A. However, DS2 remains energized to show that M1 is being used for noise measurements. M1 is then directly across the output of the receiver noise circuit.

(4) When S2 is in the OFF position and the magnetron high voltage is on, MAGNETRON indicator light DS1 is energized and meter M1 is across the output of switch S1. Depending on its position, S1 applies a voltage proportional to magnetron current (MAG MA), modulator high voltage (RECT KV), or modulator current (RECT MA).

(5) MTI SECTOR ANGLE resolver B1 is positioned to indicate the center-line of the sector display of the MTI circuits. HIPAR select relay K1 is energized when it is desired to switch from the LOPAR to the HIPAR. Among other things, K1 removes the excitation from resolver B1.

87.5 (U). Auxiliary Acquisition Control Interconnecting Group 9989071 and Auxiliary Acquisition Interconnecting Box 9989067

a. *General.* Auxiliary acquisition control interconnecting group 9989071 and auxiliary acquisition interconnecting box 9989067 are similar to and perform the same function as the auxiliary acquisition control interconnecting group 9988902 and auxiliary acquisition interconnecting box 9989089 discussed in paragraph 87.2 above. The differences in detailed theory are discussed in *b* below.

b. *Detailed Theory.*

(1) Auxiliary acquisition control interconnecting group 9989071 (fig. 94, TM 9-1430-257-20) differs from 9989089 because HIPAR resolver amplifier 9984381 is replaced. HIPAR resolver amplifier 9990729 and the associated wiring is modified as required.

(2) Auxiliary acquisition interconnecting box 9989067 replaces 9989089. Transformers T2, T3, and T4, and associated wiring are added to isolate sync, video, and preknock circuits between HIPAR acquisition radar or auxiliary acquisition radar (AAR) and the improved NIKE-HERCULES system.

88 (U). FUIF Relay Assembly 8518681

a. *General.* The FUIF relay assembly transfers fire and target tracked data from the acquisition and tracking radar systems to FUIF system AN/FSG-1 or AN/MSG-4.

b. Detailed Theory. The FUIF relay assembly contains two relays which provide ground connections to FUIF system AN/FSG-1 or AN/MSG-4. When ground is applied at connector P1-5 (fig. 47, TM 9-1430-257-20), target tracked relay K2 is energized and contacts 9-2 close, applying ground to connector P1-4. When ground is applied at connector P1-7, fire relay K1 is energized and contacts 9-2 close, allowing ground to be applied to connector P1-2. Varistor CR1C in parallel with the coil of K2 and varistor CR1A in parallel with the coil of K1 prevent arcing in the relay coils.

88.1 (U). HIPAR Resolver Amplifier 9984381

a. General. The HIPAR resolver amplifier is a dual-channel audio amplifier of conventional design used to amplify the output of an acquisition azimuth resolver.

b. Detailed Theory. Since the two channels are identical, only the north-south channel will be described. The 4-kc sine wave signal from the acquisition azimuth resolver is applied to connectors P1-1 and P1-3 (fig. 97, TM 9-1430-257-20/1). The signal is coupled through impedance matching transformer T4 and developed across variable resistor R23. The variable resistor acts as a gain control. The adjusted output signal is applied to the grid of voltage amplifier V1 through the parallel combination of resistor R1 and capacitor C6. Resistor R1 and part of variable resistor R23 form the grid load for V1. Capacitor C6 forms part of a voltage divider for the high-frequency component of the feedback voltage. Bias for V1 is developed across cathode resistor R3 and bypass capacitor C5. Resistor R5 is the screen dropping resistor, and capacitor C2 the screen bypass. The amplified and inverted output of V1 is developed across plate load resistor R4 and coupled through capacitor C3 to the grid of power amplifier V2. Resistor R9 is the grid load. Bias for V2 is developed across cathode resistor R6 and bypass capacitor C8. The amplified and inverted output of V2 is developed across parasitic suppressor resistor R7 and the primary of output transformer T2. Capacitor C9 and resistor R10 decrease high-frequency response (harmonic suppression) by shunting the primary of T2. Resistor R8 and capacitor C1 form a decoupling network for the screen and plate circuits. Response to high frequencies

244.2

(harmonics) is further reduced by shunt resistor R21 and capacitor C4 across the secondary of T2, plus selective feedback through the parallel combination of resistor R2 and capacitor C7. More energy is fed back through C7 at the higher frequencies, thus reducing the high frequency gain. Stepdown transformer T1 provides filament voltage for the amplifier tubes.

89 (U). FUIF Fixed Attenuator 8518708

a. General. The FUIF fixed attenuator is used to attenuate and transmit target coordinate data from the computer to FUIF system AN/FSG-1 or AN/MSG-4. It also isolates the computer system from the FUIF system, preventing any faulty ground connection in the FUIF system from affecting the operation of the computer.

b. Detailed Theory. The FUIF fixed attenuator (fig. 48, TM 9-1430-257 20) contains four channels for attenuating signals from the computer; the $+X_T$, $+Y_T$, $+H_T$, and $+D_T$ channels. Since all channels contain similar circuits and operate in a similar manner, only the $+X_T$ channel is discussed. The $+X_T$ impedance network Z1 contains a series-dropping resistor between terminals 1-2 and a signal-developing resistor between terminals 2-3. Capacitor C1 bypasses transient signals to ground. After the $+X_T$ signal is attenuated by Z1, the signal becomes $+X_T$ (FUIF) and is applied to connector P1-8. The four outputs, $+X_T$ (FUIF), $+Y_T$ (FUIF), $+H_T$ (FUIF), and $+D_T$ (FUIF), are fed to FUIF system AN/FSG-1 or AN/MSG-4.

89.1 (U). FUIF Relay Assembly 9984404

a. General. FUIF relay assembly 9984404 transfers fire and target tracked data from the acquisition and tracking radar systems to FUIF system AN/FSG-1 or AN/MSG-4. It also transmits target coordinate data from the computer to the FUIF system.

b. Detailed Theory. The FUIF relay assembly contains two relays which provide ground connections to FUIF system AN/FSG-1 or AN/MSG-4. When ground is applied at connector P2-5 (fig. 98, TM 9-1430-257-20/1), target tracked relay K2 is energized and contacts 9-2 close, applying ground to connector P2-4. When ground is applied at connector P2-7, fire relay K1 is energized and contacts

channel, the Y deflection channel remains grounded, resulting in a simulated target on the PPI screen at 4800 mils in azimuth. With S1 in +Y AXIS position, +15.6 volts is applied to the Y deflection channel; the X deflection channel is grounded, resulting in a simulated target on the PPI screen at 0 mils in azimuth. With S1 in the –Y AXIS, –15.6 volts is applied to the Y deflection channel, the X deflection channel remains grounded, resulting in a simulated target on the PPI screen at 3200 mils in azimuth. Capacitors C1 and C2, connected externally through terminals S1 to terminals Z1–2 and Z1–3, bypass transient voltages to ground.

(3) *Test points.* Test point TP1 is provided for monitoring the output of the pulse generator. Test point TP2 is provided for monitoring the X-analog positioning voltage, test point TP3 is provided for monitoring the +250 volts, and test point TP4 is provided for monitoring the ±15.6-volt output of Z1.

90.1 (U). Resolver-Video Amplifier 9990729

a. General. The resolver-video amplifier is a dual-channel audio amplifier of conventional design used to amplify the output of an acquisition azimuth resolver and a video amplifier which is used to separate two system grounds by 1000 ohms and provides video isolation.

b. Detailed Theory. The resolver-video amplifier (fig. 49.1, TM 9–1430–257–20) contains two channels used to amplify the output of the acquisition azimuth resolver. Also included is a video isolation amplifier connected to amplify the voltages on the center conductor of J1 with respect to the shield, and to reject any voltage differential between the shield and the chassis.

(1) *Resolver amplifiers.* Amplifiers V3 and V4 with their associated circuit components comprise the North-South amplifier channel and amplifiers V5 and V6 with their associated circuit components comprise the East-West amplifier channel. The theory of operation of the acquisition azimuth resolver amplifiers is the same as the theory for the HIPAR resolver amplifier described in paragraph 88.1

(2) *Video isolation amplifier.* Video from the AAR (auxiliary acquisition radar) is applied through AAR VID INPUT connector J1. Resistor R1 is the terminating resistor for the coaxial cable connected at J1. Capacitor C1 is a coupling resistor to grid 7 of cathode follower section 6-7-8 of V1. Resistor R2 is the grid resistor for grid 7. Crystal diode CR1 shunts the negative portions of the video to the shield connection of J1. The positive output from cathode 8 is developed across resistor R28 and R6-R7 parallel resistors. The output voltage developed across common cathode resistors R6 and R7 is cathode coupled to grounded grid amplifier section 2-3-4 of V1. Resistor R5 is the plate load for section 2-3-4 of V1. The positive output developed across R5 is coupled through capacitor C2 to the grids of cathode follower V2. The shield connection of J1 is connected to the voltage divider consisting of resistors R3 and R4. This divider reduces the gain of section 2-3-4 of V1 to compensate for the less than unity gain of section

244.1

6-7-8 of V1. Any voltage difference between the shield connection of J1 and chassis ground is inverted in amplifier section 2-3-4 of V1 causing a rejection of any voltage difference in the output developed across plate load resistor R5. Both sections of cathode follower V2 are connected in parallel to provide the necessary driving power to the external circuit. The grids of V2 are biased at –6 volts by the voltage developed across resistor R10 which is part of the voltage divider consisting of resistors R11 and R10 between –250 volts and ground.

Resistor R9 is the grid resistor and diode CR2 is a clamping diode. Resistors R12 and R13 are parasitic suppressors. The positive output voltage is developed across cathode resistor R14 and coupled to AAR VID OUTPUT connector J2 for use in the external circuit.

91 (U). Battery Control Interconnecting Box 8512908 and Housing 8513740

a. *General.* The battery control interconnecting box provides space for mounting terminal
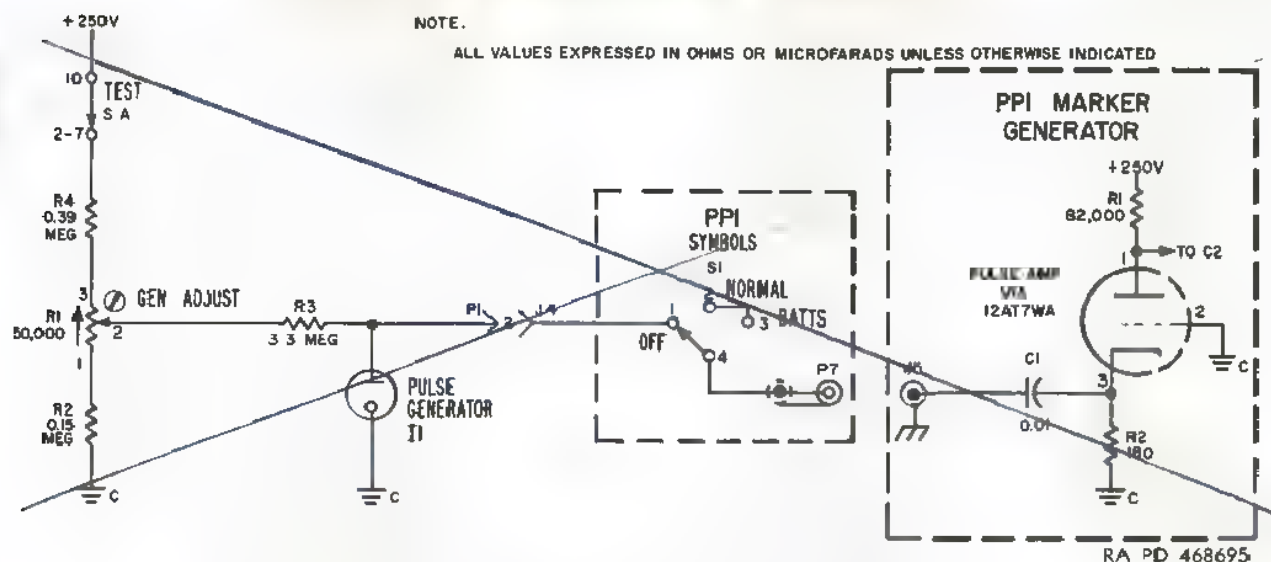
Figure 106. PPI test panel—pulse generator—simplified schematic diagram.

boards and subassemblies. Terminal boards in the box provide terminals for connecting, at a common point, several leads carrying the same data. Four subassemblies are mounted in the box: REVERSAL SWITCHES, telephone set TA 272/G, telephone protector TA 274/G, and composite telephone circuit TA–346/M. There are no items mounted on the housing.

b. *Detailed Theory.*

(1) *REVERSAL SWITCHES.* The REVERSAL SWITCHES (fig. 107) provide reversing of azimuth gyro (AG) data in the director-computer group. This insures that an indication may be read on MISSILES PREPARED meter M1 on the battery signal-panel indicator. These switches were added to the battery control interconnecting box circuits starting with system 1063. The Ordnance number remains unchanged. AG-REF switch S3 reverses polarity of the data in the AG reference circuits. AG SIG switch S2 reverses polarity of the data in the AG signal circuits. Protector blocks connected to terminals TY2 22 through TY2–25 are lightning arrestors used to protect the data circuits. The blocks are located at the first junction of the respec-

tive lines entering the trailer from the outside. These blocks are part of telephone protector TA–274/G discussed in (3) below.

(2) *Telephone set TA–272/G.* Telephone set TA 272/G is the same as telephone set TA–272/G covered in paragraph 52.

(3) *Telephone protector TA–274/G— 8008998.* Telephone protector TA–274/G (TM 9 1400–251 12) is inserted in the telephone trunk line paths to prevent damage to the telephone circuits due to an overload of voltage. Telephone protector TA–274/G is composed of 52 lightning arrestors and 52 signal binding posts. The binding posts are connected in series with the telephone circuits, and the lightning arrestors are connected between the binding posts and ground. The lightning arrestors are composed of carbon blocks which offer a high resistance to normal telephone voltages and low resistance to high voltages. The carbon blocks have an accurately gauged separation of a few thousandths of an inch. One block is connected to a binding post and the other to ground. Under normal operation, the carbon blocks present a high resistance

CONFIDENTIAL
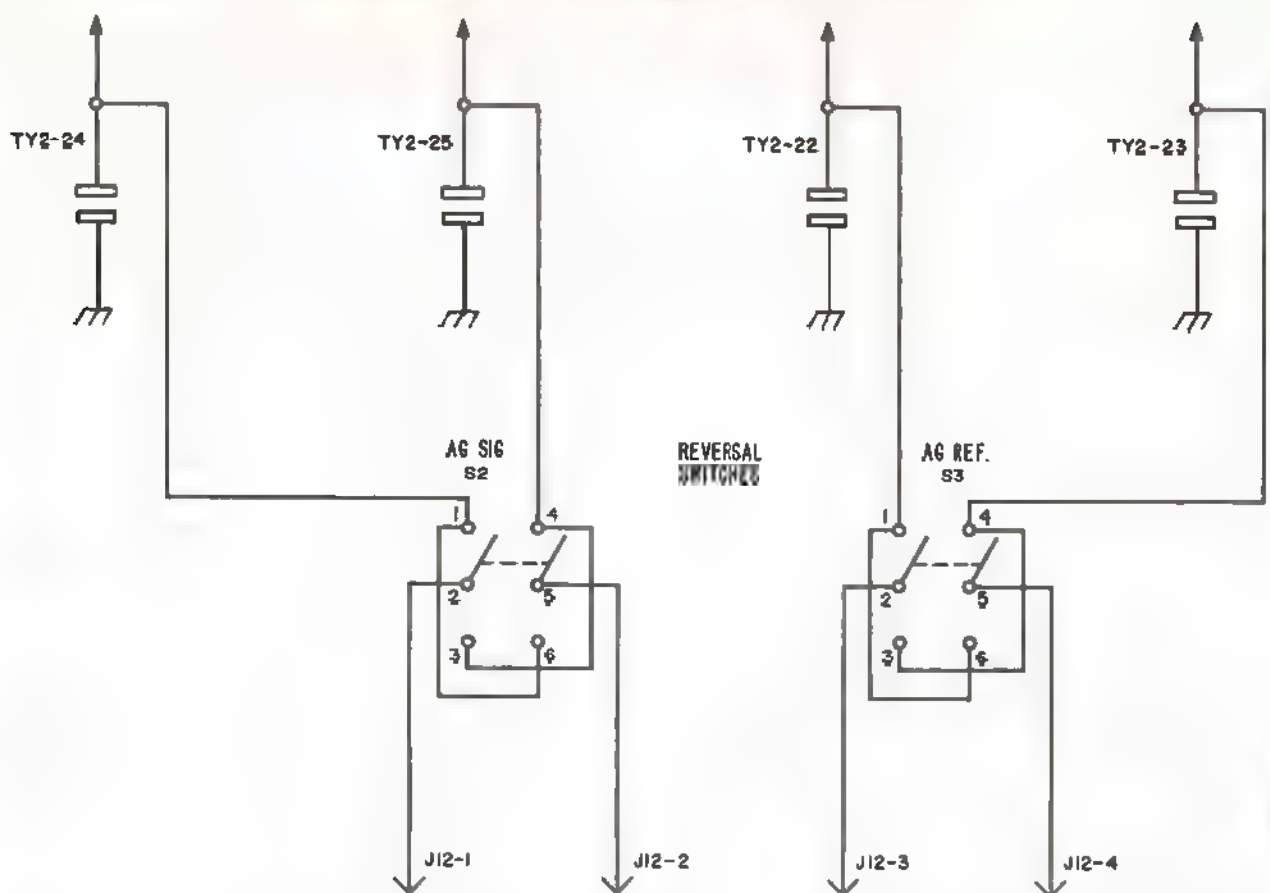
Figure 107. (U) *Reversal switches simplified schematic diagram.*

RA PD 468696

to the trunk lines, and any signals present at the binding post pass through to the telephone circuits. When an overload of voltage appears on a trunk line, the resistance of the carbon blocks decreases, allowing the high voltage to arc across the air gap to ground. This places the binding post at ground potential until the overload condition is cleared, thereby preventing any high voltages from being impressed on the telephone circuit paths.

(4) *Composite telephone circuit TA 349, or 683606.* The composite telephone circuit (TM 9-1400-251 12) is used to send gyro azimuth signal and reference voltages received from repeating coils in the computer-amplifier relay group (TM 9-1430-251-35) to a composite telephone

circuit in the launcher area. The same lines carry dc signals without interfering with the gyro azimuth signal and reference voltages.

(a) Four external wires carry the gyro azimuth signal and reference voltages to the launcher area from the composite telephone circuit. Both ac and dc sig nals are present and have separate paths through the composite telephone circuit. These signals are combined externally forming a true composite circuit. The ac and dc signals are prevented from interfering with each other by the use of capacitors C1 through C4 and inductors L1 and L2.

(b) A field telephone wire circuit is also included in this unit. The two wires

246

CONFIDENTIAL

in the field wire circuit form composite circuits in the same manner as the gyro azimuth circuits mentioned in *(a)* above. Capacitors C5 through C8 and inductor L3 prevent interference of one signal with the other.

91.1 (U). Electronic Frequency Discriminator 9990650

a. General. The electronic frequency discriminator is used in the jam strobe channel to convert the output from the amplifier-limiter to a video voltage of appropriate polarity and amplitude for use in the electronic gate.

b. Detailed Theory.

(1) The IF input signal is applied through IF IN connector J1 (fig. 49.7, TM 9-1430-257-20), developed across matching resistor R3, and coupled through capacitor C6 to the grid of IF amplifier V1. Inductor L1 in series with resistor R4 provide a grid return. Capacitor C7 stabilizes the bias voltage. A −10 volts bias is applied through connector P1-1 during calibration to cut off the amplifier. During operation, a −12-volt gate is applied from preknock to sync to allow the dc restorers to reclamp. Series resistors R5 and R6 form the cathode resistance. Unbypassed R5 provides degenerative feedback to stabilize the amplifier gain. Capacitor C8 across R6 stabilizes the cathode bias. Plate load inductor L5 and variable capacitor C14 form a tuned circuit which tunes the amplifier plate circuit to the correct frequency. Resistor R7 prevents spurious oscillations at the screen grid, and capacitor C9 bypasses screen grid RF to ground to stabilize the screen voltage. Networks Z1 and Z2 with capacitors C10 and C4 decouple RF from the plate power supply.

(2) The output of amplifier V1 is coupled through capacitors C15 and C16 to detectors V2A and V2B, which, with their associated components form a discriminator circuit. The input circuit to the plate of V2A, composed

of inductor L7, variable capacitor C18, and capacitor C20 is tuned to 48 megacycles. The input circuit to the cathode of V2B, composed of inductor L8 and variable capacitor C19 is tuned to 52 megacycles. The two frequency peaks are balanced in amplitude by adjustment of variable capacitor C14 in the output circuit of V1.

(3) A positive output voltage from detector V2A is developed across resistor R9 and capacitor C21 and applied to the summing circuit consisting of R11 and R12. A negative output voltage from V2B is developed across resistor R10 and capacitor C22 and also applied to the R11-R12 summing circuit. The output voltage at the junction of resistors R11 and R12 is applied to the control grid of cathode follower V3 and to grid 2 of differential amplifier V4. When the 48- and 52-megacycle inputs to V2A and V2B are equal in amplitude, capacitors C21 and C22 in the output circuits will be charged to equal and opposite voltages, and the output from the junction of the resistors will be zero. When the 48-megacycle input is greater, the output is greater from V2A and the output is positive. When the 52-megacycle input is greater, the output from V2B is greater and the output is negative. The output voltage will vary around a −6.3-volt reference which is developed in the voltage divider consisting of resistors R2 and R1 between −250 volts and ground and which is stabilized by capacitor C1.

(4) Cathode follower V3 is a dual triode with both sections connected in parallel. Resistors R13 and R16 are parasitic suppressors, and resistor R14 with capacitor C23 decouple the plate supply voltage. The output video is developed across resistor R15 and applied to the external electronic gate through JS VID OUT connector J2.

(5) Diode CR1 is connected to the junction of resistors R11 and R12. When the JS ALINEMENT switch S1 on the

auxiliary acquisition control indicator (fig. 49.2, TM 9-1430-257-20) is in the OPERATE or AUX ADJ position, the diode connection (fig. 49.7, TM 9-1430-257-20) is changed to the junction point between resistors R9 and R10. Diode CR1 clips the negative portion of the discriminator output so that only the positive portion which is at 48-megacycles is used as jam strobe video.

(6) Differential amplifier V4 amplifies the discriminator output and applies it to an external meter. Grid 7 of V4 is connected to the −6.3 voltage across R1 and serves to keep the meter reference at the zero input reference to the discriminator. Grid 2 is connected to the discriminator output. Resistors R17 and R18 are plate load resistors for the two sections of V4. The output from the two sections of V4 are applied through METER 1 and METER 2 connectors P1-7 and P1-9. The output of the two sections of V4 are balanced for no signal condition through resistors R19 and R20 in an external voltage divider network.

92 (U). Equipment Cooling Cabinet 8158225

The equipment cooling cabinet houses the equipment cooling fan described in paragraph 93 below. Also mounted in the equipment cooling cabinet is a 3-phase induction type motor for driving the equipment cooling fan and IFF decoder MX-1995/TPX.

92.1 (U). Equipment Cooling Cabinet 9985626

The theory of operation for equipment cooling cabinet 9985626 is the same as that for equipment cooling cabinet 8158225 discussed in paragraph 92 except for relay K1 added by DA MWO 9-1400-263-30. Coaxial relay K1 (D71, fig. 2.1, TM 9-1430-257-20), when energized, switches IFF video input to IFF decoder MX-1995/TPX from NAR (Nike acquisition radar) to AAR (auxiliary acquisition radar).

93 (U). Equipment Cooling Fan 8010350

a. General. The equipment cooling fan, located in the equipment cooling cabinet, provides air cooling for the vacuum tubes and other circuit components in the director station trailer. The equipment cooling fan is of the centrifugal (outward blowing from center of rotation) type and works in conjunction with the intake and exhaust shutters. The intake and exhaust shutters control the amount of air that is displaced. Equipment other than the equipment cooling fan shown in figure 50, TM 9-1430-257-20 is covered in paragraph 94.

b. Detailed Theory. The equipment cooling fan is driven by a 3-phase induction type fan motor B1 (fig. 50, TM 9-1430-257-20). Fan motor B1 is Y-connected to the 120-volt, 3-phase power supply through connectors J1-A, B, and C with neutral connected to connector J1-D. Fan motor B1 is started by placing MAIN POWER switch S4 and EQPT VENT switch S7 (both located on the acquisition power control panel) to the ON position. Two power factor correcting capacitors are connected across each of the 3-phase inputs to B1. Capacitors C1 through C6 are the power factor correcting capacitors. The power factor is the cosine of the phase angle between the current and voltage in the circuit. If the power factor can be made to approach unity, the power lost in the circuit due to the reactive components is small. The power factor is unity when the current and voltage are in phase. The capacitors across each of the input phase counteract the inductive effect of the induction motor, thereby reducing the phase angle between the current and voltage.

94 (U). Miscellaneous Cabinet-Mounted Components of Utility Cabinet 8010602

a. General. The miscellaneous cabinet-mounted components of the utility cabinet may be divided into four basic items; shutter and damper level, indicators, relays, and switches.

b. Detailed Theory.

(1) Shutter and damper lever. The shutter and damper lever (fig. 108) has a 5-position slide opening (close, 1/4, 1/2, 3/4, open) to regulate the ex-
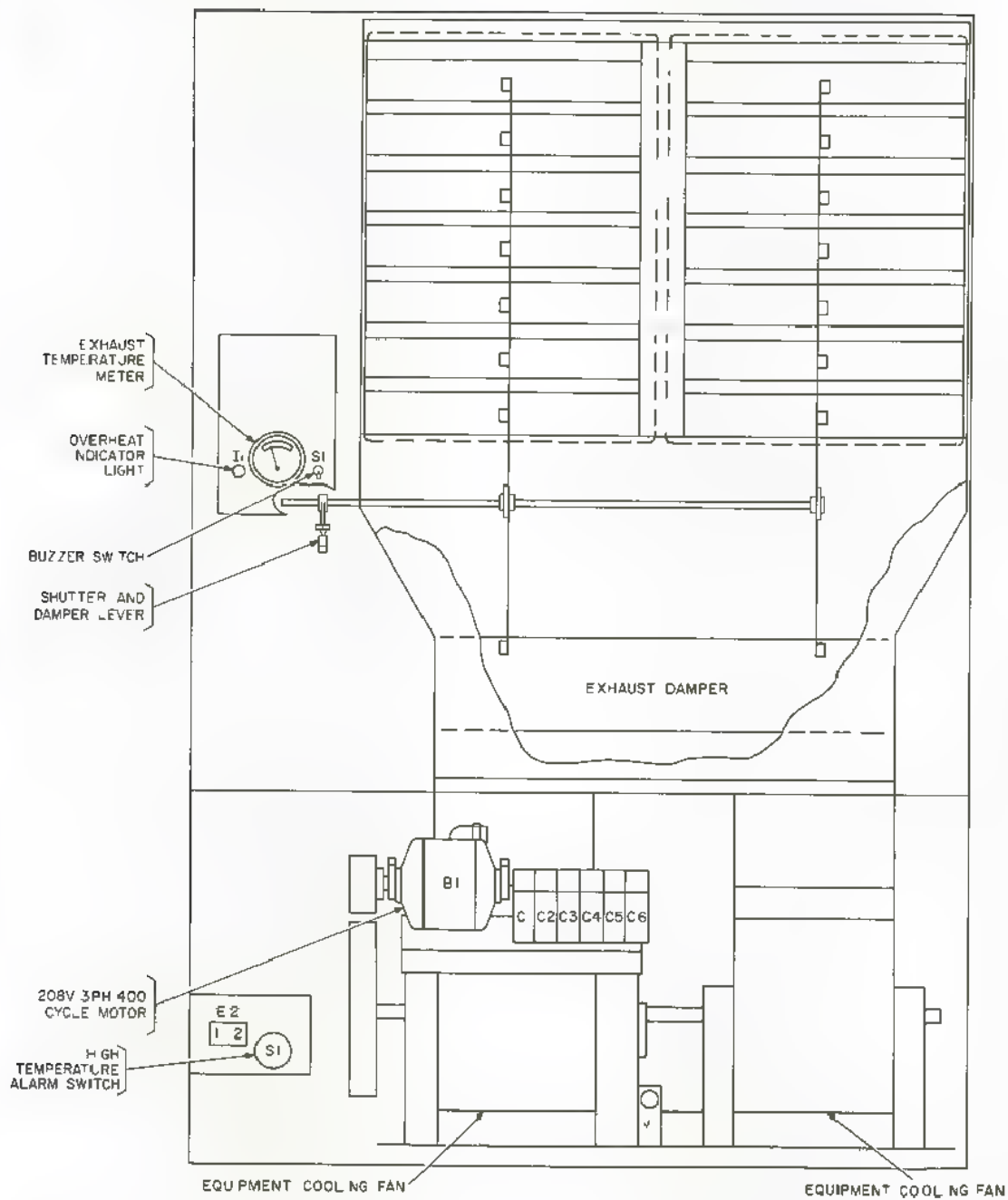
Figure 108 (U). Utility cabinet—miscellaneous cabinet-mounted components.

RA PD 468697

haust damper, and thus control the flow of air through the equipment cooling system.

(2) *Indicators.* Overheat indicator light I1 (fig. 50, TM 9-1430-257-20) is a visual overheat indicator, and buzzer indicator I2 is an audible overheat indicator. When the exhaust temperature reaches 140° F, high temperature alarm switch S1 closes and applies ground through connector TB1-5, thus completing the circuit for I1 and I2. EXHAUST TEMPERATURE meter M1 (fig. 108) is a temperature indicating meter used in conjunction with S1. The temperature range of M1 is from 20' to +180° in increments of 5° F.

(3) *Relays.* Overheat relay K1 (fig. 50, TM 9-1430-257-20), in the deenergized condition, completes the circuit for I2 through contacts 10 and 3. Relay K1 is energized by operating buzzer switch S1. When K1 is energized, contacts 10 and 3 are opened and I2 is silenced.

(4) *Switches.* Buzzer switch S1, when operated, applies a ground through connector TB1-6 and completes the energizing circuit for K1. High temperature alarm switch S1 is of the thermal type and is located in the exhaust portion of the cooling system. High temperature alarm switch S1 is designed to close when the exhaust temperature reaches 140° F and remain closed until the temperature decreases to 130° F.

95 (U). Target Data Processing Unit 9990673 and Auxiliary Acquisition Interconnecting Box 9986480

a. General. The target data processing unit and auxiliary acquisition interconnecting box provide space for monitoring terminal boards, subassemblies, relays, fuses, and fuse indicator lamps that are associated with the FUIF equipment, auxiliary acquisition radar (AAR), and antijam display (AJD).

b. Detailed Theory. The target data processing unit and auxiliary acquisition intercon-

necting box (fig. 46.2, TM 9-1430-257-20) incorporate the following subassemblies for AJD:

(1) Auxiliary electronic frequency converter 9990588 (fig. 49.6, TM 9-1430-257-20) described in paragraph 98.

(2) Main electronic frequency converter 9990577 (fig. 49.3, TM 9-1430-257-20) described in paragraph 97.

(3) Amplifier-limiter 9156529 (fig. 49.4, TM 9-1430-257-20) described in paragraph 99.

(4) Wide band IF amplifier 9990700 (fig 49.5, TM 9-1430-257-20) described in paragraph 100.

(5) Electronic frequency discriminator 9990650 (fig. 49.7, TM 9-1430-257-20) described in paragraph 91.1

(6) Auxiliary acquisition control-indicator 9990687 (fig. 49.2, TM 9-1430-257-20) described in paragraph 96.

c. Miscellaneous Cabinet Mounted Components. The theory of operation of the target data processing unit and auxiliary acquisition interconnecting box is similar to the theory of operation of the FUIF interconnecting box and cover discussed in paragraph 87. Normal IF, main IF, and auxiliary IF from the receiver-transmitter is detected, combined and converted into ACQ IF (IF, Dicke Fix or normal IF) and jam strobe (JS) video for the director station group circuits. ADJ relay K1 switches normal or main IF into ACQ IF filter. The ACQ IF filter is an extremely narrow band 60 megacycle bandpass filter of 1 megacycle. Main and auxiliary IF is coupled from the main and auxiliary electronic frequency converters through narrow bandpass IF filters of 1 megacycle. The main IF channel filter is centered at 48 megacycle and the auxiliary IF channel filter is centered at 52 megacycle. The outputs of these two filters are coupled into the IF coupler. The IF coupler is a hybrid coupler which combines the 48- and 52-megacycle IF signals into a composite IF signal output. Transformers T1 and T2 supply 6.3-volt ac to filament circuits. Transformers T1 through T4 in the auxiliary acquisition interconnecting box are used to couple preknock, sync, and IFF video signals from the AAR to the Nike system and sync from the acquisition radar system to the tracking radar system. Switches S1 through S4 are low-voltage inter-

locks. Indicator lights DS5 and DS6 indicate ac voltage is present.

96 (U). Auxiliary Acquisition Control-Indicator 9990687

a. *General.* The auxiliary acquisition control-indicator acts as a test panel for easy alignment and adjustment of the jam strobe channel. The indicator provides the appropriate switching of associated relays, correct bias voltages, blanking waveforms and meter for adjustment indications.

b. *Detailed Theory.*

(1) TEST ENABLE relay K1 (fig. 49.2, TM 9-1430-257-20), is energized by the high voltage interlock circuits. K1 is energized only when the transmitter is turned off. When the transmitter is turned on K1 deenergizes and returns all circuits associated with JS ALIGNMENT switch S1 to the operate condition regardless of the position of S1.

(2) The operations of JS ALIGNMENT switch S1 is described below:

(a) *OPERATE.* Contacts 1-6 of S1-B connect crystal diode CR1 in the differential amplifier circuit of the electronic frequency discriminator which removes the negative portion of the jam strobe video. In this manner video output from the jam strobe channel is limited to returns from the main beam of the acquisition antenna. Contacts 7-12 of S1-B connects the jam strobe blanking waveform from AGC into the input grid circuit of IF amplifier V1 in the electronic frequency discriminator. The blanking waveform cuts off V1 during the preknock to sync pulse interval. This action allows dc restorers in associated video circuits to reclamp during clockwise jamming. Resistor R17 is an input matching resistor and crystal diode CR3 block positive excursions of the blanking waveform.

(b) *CALIBRATE.* Through contacts 8-12 of S1-B a 10-volt negative dc bias from resistor R4 and R5 is applied to the input grid of IF ampli-

fier V1 in the electronic frequency discriminator. This bias cuts off V1 and prevents signal from the grid circuits of V4 in electronic frequency discriminator. Balancing voltage from BAL resistor R16 and resistor network R13 through R15 is applied to the cathode circuit of differential amplifier V4 in the electronic frequency divider. The output from the plate circuit of V4 is applied to meter M1. Crystal diodes CR1 and CR2 and resistors R1, R2, and R3 insure proper polarity and current through M1. BAL resistor R16 is adjusted to obtain a zero reading on M1.

(c) *AUX ADJ.* A negative 10 volts bias from the junction of resistors R6 and R9 is connected through contacts 15-18 of S1-B to the gain controlled stages of the main electronic frequency converter. AUX BIAS resistor R11 is adjusted for meter M1 to read —15 units. This adjustment insures that the gain of the auxiliary electronic frequency converter is sufficient to overcome noise present in the amplifier-limiter.

(d) *MAIN ADJ.* Contacts 4-6 of S1A enables the noise generators in the main and auxiliary channels. Contacts 11-12 of S1-A energize relay K1 in the main electronic frequency converter. When K1 in the main electronic frequency converter is energized a 10 db pad is removed from the converter input. The gain of the main channel is set to match that of the auxiliary channel. The output of the electronic frequency discriminator is coupled into the M1 meter circuit through contacts 16-18 of S1-A. The main channel gain is adjusted so that a zero reading is obtained on M1. SEN switch S2 is depressed which energizes relay K1 in the auxiliary electronic frequency converter. This action inserts a 2 db pad into the input circuit of the converter. M1 is then read to measure the amount of unbalance caused

248.3

by a 2 db difference in power to the main and auxiliary channels.

(3) Capacitors C1 and C2 provide ac decoupling for the dc bias circuit. Varistor RV1 provide regulation for relay K1

97 (U). Main Electronic Frequency Converter 9990577

a. *General.* The main electronic frequency converter is used in the jam strobe (JS) channel to convert the 60 megacycle main IF to 48 megacycle for further processing in the power comparator section of the JS channel.

b. *Detailed Theory.*

(1) Main IF signals are coupled through IF IN connector J1 (fig. 49.3, TM 9-1430-257-20) to relay K1 and matching resistor R1. With K1 deenergized, contacts 1-5 of K1 couple the signal through a 10db attenuator consisting of resistor R2 and R3 to DF IF OUT connector J3. From R1, the signal is coupled through contacts 3-6 of K1 to a tuned circuit composed of the primary of transformer T1 and capacitors C1 and C2. When switch S1 in the auxiliary acquisition control indicator is set to MAIN ADJ position, K1 is energized, removing the IF from the dicke-fix channel.

(2) The 60 megacycle signal is coupled through T1 to the control grid of IF amplifier V1. The output from V1 is coupled through coupling transformer T2 to the control grid of IF amplifier V2. Bias voltage from the auxiliary acquisition control-indicator is applied from connector P1-A through rf filters consisting of resistor R35, capacitors C13, C14, and C16, and filters Z1 and Z2 to the control grid circuits of V1 and V2. Cathode-resistor bias for V1 and V2 is provided by capacitors C3, C4, and resistors R6 and R11, while degenerative bias resistors R5 and R10 increase stability. Resistors R7 and R12 are screen grid dropping resistors. Resistors R8 and R13 are plate dropping resistors. Resistors R4, R9, and R14 provide impedance matching for T1, T2, and T3. The output of V2 is coupled through T3 into a 75 ohm ferrite core transformer T4, whose secondary couples balanced 60 megacycle signals to the control grids of mixers V3 and V4.

(3) Crystal Y1 maintains the output frequency of oscillator V6 at 108 megacycles. Excitation for Y1 is coupled through capacitor C19 and resistor R26 from the V6 plate circuit. The tuned grid circuit of V6 is comprised of C18, inductor L3, and resistor R27, while the tuned plate circuit is comprised of inductor L4, dropping resistor R29, C19, and R26. The output of V6 is coupled through capacitor C22 and across resistor R30 to the input grid of buffer amplifier V7, which provides signal amplification while preventing loading of the oscillator circuit. The output of V7 is fed through inductor L5, capacitor C26 and C27, forming a tuned circuit, to the primary of ferrite core transformer T6. Inductor L6 is an rf choke. Resistors R28 and R32 are screen grid dropping resistors, while C21 and C24 are screen bypass capacitors. Cathode bias for V7 is provided by resistor R31 and capacitor C23. Capacitor C28 and resistor R33 in the secondary of T6 provide grid leak bias for the mixer grids of V3 and V4. OSC BIAS test point TP1 permits monitoring of the oscillator output.

(4) The 108 megacycle signal at T6 is applied to grid 7 of both V3 and V4. The output plate circuit of V3 and V4 is tuned to 48 megacycles by inductors L1 and L2 and capacitor C9. When the 60-megacycle IF is present at grid 1 of the mixers, a resultant 48 megacycle signal is developed across resistor R20 and applied to the control grid of IF amplifier V5. During the interval between IF pulses, the 108 megacycle signal is effectively canceled and mixers V3 and V4 have no output. The 48 megacycle signal is coupled through T5 to JS IF OUT connector J2. Cathode resistor bias for V3 and V4 is provided by resistors R17, R19, and

capacitors C7 and C8. BAL variable resistor R18 is adjusted for balanced conduction through V3 and V4. Cathode bias for V5 is supplied by resistors R21, R22, and capacitor C10. Resistors R15, R16, and R23 are screen grid dropping resistors. Resistor R24 provides impedance matching for the output of V5 to T5. Capacitors C11 and C12 tune the secondary of T5 for a 48 megacycle output.

(5) Filtering for the +150-volt supply is provided by filters Z3 through Z8 and capacitors C15, C17, C20, C25, C29, C30, and C32. Resistor R34 and capacitor C31 comprise a low frequency noise filter. Capacitors C33 through C40 and inductors L7 through L13 prevent interaction of the IF signal in the filament circuit.

98 (U). Auxiliary Electronic Frequency Converter 9990588

a. General. The auxiliary electronic frequency converter is used in the jam strobe (JS) channel to convert the 60 megacycle main IF to 52 megacycle for further processing in the power comparator section the JS channel.

b. Detailed Theory.

(1) Auxiliary IF signals are coupled through IF IN connector J1 (fig. 49.6, TM 9-1430-257-20) to contacts of relay K1. With relay K1 deenergized, contacts 5-1 and 3-6 couple the signal direct to the tuned primary of transformer T1. The tuned circuit is comprised of the T1 primary and capacitors C1 and C2. When switch S1 in the auxiliary acquisition control-indicator is set to MAIN ADJ position, K1 is energized, placing a 2db attenuator consisting of resistors R1, R2, and R3 into the external input circuit which provides adjustment of the auxiliary channel.

(2) The 60-megacycle signal is coupled through T1 to the control grid of IF amplifier V1. The output from V1 is coupled through transformer T2 to the control grid of IF amplifier V2. Bias voltage from the auxiliary acquisition control-indicator is applied

from connector P1-A through rf filters consisting of resistor R35, capacitors C13, C14, and C16, and filters Z1 and Z2 to the control grid circuits of V1 and V2. Cathode-resistor bias for V1 and V2 is provided by capacitors C3, C4, and resistors R6 and R11, while degenerative bias resistors R5 and R10 increase stability. Resistors R7 and R12 are screen grid dropping resistors. Resistors R8, and R13 are plate dropping resistors. Resistors R4, R9, and R14 provide impedance matching for T1, T2, and T3. The output of V2 is coupled through T3 into a 75 ohm ferrite core transformer T4, whose secondary couples balanced 60 megacycle signals to the control grids of mixers V3 and V4.

(3) Crystal Y1 maintains the output frequency of oscillator V6 at 112 megacycles. Excitation for Y1 is coupled through capacitor C19 and resistor R26 from the V6 plate circuit. The tuned grid circuit of V6 is comprised of C18, inductor L3 and resistor R27, while the tuned plate circuit is comprised of inductor L4, dropping resistor R29, C19, and R26. The output of V6 is coupled through capacitor C22 and across resistor R30 to the input grid of buffer amplifier V7, which provides amplification while preventing loading of the oscillator circuit. The output of V7 is fed through inductor L5, capacitor C26, and C27, forming a tuned circuit, to the primary of ferrite core transformer T6. Inductor L6 is an rf choke. Resistor R28 and R32 are screen grid dropping resistors, while C21 and C24 are screen by-pass capacitors. Cathode bias for V7 is provided by resistor R31 and capacitor C23. Capacitor C28 and resistor R33 in the secondary of T6 provide grid leak bias for the mixer grids of V3 and V4. OSC BIAS test point TP1 permits monitoring of the oscillator output.

(4) The 112-megacycle signal at T6 is applied to grid 7 of both V3 and V4. The output plate circuit of V3 and V4 is

tuned to 52-megacycles by inductors L1 and L2 and capacitor C9. When 60-megacycle IF is present at grid 1 of the mixers, a resultant 52 megacycle signal is developed across resistor R20 and applied to the control grid of IF amplifier V5. During the interval between IF pulses, the 112-megacycle signal is effectively canceled and mixers V3 and V4 have no output. The 52-megacycle signal is coupled through T5 to JS IF OUT connector J2. Cathode resistor bias for V3 and V4 is provided by resistors R17, R19, and capacitors C7 and C8. BAL variable resistor R18 is adjusted for balanced conduction through V3 and V4. Cathode bias for V5 is supplied by resistors R21, R22, and capacitor C10. Resistors R15, R16, and R23 are screen grid dropping resistors. Resistor R24 provides impedance matching for the output of V5 to T5. Capacitors C11 and C12 tune the secondary of T5 for a 52-megacycle output.

(5) Filtering for the +150 volt supply is provided by filters Z3 through Z8 and capacitors C15, C17, C20, C25, C29, and C30. Resistor R34 and capacitor C31 comprise a low frequency noise filter. Capacitors C33 through C40 and inductors L7 through L13 prevent interaction of the IF signal in the filament circuit.

99 (U). Amplifier-Limiter 9156529

a. *General.* Two amplifier-limiters are used in the jam strobe (JS) channel to obtain the necessary degree of limiting and filtering to enable stronger signal capture principle operation. The amplifier receives 48- and 52-megacycle composite IF signals from the hybrid IF coupler. A power difference of 2db at the input causes the output signal to be entirely at the frequency of the stronger of the two input frequencies

b. *Detailed Theory.*

(1) The composite IF signal is coupled into the amplifier-limiter (fig. 49.4, TM 9-1430-257-20) through IF IN connector J2, across resistor R34 and through capacitor C1 to inductor L1,

where it is developed and applied to the control grid of amplifier V1. The signal is amplified and coupled through transformer T1 to amplifier V2, amplified again, and coupled through transformer T2 to the grid circuit of V3.

(2) The grid circuit of V3 contains a pair of crystal diodes CR1 and CR2, with both CR1 "cathode" and CR2 "plate" at ground. CR1 and CR2 are low capacity, high speed switching diodes that conduct on signals greater than 0.5 volt and effectively limit the signal amplitude. The transitionally-coupled tuned transformers in the plate circuit of each limiter stage acts as a filter to reshape the bandpass characteristics of the amplifier before limiting takes place in the grid of the following stage.

(3) If the signal at the grid of V3 is greater than one volt peak-to-peak limiting action takes place. The limited signal appears at the grid of V4, increased 12db in gain by V3 and reshaped filtering action of T3. V4 amplifies the signal by another 12db and transformer T4 again filters the signal. Crystal diodes CR3 and CR4 in the grid of amplifier V5 limits the signal to one volt peak-to-peak and the whole process is repeated in the last three stages of amplifiers V5, V6, and V7. The output is coupled from the tuned secondary of transformer T7 to IF OUT connector J3 into the second amplifier limiter unit. The amplifier limiter has a center frequency of 50 megacycles, with a midpower-point bandwidth of 12 megacycles. With two amplifier-limiters cascaded, the overall midpower-point is reduced to 8 megacycles. The effective gain for a single unit is approximately 90db.

(4) When the 48-megacycle signal from the main channel is larger than the 52-megacycle signal from the auxiliary channel, the amplifier limiter captures the stronger signal. The output is then at 48 megacycle and the

electronic frequency discriminator has a positive output which is used as JS video in the composite antijam display. The only time the 48-megacycle IF main channel signal can be larger than the 52-megacycle IF auxiliary channel signal is when the major lobe is not pointing at the target or jamming source.

(5) Amplifier bias is cathode resistor developed with an additional small unbypassed resistor providing slight degeneration to increase stability of the circuit. Detuning resistor R35 and capacitor C36 in the +150-volt supply circuit prevent interaction with IF frequency signals.

100 (U). Wide Band IF Amplifier 9990700

a. General. The wide band IF amplifier is a 10-megacycle bandpass IF amplifier which amplifies and provides hard limiting for all signals and normal noise. Two of these amplifiers are connected in series in the dicke-fix receiver channel to limit any input signal. The input signal is amplified in each amplifier stage until the signal reaches the amplitude necessary to cause limiting. Depending on the strength of the input signal, first limiting will take place in the first amplifier or the first limiter stage in the second amplifier. The gain of the amplifier is such that receiver noise causes limiting in all stages of the second amplifier. The power output of the second amplifier will remain constant regardless of input signal amplitude.

b. Detailed Theory.

(1) The 60-megacycle input signal is applied through IF IN connector J1, developed across terminating resistor R1, coupled through capacitor C1 and applied to the control grid of amplifier V1. Inductor L1 resonates with C1 as a series tank, such that the input impedance appears as a pure resistance. Resistor R2 provides degenerative feedback to stabilize the gain of V1. R30 is the cathode bias resistor and C17 is the cathode bypass capacitor. Resistor R3 is the screen dropping resistor. The IF signal is amplified and inverted by V1 and coupled to the primary of IF transformer T1,

with the output signal on the secondary of T1 being coupled directly to the control grid of amplifier V2. Resistors R4 and R5 broaden the bandpass of T1 to provide the proper bandwidth. Resistor R6 is unbypassed to provide degenerative feedback to stabilize the gain of V2. C8 is the V2 cathode bypass capacitor. The cathode bias resistance is composed of resistor R32 in series with the resistance through transistor Q2 and or Q1. The IF signal is amplified and inverted by V2 and coupled through transformer T2 to the control grid of amplifier V3. Resistors R8 and R9 broaden the bandpass of transformer T2, R7 is the V2 screen dropping resistor, and variable capacitor C2 tunes the V3 control grid circuit to 60 megacycles.

(2) Amplifier stages V4 and V6 operate the same way as does stage V2, and amplifier stages V3, V5, and V7 operate the same way as V1, except that the secondary of T7 may be tuned to 60 megacycles by variable capacitor C7 in parallel with capacitor C6. The output is coupled directly to IF OUT connector J2.

(3) There are three limiting circuits in the amplifier, each composed of two transistors with their associated components. These are transistors Q1-Q2, Q3-Q4, and Q5-Q6. Since these circuits are identical, only the Q1-Q2 circuit will be discussed.

(4) Transistor Q2 is normally turned on by a positive voltage on its base which is developed in the voltage divider network composed of diodes CR2, CR8, and resistor R35 from +150 volts to ground through the secondary of T2. When Q2 is turned on, the cathode resistance is through R32 and from the collector to the emitter of Q2 to ground. The collector-emitter impedance is very low when Q2 is turned on. When a jamming signal of sufficient amplitude to cause the output signal from the T2 secondary to exceed approximately 1 to 2 volts is applied to the input of V2, the negative

portions are passed through diodes CR2 and CR7. Diode CR7 acts as rectifier and capacitor C10 as a filter. The negative voltage is passed through CR8 and applied to the base of transistor Q2, turning Q2 off. The collector-emitter impedance of Q2 rises rapidly to a high value and the cathode circuit of V2 is now through R33 and the base-emitter resistance of Q1 and resistor R34 to ground. This also turns on normally off transistor Q1. The cathode voltage of V2 rises to a much higher positive value and lowers the gain of V2 by the increased bias Simultaneously, the low collector-emitter resistance of the now on transistor Q1 is in parallel with resistor R30 This action increases the gain of V1 because the cathode voltage is reduced through the low resistance to ground. This action also causes a positive voltage drop across resistor R34 which is applied to the cathode of diode CR1. This action keeps the positive portions of the signal from being clipped and shunted through CR1 to ground. When the jamming signal is removed the amplifier clipping circuits return to their normal condition Since the gain of V1 is increased slightly when the gain of V2 is decreased by the limiting action, the signal to noise ratio is decreased and better performance is realized. Since a constant power output is desired from the second wide band IF amplifier, the limiting action will occur in one of the limiter stages in the second amplifier with only normal noise

and signal input to the first amplifier. The signal strength of the jamming signal will determine whether limiting begins in the first, second, or third limiting stage. When one limiting stage operates, however, all succeeding limiting stages will operate.

(5) Resistor R48, capacitors C26 through C34 and C43, and networks Z1 through Z7 forms a detuning and decoupling circuit for the +150-volt supply and prevents interaction between amplifier stages. Capacitors C35 through C42 and inductors L2 through L8 prevent interaction between stages and keep the IF signals out of the filament supply.

101 (U). Fixed Attenuator 9993003

a. General. The dicke-fix IF output from the wide band amplifiers is applied to the fixed attenuator. In normal system operation without AJD (antijam display) the dicke-fix IF is terminated in the fixed attenuator. With AJD the IF signal is attenuated so that the AGC bias to the narrow band IF amplifiers will be the same for normal and dicke-fix IF signals.

b. Detailed Theory. Dicke-fix IF is coupled from IF IN connector J1 (fig 46.3, TM 9-1430-257-20) through attenuator pad consisting of resistors R1, R2, and R3. Relay K1 is normally deenergized. With contacts 6-3 of K1 made, the IF is terminated across the attenuator pad. When the system is in AJD operation relay K1 energizes and the IF signal is attenuated approximately 20db and fed through contacts 6-4 and 5-2 of K1 to IF OUT connector J2. Crystal diode CR1 maintains regulation across relay K1 energizing coil.

APPENDIX

REFERENCES

1. Publication Indexes

The following indexes should be consulted frequently for latest changes or revisions of references given in this appendix and for new publications relating to material covered in this manual.

Index of Administrative Publications.	DA Pam 310–1
Index of Blank Forms	DA Pam 310–2
Index of Ordnance Corps Supply Manuals.	DA Pam 310 29
Index of Technical Manuals, Technical Bulletins, Supply Bulletins, Lubrication Orders, and Modification Work Orders.	DA Pam 310–4

2. Supply Manuals

Antenna – Receiver – Transmitter Group OA 1596/T (9000228), Derrick, Acquisition Antenna (7613500), and Harness Assembly (8007435) (NIKE-HERCULES Antiaircraft Guided Missile System)	TM 9–1430–250–35P/2
Director-Computer Group, Missile OA–1479/MSA–19 (8511317) (NIKE-HERCULES Antiaircraft Guided Missile System).	TM 9-1430–250–35P/4
Director-Computer Group Guided Missile (9143988) (Improved NIKE-HERCULES Antiaircraft Guided Missile System)	TM 9–1430–250–35P/9

3. Forms

DA Form 5 31, Shop Job Order Register
DA Form 9-12, Inspection of Ordnance Equipment
DA Form 9-79, Parts Requisition
DA Form 9-80, Job Order File
DA Form 9-81, Exchange Part or Unit Identification Tag
DA Form 11-3, Shop Tag
DA Form 421, Stock Record Card
DA Form 468, Unsatisfactory Equipment Report
DD Form 6, Report of Damaged or Improper Shipment
DD Form 250, Materiel Inspection and Receiving Report

4. Other Publications

Accident Reporting and Records.	AR 385–40
Army Safety Policy	AR 385–10
Assembly and Emplacement. Radar Course Directing Cen-	TM 9–1430–251–10/1

tral (NIKE-HERCULES and Improved NIKE-HER-CULES Antiaircraft Guided Missile System).

Authorized Abbreviations and Brevity Codes.	AR 320–50
Check Procedures: Acquisition Radar System (NIKE-HER-CULES Antiaircraft Guided Missile System) (Includes Check Sheets).	TM 9–1430–250–12/1
Check Procedures: Acquisition Radar System (Less HIPAR) (Improved NIKE-HERCU-LES Air Defense Guided Missile System) (Includes Check Sheets).	TM 9–1430 250–12/2
Dictionary of United States Army Terms.	AR 320–5
Use, Care, and Maintenance of Electric Motors.	TM 9-244
Field Maintenance: Acquisition Antenna–Receiver–Trans-mitter Group (NIKE-HER-CULES Antiaircraft Guided Missile System).	TM 9–1430–254–34/1
Field Maintenance: Director-Computer Group (NIKE-HERCULES Antiaircraft Guided Missile System).	TM 9 1430 251 34
Instruction Guide: Ordnance Preservation, Packaging, Storage and Shipping.	TM 9 1005 _First Aid For Soldiers FM-21-11_
Logistics (General): Electronic Failure Report.	AR 700–39
Logistics (General): Unsatisfactory Equipment Report	AR 700–38
Lubrication	TM 9–2835
Military Symbols	FM 21–30
Operation· Radar Course Directing Central (NIKE-HERCULES Antiaircraft Guided Missile System).	TM 9 1430–250–10/1
Operation: Radar Course Directing Central (Improved NIKE-HERCULES Air Defense Guided Missile System).	TM 9–1430 250 10/2
Operation and Organizational Maintenance. Voice Communications System (NIKE-HERCULES and Improved (NIKE-HERCULES Antiaircraft Guided Missile Systems).	TM 9 1400–251–12
Ordnance Maintenance: Materials used for Cleaning, Pre-	TM 9–1007

INDEX

CONFIDENTIAL